

SCT Module Controller Update August '08

Mitch Newcomer
Penn

Status

The basic concept of an SCT Module Controller ASIC to interface between the Stave and Module Front End chips has been accepted since the Spring '07. Although there has been significant progress in the past year in understanding potential readout schema, the basic MCC functionality is not specified well enough to begin work due mostly to the lack of a coherent readout architecture (and data/control protocol) that sets out the functionality of all three primary SCT ASICS: FEC or ABCx (Front End Chip), MCC (Module Controller Chip), SCC (Stave Controller Chip).

Now that the ABCn ASIC has been submitted a higher level of interest is being given to the generic problem of how to readout multiple front end ASICs. The immediate result is that a group of specialists is being gathered by Philippe Farthouat and Alex Grillo to meet regularly and examine / develop a candidate architecture that will allow specification of the module readout and expedite the development of an SCT MCC.

MCC Issues TBD

- Data Readout – perhaps best understood but not fully defined. 40/80/160MHz? Probably bi-directional token passing, but Daniel Lamarra from Geneva has a significantly different proposal.
- Command / Clock / L1 - Encode Clock and Command? Break out L1? Send separately? Keep Clock separate (multi-speed?) Encode clock and command as they are?
- Redundancy - Two MCC's per module? Independent? Tandem?
- Power -
 - Does the MCC participate in module level voltage regulation?
 - Serial Power will make it difficult to include Independent DCS monitoring / functionality
- Technology – The technology used for the MCC needs to be compatible with the next version of the ABC chip. It would be useful to choose a candidate FEC process so that designers can re-use some of the blocks and transfer some of their MCC design experience to the next FEC design.

Many of these issues are stylistic, not show stoppers. A working group should be able to prioritize and develop the necessary specifications for an MCC proptotype within a six month time frame.

Current State of the Art MCC

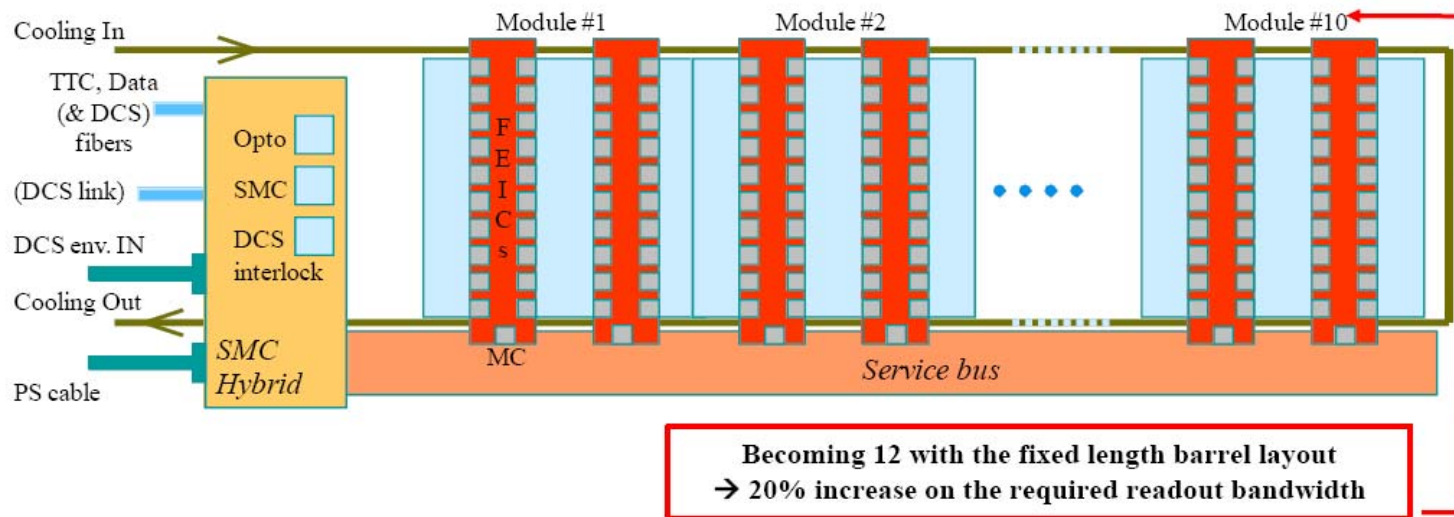
The following slides were given at the July 2, at the ABCn / Module Readout meeting By Philippe Farthouat (with input from Alex)

They encapsulate much of the conversation that has taken place over the past year in developing an approach for module readout for the upgrade.

Architecture paper

- ▶ The readout architecture paper introduced the module controller in the readout chain
 - ▶ Hybrid controller would be more appropriate as the readout is organised around hybrids
- ▶ Interfaces ABCn – Stave controller
- ▶ Basic functionality
 - ▶ Receives TTC signals from the stave controller
 - ▶ Distributes them to the ABCn of the hybrids
 - ▶ Max 20 ABCn
 - ▶ After each L1A it gathers data from the ABCn and sends them to the stave controller
 - ▶ DCS functionality to be embedded

Sketch of stave readout



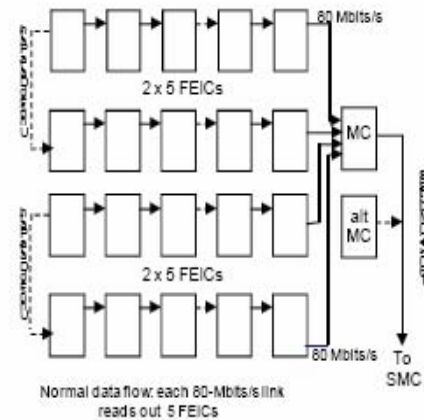
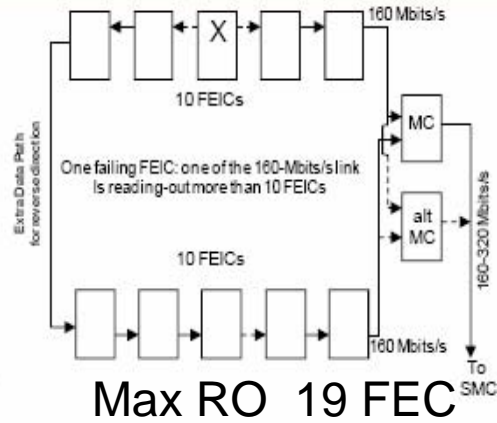
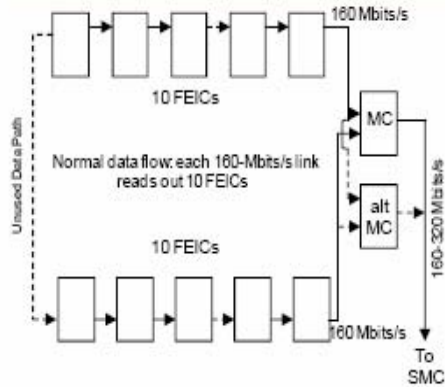
► One side of half a barrel stave (short strips)

Readout path (1)

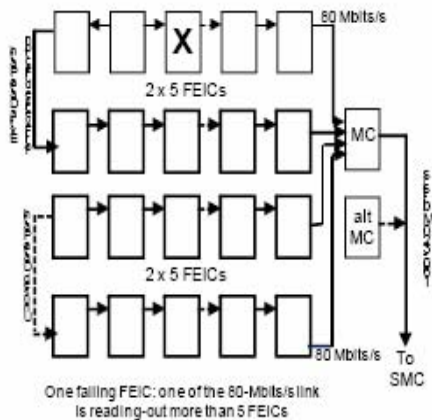
ABCn sharing a data path at 160 Mbits to MC

- ▶ Simulations have shown that at SLHC and with a safety margin of about 20% on the hit occupancy, 80Mbits/s is enough for reading out 20 FEIC (short strips)
- ▶ A MC readouts an hybrid with two links but that for redundancy reason a link could be used for reading out up to 19 FEIC
 - ▶ → at least 80Mbits/s should be available for the connection FEIC-MC
- ▶ It is felt safer to allow more bandwidth because the safety factor applied is not so high and one should anticipate
 - ▶ Possible higher luminosity
 - ▶ Remember the machine is now planning a x2-3 improvement in 2012-2013
 - ▶ A possible L1A rate higher than 100 kHz

Readout path (2)



Max RO 9 FEC



Module Data Clk 160MHz

- ▶ Two possible schemes for redundancy and readout

- ▶ One could accept half the speed at the cost of extra links on the hybrid

Module Data Clk 80MHz

Readout path (3)

- ▶ The output bandwidth should not be relaxed and requires at least 160 Mbits/s
 - ▶ One output link for 20 ABCn
 - ▶ Increasing the number of data links MC → SMC has a lot of impact on the “service bus” and on the SMC board
- ▶ Data format, protocol and sharing of “header responsibility” (who is introducing BCID, L1ID, etc.) to be defined

- ▶ SMC → MC not yet defined
 - ▶ Will depend on multidrop capability at different speed
- ▶ MC → ABCn
 - ▶ Either we keep an encoded transmission
 - ▶ Single line or two lines (1 clock + 1 data)
 - ▶ More than 80 Mbits/s required to allow simultaneous L1A and commands (e.g. BCR)
 - ▶ Or we separate command and L1A at the MC level
 - ▶ Lower speed for command
 - ▶ Higher number of lines on the hybrid
 - ▶ Multidrop capability to be seriously studied

Architecture document and next steps

- ▶ The document is being updated and should always be updated
 - ▶ Layout change
 - ▶ After decisions have been taken
 - ▶

- ▶ ABCn specs and MC specs to be defined
 - ▶ Working group to be formed
 - ▶ List to be established
 - ▶ Bi-weekly phone meeting
 - ▶ Sharepoint web site for sharing documents
 - ▶ <https://espace.cern.ch/project-atlas-stripsreadout/default.aspx>
 - ▶ Can we get reasonable specs for the upgrade tracker workshop?

First Steps towards an MCC ASIC

1. Choose Technology (IBM 130nm for instance) Note that choosing a highly advanced technology increases prototyping costs, reduces the number of available prototyping cycles and can reduce the number of participating institutions due simply to the large investment in training and cost of tools required. **It would probably be wise on all fronts to choose the least sophisticated technology that can meet reasonable power and performance requirements.**
2. Identify Candidate Blocks and begin designs: PLL, LVDS Rcvr/Driver, Data Buffer-> Tag -> Concentrator, Monitors?
3. Develop FPGA Module readout compatible with ABCn to readout .25um ABCn ASIC. Requires a module hybrid with specialized connector with access to Stave / Module Data and Control lines.
4. Converge on a **Conservative** set of protocol / architecture choices for FEC and MCC. Attempt to understand tradeoffs:
Wiring complexity vs Clock Speed and Digital Encoding Complexity.
Use FPGA as test bench were possible.
5. Physicists → Define Realistic Redundancy Goal

MCC / FEC ASIC Technology

Requirements:

Long Term Availability

Radiation Tolerance

Low Power Operation

Compatibility with Analog Front End Requirements

Other Considerations:

Affordability:

→ first: Prototyping Costs Schedule

→ finally: Production Costs

Accessibility to design tools

IBM 130nm CMOS Processes

- CERN Frame contract assures Long term 130nm Process.
- Studies at CERN indicate high radiation tolerance of the Native CMOS IBM 130nm process. Gate around transistors will likely be un-necessary significantly lowering the power requirement from previous 250nm Designs.
- Appears to be compatible with either a pure CMOS or SiGe Bipolar analog Front End.

Preliminary Look at **relative** Digital Power Requirements for 130nm / 250nm Rad Tolerant CMOS Technology

Digital Design Studies → Brandon Bloch and Jake Hindenburg (Penn undergrads)

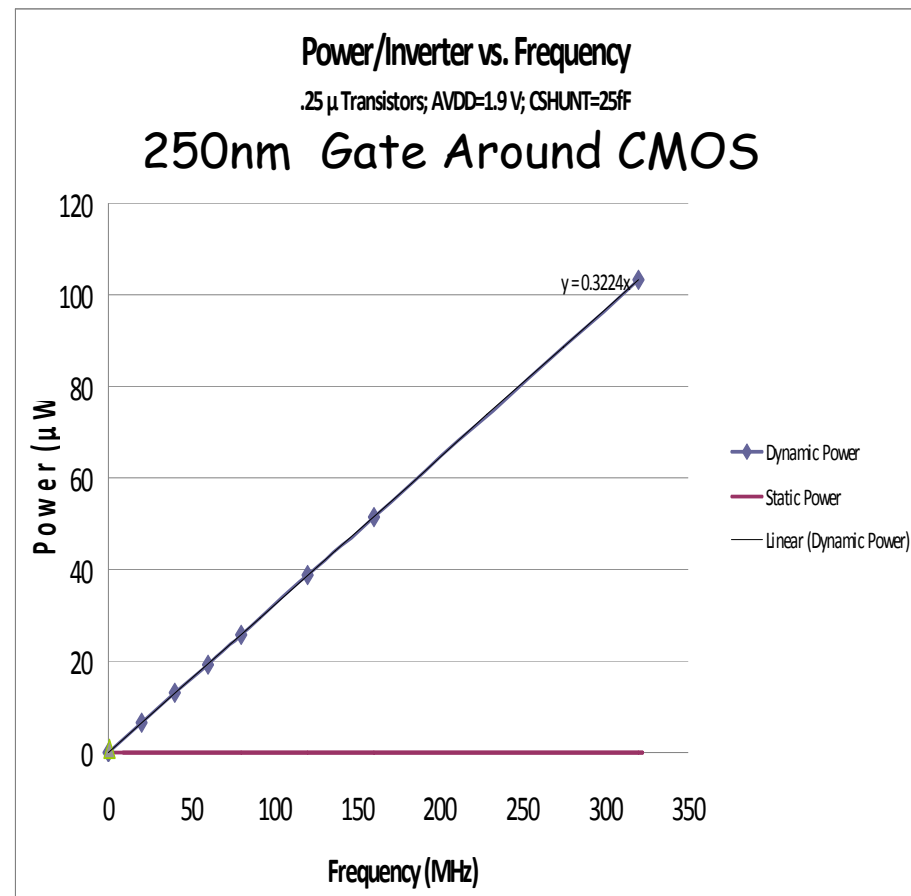
$\frac{1}{4}$ μm Reference

To begin we designed and studied a CMOS8RF (250nm) (RAL Digital Library parts) inverter chain with 2X drive six levels deep. Our previous work with this process showed that 25fF was a reasonable wiring load.

PMOS $W = 14\mu\text{m}$

NMOS $W = 8\mu\text{m}$

We found Acceptable response (Full rail to rail logic swings) out to 320MHz at 1.9V.



Preliminary Look at **relative** Digital Power Requirements for 130nm / 250nm Rad Tolerant ASIC Technology

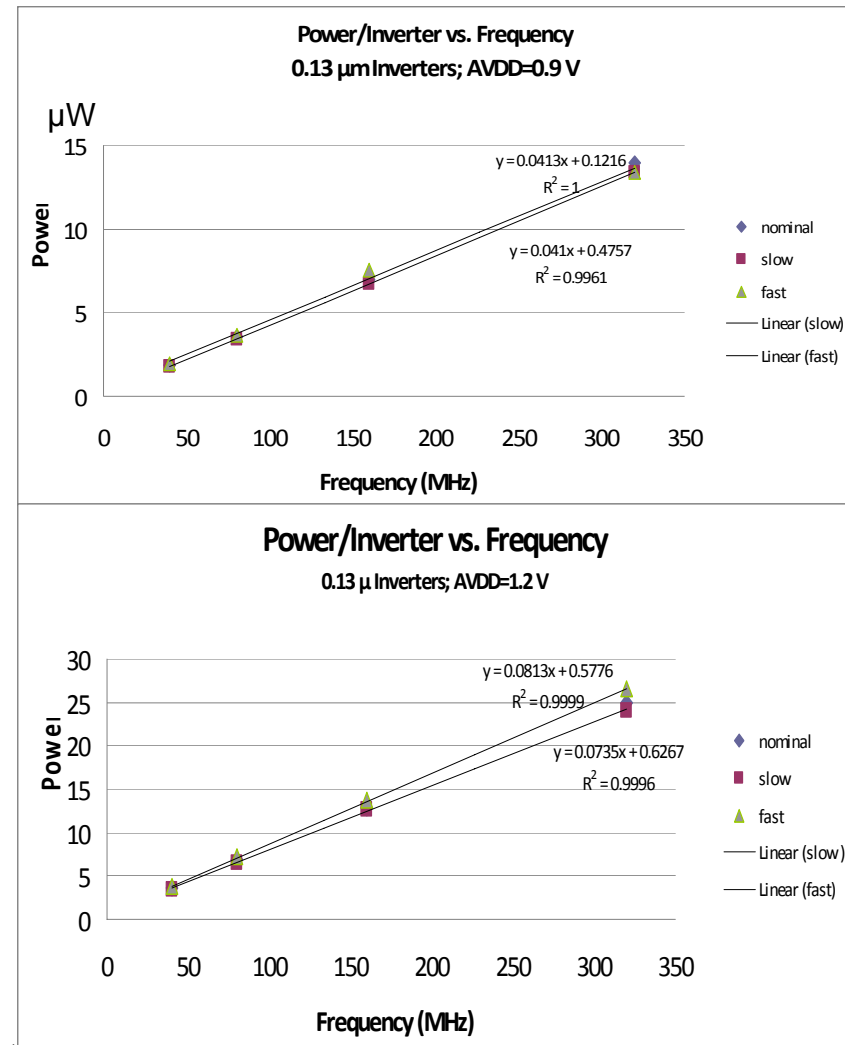
130nm candidate Technology

CERN uses the ARTESIAN Digital library parts for their 130nm designs. Shane Smith (Ohio State) who has had the digital design training at CERN Provided the full set of inverter library sizes. We chose the 2X and imposed the same conditions as for the 250nm parts, scaling the inverter load from 25fF to 15fF.

PMOS $W=1280\text{nm}$

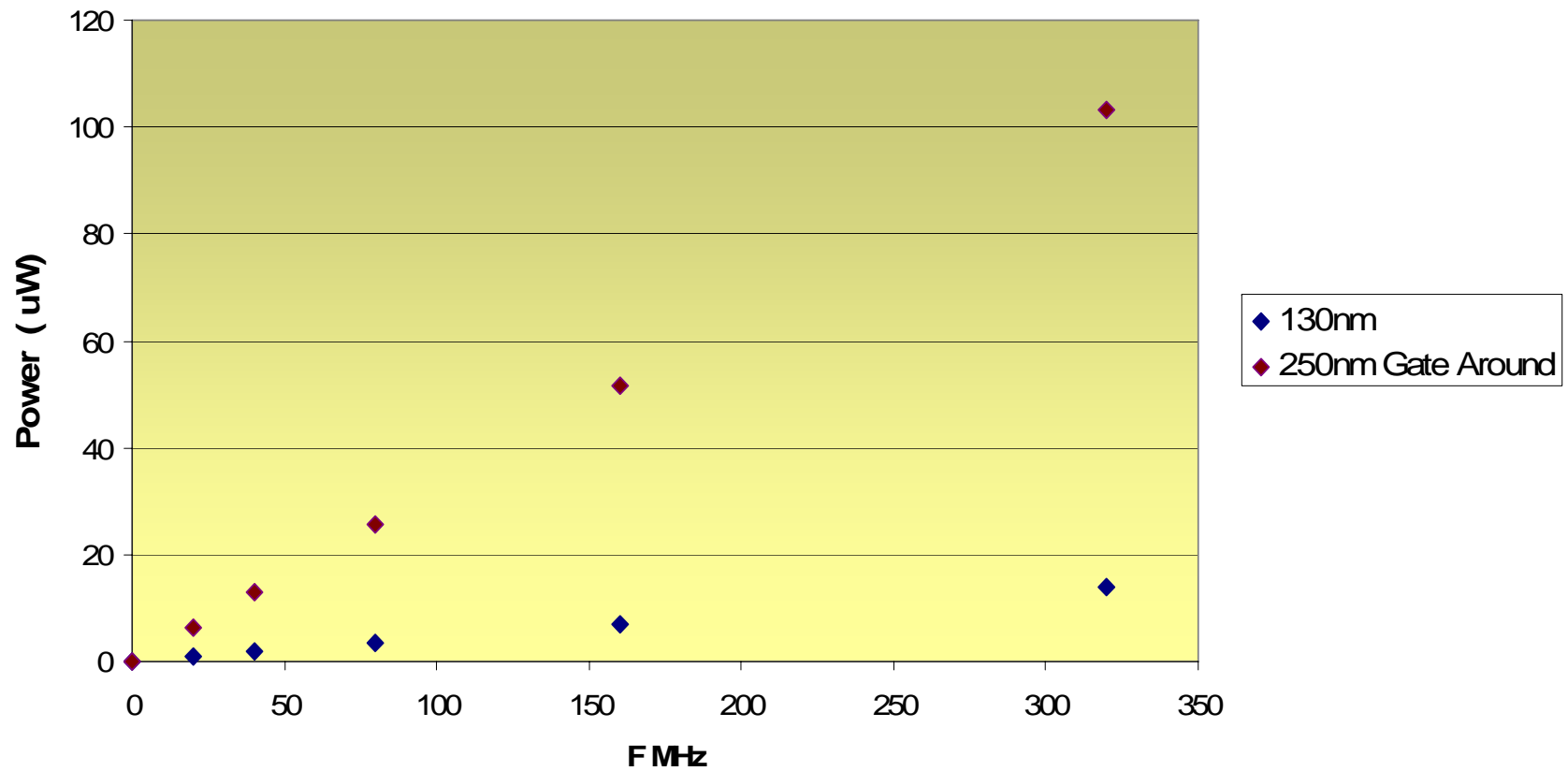
NMOS $W=920\text{nm}$

Note that we looked for and found the static leakage current but it was less than 1% of the total power consumption.

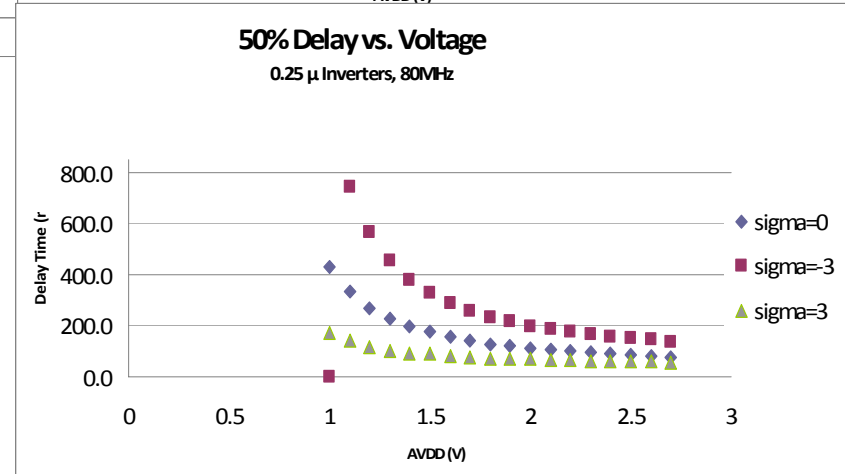
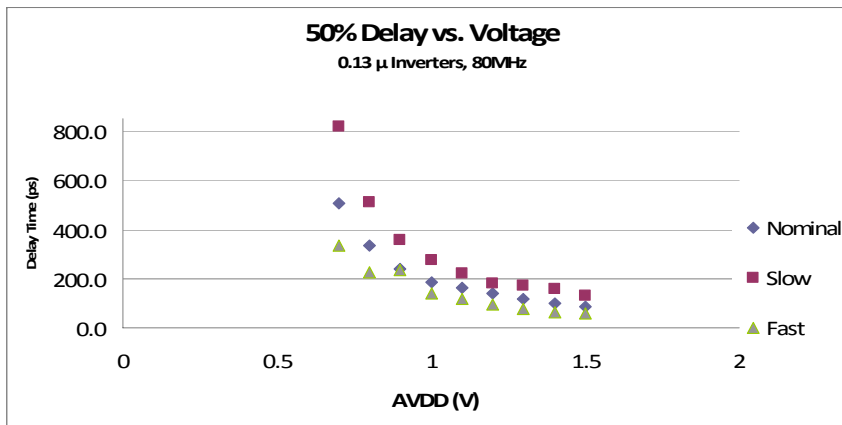
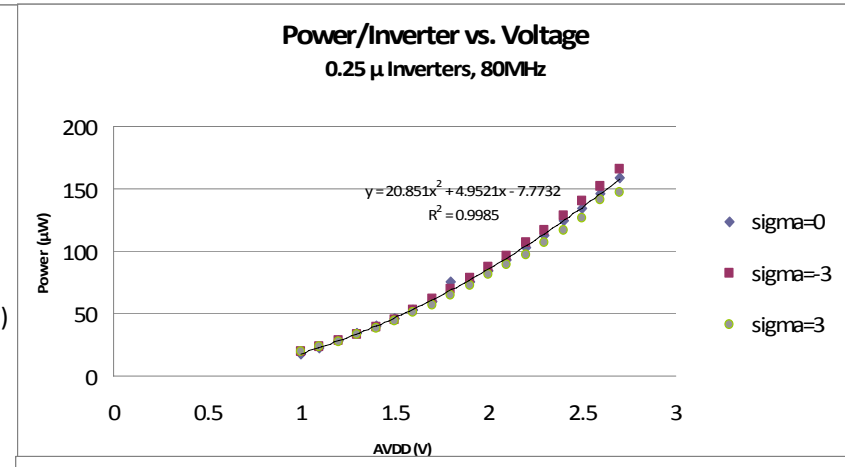
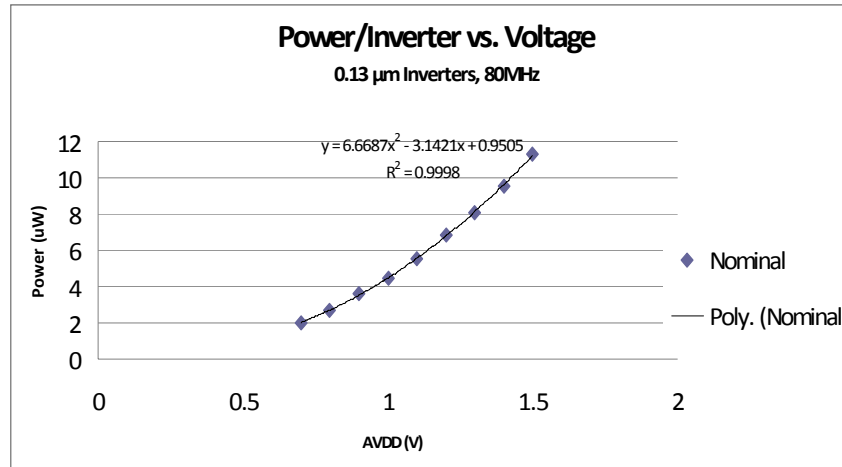


250 / 130nm Direct Comparison

Power / Inverter 250nm Gate Around and 130nm

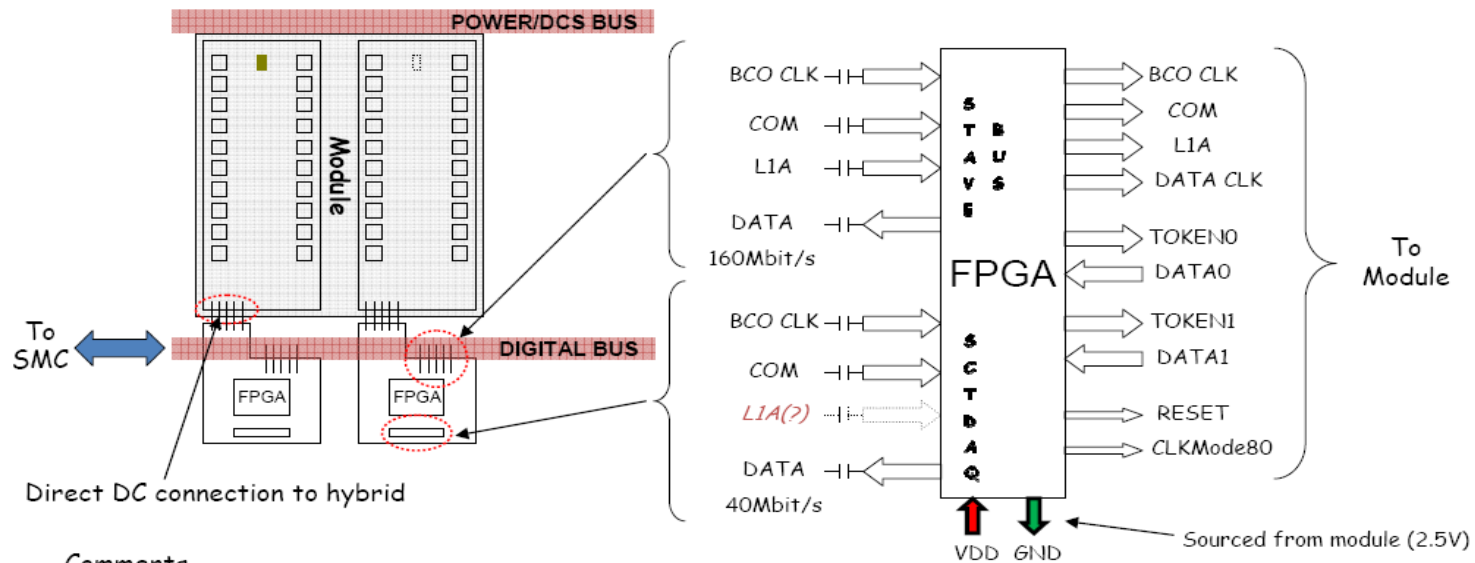


Power and Delay Vs Vdd



Ideas from Liverpool / Ral for an FPGA for a Prototype ABCn MCC

Within the work-frame of the UK WP8 group (DAQ), work has tentatively begun on a readout DAQ for exercising ABCn hybrid/module (small) assemblies



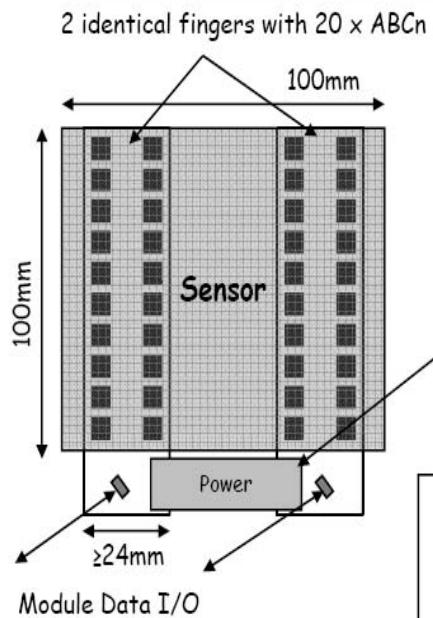
Comments

- Connections shown are absolute minimum - will increase if additional ABCn data redundancy paths added
- Module NTC (one per module?), power, DCS and HV distribution come in at top end of module
- FPGA connection to Stave Bus should be made via shortest physical route i.e. keep the stubs short!
 - Due to multi-drop LVDS (bus length $\geq 1m$)
 - Make use of dc-balanced signals
- Connection to hybrid is either by wire bond OR connector system i.e. make both available
- FPGA powered parasitically off module

Considerations for an FPGA Prototype MCC



Conceptual layout of the hybrid & build



Mezzanine Board (for prototyping)

Merges 2 fingers to form a 'single-sided module'

Provides real-estate for various powering schemes to be implemented...See later

Proposed Build

4 Cu Layers with Kapton dielectrics (example from LHCb VELO)

- 100 μ m track & gap, 150 μ m vias with 350 μ m via lands
- 2 x Outer layers 5 μ m Cu with additional 8 μ m plating
- 2 x Inner planes to be 12 μ m Cu
- 50 μ m Bond Ply (Espanex) between layers
- 200 μ m total build thickness
- Layer stack (top-down): Route1, Route2, Power & Ground
- Unusual stack ordering - final outer ground layer provides shielding

A more aggressive approach would be to consider removing the inner plane for trace routing and route the common electrical bus on the power plane

ABCn (MCC) Testing

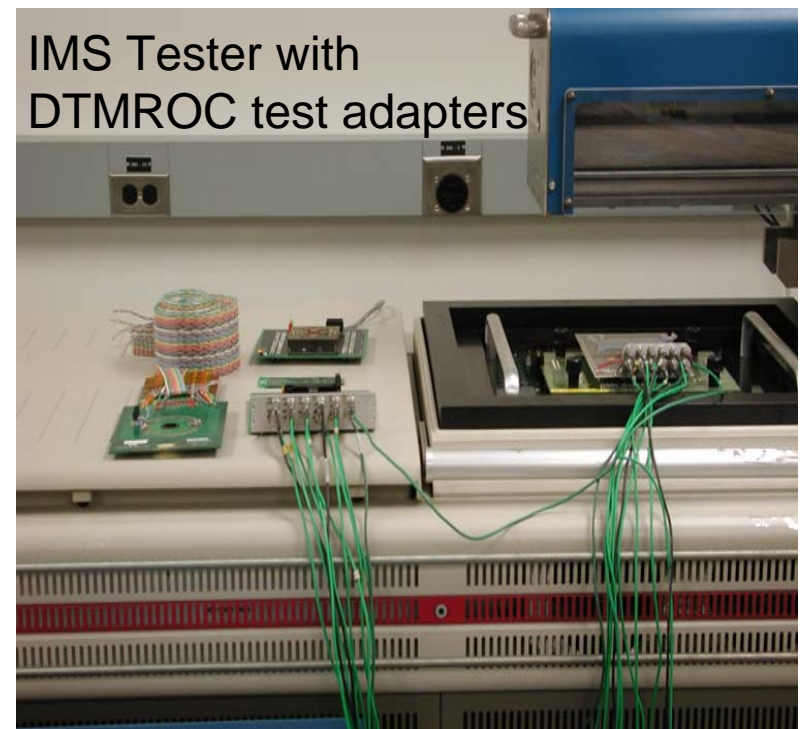
We propose to develop a wafer level test station for ABCn die verifying basic digital and analog functionality using Verilog based test vectors executed by our IMS tester with a manual wafer probe manipulator and custom wafer probe card.

Basic tests:

- Write and read back commands and status registers
- Read back Pipeline test data
- Threshold Noise ramps.
- Exercise Test Pulse
- Calculate channel noise induced occupancy
- Derive channel to channel offsets.

Log Results in an SQL database

ABCn testing can easily lead the way
towards MCC testing



Conclusions

- The formation of a module readout working group is a very encouraging step. Representation from hybrid and ASIC designers as well as Physicist input will be required for a “good” design.
- The 130nm CMOS appears to be an excellent candidate technology. It could reduce the predicted ABCn 2.5mW/channel digital power requirement by 8 - 10X.
- An adiabatic ramp up of the MCC design effort seems possible without compromising effort available within participating groups given the interest in using ABCn with FPGA module controllers as a test bed for potential readout improvements.