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Paper submitted to Nuclear Instruments and Methods in Physics Research A

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

Fabrication of 3D detectors with columnar electrodes of the same doping type

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Elsevier use only: Received date; revised date; accepted date

Abstract

Recently we presented a new 3D detector architecture aimed at simplifying the manufacturing process, making it more suitable for high volume production. In particular, the proposed device features electrodes of one doping type only, e.g., n^+ columns in a p-type substrate. In this paper we report on the fabrication at ITC-irst of the first batch of prototypes. The main issues related to the fabrication process along with preliminary results from the electrical characterization of different detectors and test structures are discussed.

PACS: 29.40.Wk; 29.40.Gx; 85.30.De
Keywords: Silicon detectors; Fabrication technology; Electrical characterization; 3D detectors; DRIE etching

1. Introduction

After they were first proposed by S. Parker et al. in the middle 90's [1], three-dimensional (3D) detectors have been the object of an ever increasing attention owing to their possibility to be fully depleted at very low voltages by acting on the layout of the vertical electrodes only, regardless of the substrate thickness. This property allows for very fast signal response and enhanced radiation tolerance, making 3D detectors very attractive for a variety of applications, including tracking of high-energy particles and X-ray imaging [see 2 and references therein]. Nevertheless, these advantages come at the expense of a quite complicated fabrication technology, involving several non standard steps, a fact that may become a major concern in view of future large volume production of these detectors.

In the framework of the CERN RD50 Collaboration, we have developed a new 3D detector architecture aimed at simplifying the manufacturing process [3]. The proposed device, in the following referred to as 3D-stc, features electrodes of one doping type only, e.g., n^+ columns in a p-type substrate, so that the column etching and doping are performed only once, resulting in a considerable

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process simplification. For the sake of completeness, it is worth citing that this approach has been independently developed by another group in Finland, that has reported on detectors featuring p^+ doped columns on n- substrates [4].

In a previous work, we have presented TCAD simulation results providing deep insight into the static and dynamic behavior of this detector, highlighting its advantages and potential drawbacks with respect to the original 3D detector design [3]. In this paper, the main processing issues are addressed and preliminary results from the electrical characterization of the first prototypes of 3D-stc are discussed.

2. Detector fabrication

The first batch of 3D-stc detectors has been fabricated on p-type, high-resistivity silicon substrates grown by Floating Zone (FZ) and Czochralsky (CZ) techniques, both with <100> crystal orientation. FZ wafers are 500-µm thick with a nominal resistivity of 5kΩcm, whereas CZ wafers are 300-µm thick with a nominal resistivity higher than 1.8 kΩcm. Detectors have all-n-type columnar electrodes extending deep into the bulk (down to 150 µm) but not extending all the way through it, so that additional steps related to the use of a support wafer are avoided. A uniform p^+ layer provides the ohmic contact on the detector backside.

The main processing issues, already reported in [3], are briefly summarized in the following with reference to the device cross-section of Fig. 1a:

- Boron implantation is used to obtain the ohmic contact on the backside and the isolation between n^+ electrodes on the front-side;
- circular columns with a diameter in the range 6 - 10 µm are etched by DRIE using thick oxide and photoresist layers as a mask;
- column n^+ doping is performed by Phosphorus diffusion from a solid source. It extends to a toroidal region around the top of the holes to ease contact formation;
- after doping, columns are only partially filled with an oxide layer;
- contact openings are defined inside the surface region only, out of the column hole;
- Aluminium sputtering is used for metal layer deposition.

All processing steps were carried out at ITC-irst, but the column etching, that was done at CNM in Barcelona by means of a DRIE machine. A SEM micrograph of a structure is shown in Fig.1b.

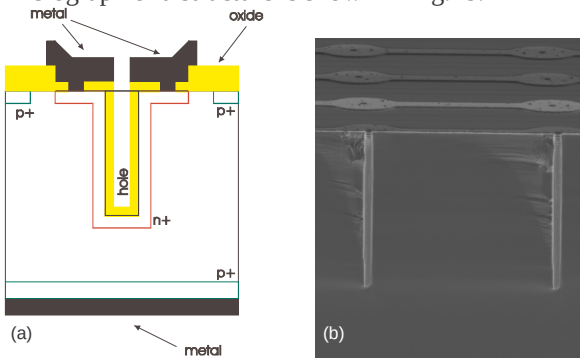

Fig. 1. (a) Schematic cross-section of one columnar electrode; (b) SEM cross-section of a 3D-stc structure.

In order to ease the electrical tests and the bonding to standard read-out chips for functional characterization, a strip-like layout has been chosen for the detectors. As an example Fig.2 shows the micrograph of a detector corner, where several columnar electrodes (one row) are connected by a metal strip, with a bonding pad at the end. All around, two frames of columnar electrodes act as guard-rings in order to shield the active volume from edge leakage currents. A magnified image of one column is also shown, where details can be observed. Several detector layouts have been designed, differing by the following options:

- two detector sizes have been considered, the first featuring an active area of 1 cm^2, and the second featuring an active area of 6 mm^2;
- column width: 6 to 10 µm;
- several pitches between columns have been considered, in the range 50 - 100 µm;
- either p-stops or p-spray have been used for surface isolation;
- either DC or AC coupling between strip diffusions and metal layers have been used. In AC coupled detectors, strips are biased by punch-through at both edges from the inner guard ring, acting as a bias ring. The same effect can be exploited for test purposes on DC coupled detectors.

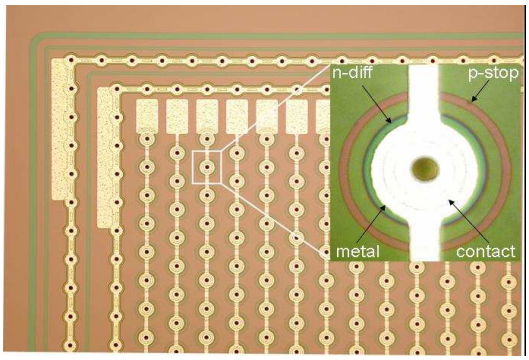

Fig. 2. Micrograph of a detector corner, with detail of one column.

Besides detectors, planar test structures (e.g., diodes, MOS capacitors, gated diodes) have been included in the wafer layout in order to monitor the main process parameters. 3D diode test-structures (both single-column and multi-column) are also present, in order to ease a comparison between measurement data and simulation results.

3. Experimental results

The electrical characterization of detectors and test structures has been performed at room temperature and under dark conditions by using a probe-station connected to a semiconductor parameter analyzer. For the sake of conciseness, only results relevant to devices fabricated on FZ substrates will be reported in the following. Similar results have been obtained on CZ wafers, although, due to thermal donor generation, much larger variations in the substrate doping concentration are present on CZ substrates, as also evidenced by other groups [5].

3.1. Planar test structures

Table 1 summarizes the main results obtained from planar test structures. Very low leakage currents are measured, comparable to typical values from good planar processes, thus assessing that the DRIE step does not cause any detrimental effect on the substrate. The reported values refer to a 100V bias; however, for those diodes having a lower breakdown voltage, the current value before breakdown is given. Early breakdown is observed on wafers with p-spray, as expected from simulations [3]. It should be stressed that, in all wafers, the diode breakdown voltage is lower than the full depletion voltage, so that the latter had to be estimated from the slope of the $1/C^2$ curves within the meaningful voltage range.

Also the surface related parameters confirm the good quality of the fabrication process, with slight differences between wafers implementing the two surface isolation options, as a result of the different thermal budgets characterizing the two process splits.

Table 1: Summary of the main results from planar test structures.

Parameter	Unit	Typical range	
		p-spray	p-stop
Substrate doping conc.	10^{12} cm^{-3}	1.6 – 2.3	
Depletion voltage	V	300 – 440	
Leakage current density	nA/cm^2	3.0 – 5.5	
Breakdown voltage	V	60 – 140	155 – 175
Field oxide thickness	nm	570 – 585	860 – 875
Field oxide charge density	10^{10} cm^{-2}	9.5 – 11.0	6.0 – 9.6
Surface generation velocity	cm/s	1.3 – 1.7	7.0 – 7.5

3.2. 3D detectors and test structures

Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements have been performed on 3D detectors and test structures.

From the capacitance values measured between columnar electrodes and substrate and between adjacent rows of columnar electrodes, we could infer the following information about detector depletion:

-the lateral full depletion between columns is obtained at a very low voltage (5V for 100µm pitch);

- the vertical full depletion of the substrate region below the bottom of the columnar electrodes is estimated at voltages of about 200V.

These values are in good agreement with the substrate doping concentration extracted from planar test diodes. Nevertheless, it should be stressed that in 3D devices the analysis of C-V data is not straightforward, since the measured capacitances are largely affected by surface non idealities that are strongly dependent on the layout (e.g., the MOS-like effect of probe pads and metal interconnections). Thus, in order to extract accurate values, 3D numerical simulations are currently being carried out, enabling to discriminate between intrinsic column capacitances and parasitic capacitances.

Leakage current measurements confirmed the good quality of the process. As an example, Fig. 3 shows the leakage current curves as a function of

reverse bias for eight, 1-cm^2 large, AC-coupled detectors featuring p-stop and p-spray isolation and different combinations of column pitches and diameters. As can be seen, at low voltage, the leakage current is very good, its values corresponding to less than 1pA per column for all detectors. Note that for detectors with p-spray, the punch-through voltage is higher so that the columns are biased at a lower effective voltage. This effect, together with a reduced surface contribution (see Table I), explains the leakage current difference observed in Fig.3.

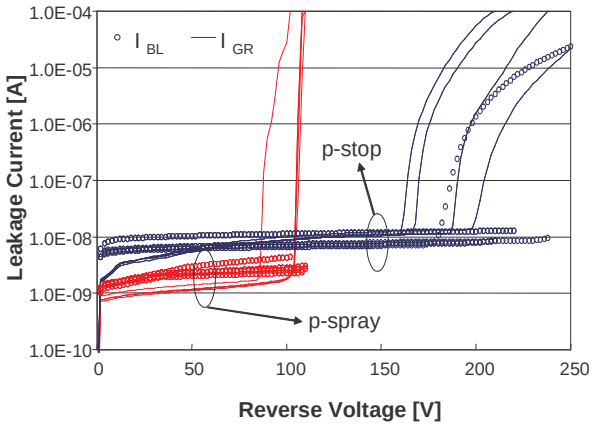

Fig. 3. Bias-line and guard-ring leakage currents vs. bias voltage in 8 AC coupled, 3D-stc detectors (4 with p-stop, 4 with p-spray).

At higher voltages, breakdown occurs on the guard-ring, and this can cause a sharp increase of the bias-line current too. For p-spray isolation the breakdown voltage is close to 50V, slightly lower than the value measured on planar diodes with p-spray; nevertheless, it should be mentioned that in planar diodes the presence of field-plates enhances the breakdown characteristics. For p-stop isolation, the breakdown voltage is ranging from 150 to 200V, that are approximately the same values observed for planar diodes. The good agreement between breakdown voltages on 3D and planar structures suggests that breakdown is located at the surface. According to the simulations [3], the surface is indeed the most critical point for breakdown if the substrate doping is low, that is the case for the devices considered in this study, whereas column tips can be of concern at higher doping concentrations. Fig. 4 shows the distribution of the bias line leakage current measured at 40V (i.e., before breakdown) on 70 detectors: only few detectors exhibit currents in excess of 50nA, evidence of the very good yield obtained with this process.

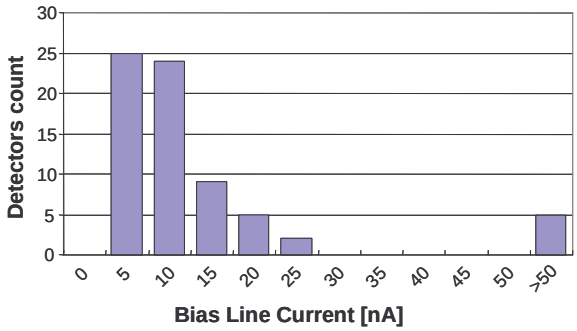

Fig. 4. Distribution of the bias-line leakage current measured at 40V on 70 3D-stc detectors with both p-stop and p-spray isolation.

4. Conclusions

We have reported on the first prototypes of 3D-stc detectors fabricated at ITC-irst. Preliminary results from the electrical characterization demonstrate the feasibility of the technological approach, with very good leakage current figures. A thorough analysis of device C-V characteristics with the aid of TCAD simulations is under way to gain deep insight into the depletion mechanisms characterizing these detectors.

Acknowledgements

Author S.R. wishes to thank the Provincia Autonoma di Trento for providing financial support under the grant program FPR-PAT 2003 HR-3D.

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