RD50 funding request

- Call March 2005-

Title of project: *Commercial production of prototype silicon strip detectors on 6" wafers of non-inverting substrates*

Contact person: *Hartmut Sadrozinski*
SCIPP, Nat Sci 2, UC Santa Cruz, CA 95064
(831) 459 4670
hartmut@scipp.ucsc.edu

RD50 Institutes:
1. *SCIPP, UC Santa Cruz, Bruce Schumm, schumm@scipp.ucsc.edu*
2. *Brookhaven National Lab., Zheng Li, zhengl@bnl.gov*
3. *PSI, Tilman Rohe, tilman.rohe@psi.ch*
4. *INFN Bari, Donato Creanza, donato.creanza@ba.infn.it*
5. *Purdue U., Daniela Bortoletto, bortolet@exchange.purdue.edu*
6. *Liverpool U., GianLuigi Casse, gcasse@hep.ph.liv.ac.uk*
7. *Syracuse U., Marina Artuso, artuso@physics.syr.edu*
8. *U. of New Mexico, Sally Seidel, seidel@panda3.phys.unm.edu*
9. *INFN Pisa, Alberto Messineo, alberto.messineo@pi.infn.it*

Request to RD50: *sfr 30,000*
Total project cost: *€ 60,000*

Project description (abstract):
This project is the outcome of the RD50 Workshop on p-type detectors in Trento in Feb. 2005. It will demonstrate to the LHC upgrade communities a first prototype of the detector technology for the "intermediate" tracking layers in future upgrade detectors with a fluence level of about 10^{15} cm^{-1}. Thus it is important that the fabrication be done by a commercial manufacturer on 6" wafers. Besides strip sensors (which could be common with a companion 4" proposal) of about 3 cm length and sufficient number of strips to allow reliable charge collection and noise studies as a function of fluence, we will include longer strips, full-size 2-D sensors, and pixel detectors. Processing will be done on several substrate types, which permit charge collection on the junction side throughout the detector lifetime.

Detailed Project description:
(for details, see the presentations at the RD50 Workshop on p-type detectors in Trento, February 28 on the Rd50 web page)

I. Motivation:

The progress of the RD50 working groups allows us to propose fabrication of strip detectors, which we can present to the CMS – ATLAS experiments as sensor prototypes for the tracking detector upgrade. Fabrication on 6" wafers and at a commercial manufacturer will prove that the ideas of RD50 can be transferred to commercial production, instead of being just "boutique-style" projects. In addition to the economic advantage of 6" wafers, they might be the only wafer size used by commercial manufacturers in a few years.

The sensors in upgrade tracking detectors will be finely segmented, i.e. consist of strips or pixels. There are many issues in sensor radiation damage which are related to both the segmentation and the substrate, like charge sharing, operation at under- or over-depletion, interstrip isolation and capacitance and so on, which can only be investigated with segmented detectors and not with pad diodes. Our proposal concentrates on studies on segmented detectors, and the interplay of surface processing techniques, strip geometry and wafer substrate in the sensor performance.

The new microstrip detectors included on this mask will target the fluence level expected at the innermost microstrip layer foreseen at the upgraded General Purpose Detectors (GDPs) at sLHC. In the inner part of the experiment there will be 3-4 layers of pixels, and microstrips will presumably start at the radius R = 20-30cm. The fluence level is a few times $10^{15}cm^{-2}$. In order to keep the same occupancy level as in the present LHC tracker, a simple scaling down factor of the cell size can be extrapolated from the present ATLAS and CMS geometries, and a strip length of 3cm for a strip width of 80um would fulfill the requirement of 1% occupancy. It was agreed that this geometry is to be kept as the most direct demonstrator for sLHC-like strip detector size, but a few other geometries are possible on the wafer. For example we want to include pixels (the present pixel devices of the RD50-FDS-1 mask could be kept as our pixel demonstrator), and longer strips to determine noise performance at larger radii.

II. Workplan

The RD50 workshop on p-type detectors held in Trento proposed to have two different production runs for silicon strip detectors: one using 4" wafers, concentrating on studying technology details like n-strip isolation and strip geometry questions, and one using 6" wafers, concentrating on charge collection, noise and system studies and on new structures like 2-D detectors and detectors with longer strips. There should be detectors with common layout in the 4" and 6" submissions to allow comparison between the fabrication runs. Processing on 6" wafers could be done by Sintef, Micron, and Colibrys. Hamamatsu will most likely be approached by the experiments.

The masks will be assembled by Liverpool, and ~20 wafers will be processed, subject to the number of appropriate substrate (see below).

The strip detectors fabricated with the proposed mask set in different substrates will be irradiated and used for the following studies:

a. Charge collection studies with min. ion. particles
b. Noise studies
c. N-strip isolation study
d. Different materials (MCz, Epi)
e. Geometry dependence
f. System studies: cooling, high bias voltage operation,

At the conclusion of these studies, RD50 will be able to recommend silicon strip technologies for the entire tracking region of the upgrade detectors beyond the innermost pixel layers. At that point, the experiments can start with the detailed work on these large systems, while the R&D for the more challenging innermost region continues, most likely based on non-planar detectors.

III. Background and previous work

An RD50 mask set has been already produced as part of a common project in 2004. The project will be completed by the CNM processing in 2005 (CNM-2005). In these masks there are also pixel structures. This mask set will be used by Micron for thick/thin detector comparison (140/300 μm). These masks have only p-spray isolation, but no p-stops. Micron is already producing large-scale n-in-n detectors with p-spray so they qualify as an experienced producer. We want to have a new mask set allowing a combination of p-stops and p-spray.

Wafer substrates of interest are:

A. p-type standard FZ (200 μm and 300μm)
B. p-type oxygenated by diffusion on few standard p-type (DOFZ)
C. p-type MCz Si
D. p-type epi >150μm
E. n-type MCz Si
F. n-type epi >150μm

All of them have been the subject of a processing run already completed or under way:

Material	Done or under way
A	CNM-2005
B	CNM-2005
C	SMART-2
D	CNM-2005
E	SMART-1
F	CNM-2005

The studies under way investigate material optimization. Of special interest is the performance of n-type MCz Si after irradiation in comparison with p-type FZ and MCz: is n-type MCz inverting or not? These studies would most likely reduce the list of interesting materials, and our new project can concentrate on investigating strip isolation and detector geometries, in addition to noise and CCE studies. If there is a common RD50 project on epitaxial detectors with sufficient thickness (>150μm), we will propose that two of our strip detectors are included in that mask so that we can reduce the number of required runs.

IV. Details on common structures

P-spray and p-stop

An investigation on the p-spray dose will be performed to ensure high breakdown voltage before irradiation. The advantage of p-spray isolation is that it provides extremely high breakdown voltage after irradiation. On the contrary, p-stop detectors behave better before irradiation and worse after irradiation. Possibly a combination of the two isolation techniques will prove to be the optimum. We will use the experience the pixel community has gained with the modified p-spray technique.

Strip geometry

As discussed above, the suggested strip length is 3cm, with a few longer strip detectors. The number of strips should be 128 to match the number of channels in presently available electronics analogue chips at LHC speed, and allow comparison with existing results. A preliminary strip definition are: pitch of 50-80-100μm, strip width over pitch ratio 0.25, metal overhang (after processing) of 2-3μm on both sides.

Wafer thickness

The detector thickness will not be a major constraint as p-type detectors, like n-on-n, or other non-inverting sensors, can work well non-fully depleted. It is suggested to test two thicknesses: 200μm, and 300μm. To ensure sufficient charge collection, the epi layers on wafers should be at least 150μm thick. Thinner active layers seem to have little support in the experimental community.

Project costs, contributions from participating institutes and request to the RD50 common fund:

Costs:

Processing in commercial foundry		€40,000
Mask Costs		€15,000
Wafers		€ 5,000
Total Costs		**€60,000**

Contributions:

BNL	$10,000	€ 7,692
Purdue U.	$ 2,000	€ 1,538
Liverpool	£10,000	€15,000
UCSC	$17,300	€13,308
INFN Pisa		€ 1,500
PSI	sFr 1,500	€ 1,000
Total Contributions		**€40,038**
Request from RD50	**sFr 30,000**	**€20,000**