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Investigation of design parameters for radiation hard silicon microstrip detectors

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Abstract

In the context of the development of radiation hard silicon microstrip detectors for the CMS Tracker, we have investigated the dependence of interstrip and backplane capacitance as well as depletion and breakdown voltage on the design parameters and substrate characteristics of the devices. Measurements have been made for strip pitches between 60 and 240 μm and various strip implants and metal widths, using multi-geometry devices, fabricated on wafers of either $\langle 1\,1\,1 \rangle$ or $\langle 1\,0\,0 \rangle$ crystal orientation, of resistivities between 1 and 6 kΩ cm and of thicknesses between 300 and 410 μm. The effect of irradiation on properties of devices has been studied with 24 GeV/c protons up to a fluence of 4.3×10^{14} cm^{-2}. © 2001 Elsevier Science B.V. All rights reserved.

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1. Introduction

The operation of silicon microstrip detector systems at the Large Hadron Collider (LHC) sets new demanding requirements on the performance of such systems. At design luminosity, several hundreds of particles will be produced every 25 ns. Their detection requires a tracking system with high granularity and fast response. In addition, the system as a whole, and the silicon detectors in particular, need to be sufficiently radiation hard to survive a period of 10 years of LHC operation. This implies in the most exposed regions of the silicon tracker an equivalent irradiation fluence of up to 1.6×10^{14} 1 MeV-neutrons/cm^2 and up to about 70 kGy of ionizing radiation [1]. This radiation damage will increase the bias voltage

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required for efficient charge collection to up to several hundreds volts, the leakage current to a few μA per strip and the oxide charge to the saturation value. Finally, in order to provide enough measurement points along the particle trajectory and to supply good angular coverage it is necessary to instrument a large volume with many detection planes, with a total surface to be instrumented of up to 200 m^2. These requirements go significantly beyond those of existing silicon microstrip detector systems.

The silicon microstrip detectors at LHC should operate with a single-to-noise ratio of at least 10:1 over the lifetime of the experiment. The signal level is directly proportional to the charge collection efficiency. Operation of detectors in overdepletion, with bias voltage up to several hundreds volts, is required to ensure an efficient charge collection efficiency also after the type inversion of the bulk, produced by the exposure to irradiation. An appropriate choice of the resistivity of the substrate material may limit the maximum bias voltage required for a good charge collection efficiency. The total noise figure, on the other hand, for an appropriate choice of the strip resistance and the bias resistors, is dominated by the intrinsic amplifier noise and by the leakage current shot noise [2]. The former scales with the capacitive load which the strips present to the preamplifier. The required short shaping time of around 25 ns mitigates the shot noise contribution, which increases with the square root of the shaping time, but it boosts the intrinsic amplifier noise which scales with the inverse square root of the shaping time. Therefore, it is crucial to understand the dependence of the total strip capacitance on the strip geometry and, where possible, to reduce it. The effect of irradiation on the interstrip and backplane capacitance must also be understood in order to ensure the performance of the silicon detectors over the LHC lifetime. It will be seen that this depends strongly on the choice of the crystal orientation of the silicon substrate. Finally, the requirement of stable operations at high bias voltage, and also the desire to use rather large strip pitches, make it essential to design the silicon sensors in such a way as to avoid an excessive electric field strength both at the strips and at the cutting edge.

The results reported in this paper were obtained in the framework of an R&D activity [3] for the silicon tracker for the CMS experiment [1]. As the strip pitches to be considered varied from 60 to 280 μm, these studies had to be performed over this wide range of strip geometries. In particular, measurements were needed for large strip pitches of more than 120 μm since there were no published results in the literature. As will be shown in the paper, the key geometrical parameter is the strip width-to-pitch ratio w/p (cf. Fig. 1). The final design of the strip is a compromise between the minimization of the total strip capacitance, which favours small values of w/p, and the requirement of high voltage stability, which disfavors small values of w/p.

The structure of this paper is as follows: In Section 2, the expectations for the detector electrical properties as a function of the detector geometry and of the substrate characteristics are reviewed. The experimental set-up and the measurement procedure used in the present study are described in Section 3. In Section 4, an overview of the measured backplane and interstrip capacitance as a function of the applied bias voltage and

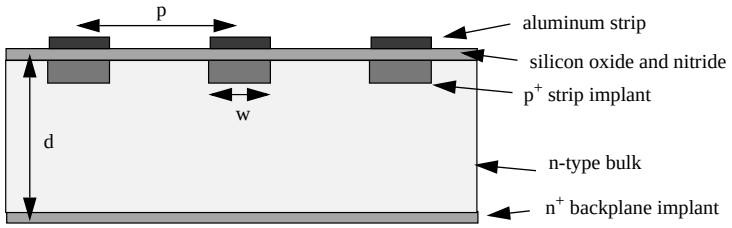

Fig. 1. Cross-section through an AC-coupled strip detector. Throughout the paper w will indicate the width of the p^+ implant, p the strip pitch and d the detector thickness.

measurement frequency is given. Capacitances and depletion voltage are then discussed as a function of the geometrical and substrate parameters (resistivity and crystal orientation), before and after exposure to irradiation, in Sections 5 and 6, respectively. In Section 7, the performance of the detectors at high voltages are discussed. The implications of the results on the sensor design which has been adopted for the CMS silicon tracker are discussed in Section 8.

2. Expected detector characteristics

2.1. Depletion voltage and backplane capacitance

In the most simple ansatz one could approximate the strip by a planar diode of thickness d and width p. In this case, the thickness of the depleted layer is

$$x = \sqrt{\frac{2\varepsilon_0\varepsilon_{\mathrm{Si}} V_{\mathrm{bias}}}{q_{\mathrm{e}} N_{\mathrm{eff}}}} \tag{1}$$

where N_{eff} denotes the effective doping concentration, q_{e} the electron charge, ε_0 the free space permittivity and $\varepsilon_{\mathrm{Si}}$ the dielectric constant of silicon. Therefore, full depletion is reached if the diode is biased at

$$V_{\mathrm{dep,diode}} = \frac{q_{\mathrm{e}} N_{\mathrm{eff}} d^2}{2\varepsilon_0\varepsilon_{\mathrm{Si}}}. \tag{2}$$

The backplane capacitance per unit length at full depletion is

$$C_{\mathrm{back,diode}} = \varepsilon_0\varepsilon_{\mathrm{Si}}\frac{p}{d}. \tag{3}$$

The fact that the width w of the strip is actually smaller than the pitch p modifies these two key parameters. A semi-analytical solution of Poisson's equation predicts [4]

$$\begin{aligned} V_{\mathrm{dep}} &= V_{\mathrm{dep,diode}}\left[1 + 2\frac{p}{d} f\left(\frac{w}{p}\right)\right] \\ &= \frac{q_{\mathrm{e}} N_{\mathrm{eff}}}{2\varepsilon_0\varepsilon_{\mathrm{Si}}}\left[d^2 + 2pdf\left(\frac{w}{p}\right)\right] \end{aligned} \tag{4}$$

$$\begin{aligned} C_{\mathrm{back}} &= C_{\mathrm{back,diode}}\frac{1}{1 + \frac{p}{d} f\left(\frac{w}{p}\right)} \\ &= \varepsilon_0\varepsilon_{\mathrm{Si}}\frac{p}{d + pf\left(\frac{w}{p}\right)} \end{aligned} \tag{5}$$

where f is a universal function which is numerically approximated by

$$\begin{aligned} f(x) = &-0.00111x^{-2} + 0.0586x^{-1} + 0.240 \\ &- 0.651x + 0.355x^2. \end{aligned} \tag{6}$$

All detector layouts analysed in this work are in the range $0.1 < w/p < 0.6$ where the function f monotonically decreases from about 0.65 to 0.10. Hence, compared to a diode one expects a higher depletion voltage and a lower backplane capacitance for the strip, this correction becoming smaller for larger values of w/p.

2.2. Interstrip capacitance

The capacitance of a strip to its neighbours (interstrip capacitance) often dominates the total strip capacitance. For the simplified case of a strip in between two semi-infinite plates, from which it is separated by gaps $(p - w)$, and infinite detector thickness, one can calculate the capacitance analytically [5]. In the range $0.10 < w/p < 0.55$ a good approximation is given by

$$C_{\mathrm{int},d\to\infty} \approx \left(0.8 + 1.9\frac{w}{p}\right)\ \mathrm{pF/cm}. \tag{7}$$

A backplane at a finite distance from the strips will reduce this capacitance as it reduces the volume of the dielectric.

2.3. Total capacitance

The relevant parameter for the electronics noise figure is total strip capacitance C_{tot}. It has been calculated by an electrostatic simulation [6] solving a two-dimensional Poisson equation. For a given pitch p, it predicts a linear dependence on the strip width w. In the range $0.10 < w/p < 0.55$, for a

detector thickness of 300 μm one obtains

$$C_{\mathrm{tot}} = \left(0.8 + 1.6\frac{w}{p}\right)\mathrm{pF/cm} \quad p = 100\ \mu\mathrm{m}$$
$$C_{\mathrm{tot}} = \left(0.9 + 1.4\frac{w}{p}\right)\mathrm{pF/cm} \quad p = 50\ \mu\mathrm{m}$$
$$C_{\mathrm{tot}} = \left(0.9 + 1.6\frac{w}{p}\right)\mathrm{pF/cm} \quad p = 25\ \mu\mathrm{m}. \qquad (8)$$

Predictions from this model have been compared with measurements for pitches varying between 25 and 80 μm. Agreement of up to 15% is found in Ref. [6].

It appears that the coefficients in Eqs. (8) for intercept and slope are rather similar for the different pitches. To the extent the parametrization is independent of p. It is also independent of d and therefore the total strip capacitance is approximately a function of the ratio w/p only. This somewhat surprising result is readily obtained from the observation that the total strip capacitance will not change if strip width w, pitch p and detector thickness d are all scaled by the same factor. If the total strip capacitance is also invariant under a common scaling of just the width w and the pitch p, then it cannot depend on the thickness d. Apparently, the decrease in backplane capacitance with increasing detector thickness is compensated by a corresponding increase in interstrip capacitance. The prediction that the total strip capacitance does not depend on the detector thickness d has not been found in the literature.

2.4. Radiation damage

The high particle flux at the LHC experiments will lead to radiation damage of both the bulk and the surface of the silicon detectors. The bulk damage is due to the non-ionizing energy loss (NIEL) which, through the displacement of atoms in the crystal lattice, creates new energy levels in the band-gap, effectively acting as acceptors. Therefore, the effective doping concentration will change and with irradiation, the initially n-type bulk will eventually behave under reverse bias as p-type (type inversion) [7]. As a consequence, the depletion voltage will go through a minimum at inversion and then rise linearly with fluence. The radiation-induced defects are not stable at room temperature. Some fraction can anneal with time (beneficial annealing). However, it is also found that the long-term annealing of the radiation-induced defects results in a further deterioration of the detector performance (reverse annealing). Both processes depend strongly on temperature and below 0°C reverse annealing is virtually completely suppressed. A further consequence of the radiation-induced energy levels is an increase of the leakage current. It rises linearly with the NIEL, irrespective of the type of radiation or the resistivity and crystal orientation of the substrate material. Therefore, using the damage cross-sections, a given irradiation fluence can be converted to a reference radiation type. It is a common practice to represent the intensity of any hadron irradiation by its equivalent fluence of 1 MeV neutrons. If one allows for full beneficial annealing, the proportionality factor between leakage current density i_{leak} and 1 MeV-neutron fluence Φ, known as the damage constant, is measured to be $\alpha_\infty = (2.9 \pm 0.2) \times 10^{-17}$ A/cm at 20°C [8]. At a given temperature T the leakage current density will be

$$i_{\mathrm{leak}} = \alpha(T_0)\Phi\left(\frac{T}{T_0}\right)^2 \exp\left(-\tau\left(\frac{1}{T} - \frac{1}{T_0}\right)\right) \qquad (9)$$

where T is the absolute temperature of the silicon and $\tau \approx 7020$ K.

The most relevant surface damage is the formation of trapped charges in the oxide and its interface to the silicon bulk. This charge is predominantly positive and therefore leads to the accumulation of an electron layer under the oxide in the region between the strips [9]. This in turn leads to an increase of the interstrip capacitance with irradiation. The density of trapping centres depends on the density of dangling bonds and thus on the crystal orientation of the wafer. For wafers with a $\langle 1\,0\,0 \rangle$ crystal orientation the saturation density of oxide charge is expected to be significantly smaller than for $\langle 1\,1\,1 \rangle$ [10].

3. Experimental set-up and measurements

3.1. Multigeometry detectors

In order to study device characteristics as functions of geometric design parameters and substrate material choice, three special R&D detector layouts were developed, called GEOM1, GEOM2 and GEOM3 (cf. Tables 1, 2). Detectors were single-sided, produced on n-type substrate, with p^+ strip and with a common n^+ implant on the backside to provide a good ohmic contact and a charge injection barrier.

The GEOM1 and GEOM2 detectors were produced on 4″ wafers and had a thickness of 300 μm. Detectors of the GEOM3 batch were produced on 6″ wafers with three different thicknesses: 320, 375 and 410 μm.

Within the 6.3×6.3 cm^2 fiducial surface of a 4″ wafer, 12 subdetector regions were defined, each having 32 p^+ strips, and independent bias and guard rings. The subdetectors are separated by n^+ implants. Four different pitches were implemented (60, 80, 120, and 240 μm) with three subdetectors for each pitch, thus allowing to study on the same device the effect of varying a second parameter.

In the case of GEOM1 devices the p^+ implant width was varied in the three subdetectors, but keeping the width of the metal strip 2 μm narrower than the p^+ implant in all the regions. In GEOM2 the effect of using metal strips wider than the implants, referred to as overmetal in the following,

Table 1
Design parameters of multi-geometry detectors of the GEOM1 and GEOM2 samples. All dimensions are in μm if not otherwise specified. The field oxide covers the region between the p^+ implants. Indicated tolerances in the wafer thickness come from the specifications provided by Hamamatsu Photonics [11]

GEOM1												
Thickness	⟨1 0 0⟩ 1 kΩ cm						320 ± 15 μm					
	⟨1 1 1⟩ 6 kΩ cm						320 ± 15 μm					
Thickness of SiO_2	⟨1 0 0⟩ 1 kΩ cm						5200 Å					
	⟨1 1 1⟩ 6 kΩ cm						6000 Å					
Pitch	60			80			120			240		
Width p^+	15	20	25	15	25	40	20	35	50	30	50	70
Width Al	13	18	23	13	23	38	18	33	48	28	48	68
w/p	0.25	0.34	0.42	0.19	0.31	0.50	0.17	0.29	0.42	0.13	0.21	0.29
GEOM2 shallow implant (1 μm)												
Thickness	⟨1 0 0⟩ 1 kΩ cm						290 ± 15 μm					
	⟨1 1 1⟩ 6 kΩ cm						295 ± 15 μm					
Thickness of SiO_2	⟨1 0 0⟩ 1 kΩ cm						6200 Å					
	⟨1 1 1⟩ 6 kΩ cm						5700 Å					
Pitch	60			80			120			240		
Width p^+	10	10	18	13	13	23	18	18	33	48	48	78
Width Al	10	18	26	13	21	31	18	26	41	48	56	86
w/p	0.17	0.17	0.30	0.16	0.16	0.29	0.15	0.15	0.28	0.20	0.20	0.33
GEOM2 deep implant (2 μm)												
Thickness	⟨1 0 0⟩ 1 kΩ cm						290 ± 15 μm					
	⟨1 1 1⟩ 6 kΩ cm						295 ± 15 μm					
Thickness of SiO_2	⟨1 0 0⟩ 1 kΩ cm						6200 Å					
	⟨1 1 1⟩ 6 kΩ cm						5700 Å					
Pitch	60			80			120			240		
Width p^+	12	12	20	15	15	25	20	20	35	50	50	80
Width Al	10	18	26	13	21	31	18	26	41	48	56	86
w/p	0.20	0.20	0.33	0.19	0.19	0.31	0.17	0.17	0.29	0.21	0.21	0.33

Table 2
Design parameters of multi-geometry detectors of the GEOM3 sample. All dimensions are in μm if not otherwise specified. The field oxide covers the region between the p^+ implants. Indicated tolerances in the wafer thickness come from the specifications provided by Hamamatsu Photonics [11]

GEOM3												
Thickness	⟨1 0 0⟩ 1 kΩ cm						320±15 μm					
	⟨1 0 0⟩ 6 kΩ cm						320±15 μm					
	⟨1 1 1⟩ 6 kΩ cm						320±15, 375±15, 410±15 μm					
Thickness of SiO_2	⟨1 0 0⟩ 1 kΩ cm						6200 Å					
	⟨1 0 0⟩ 6 kΩ cm						6200 Å					
	⟨1 1 1⟩ 1 kΩ cm						5700 Å					
Pitch	60			80			120			240		
Width p^+	9	12	18	12	16	24	18	24	36	36	48	72
Width Al	17	20	26	20	24	32	26	32	44	44	56	80
w/p	0.15	0.20	0.30	0.15	0.20	0.30	0.15	0.20	0.30	0.15	0.20	0.30

was studied. For each pitch two different regions were designed having the same w/p around 0.2, but in one case with the width of the aluminium strip chosen 6–8 μm wider than the width of the p^+ implant (i.e. 3–4 μm overmetal on each implant side). Moreover, for each pitch a region with the overmetal was designed with w/p around 0.3. Finally, in the case of GEOM3 detectors three values of w/p ratio were investigated (0.15, 0.20 and 0.30) with a constant overmetal of 8 μm (4 μm overmetal on each implant side).

Results reported in this paper refer to AC coupled devices. The AC coupling was implemented by separation of the metal strip and the implant by means of a multi-layer of silicon-oxide and silicon-nitride with thicknesses of 250 and 50 nm, respectively. The bias potential on the implants was supplied through 2 MΩ polysilicon resistors.

To study the possible effect of p^+ implant depth on detector characteristics, two different depths, referred to as deep implant (≈ 2 μm) and shallow implant (≈ 1 μm), were produced for GEOM2 detectors. The two detector sets were made with the same set of masks but by varying the temperature and the time of the diffusion process. The increased diffusion in the deep implant devices results in a strip width that is 2 μm wider than that of the shallow implant.

The behaviour after irradiation of detectors with different bulk parameters was investigated testing detectors with:

- two initially different substrate resistivities (low resistivity, around 1 kΩ cm, and high resistivity, around 6 kΩ cm) to investigate the consequences of irradiation on the depletion voltage;
- two different orientations of the plane along which the crystal was cut (⟨1 0 0⟩ and ⟨1 1 1⟩) to investigate the consequences of irradiation on the interstrip capacitance.

The GEOM1 and GEOM2 had either a ⟨1 1 1⟩ high resistivity substrate or a ⟨1 0 0⟩ low resistivity one. To factorize the effect of resistivity and crystal orientation an additional set of ⟨1 0 0⟩ high resistivity detectors was produced in the GEOM3 batch.

The detectors were fabricated by Hamamatsu Photonics [11]. All aspects of the processing were devised and optimized by Hamamatsu Photonics together with certain aspects of the design, in particular that of the guard ring structure.

3.2. Measurement set-up and procedure

The characterization of multigeometry detectors consisted of three basic measurements:

- leakage current drawn by a subdetector at a known temperature;

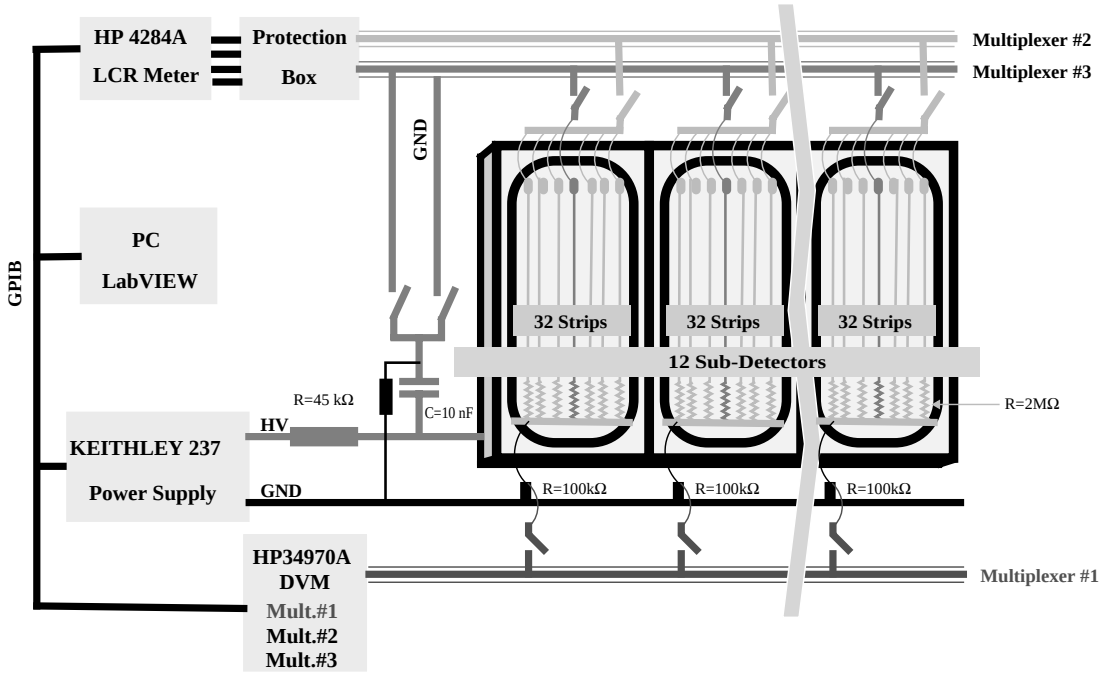

Fig. 2. Schematic view of the set-up for measurement of leakage current, interstrip capacitance and backplane capacitance on the multi-geometry detectors.

- capacitance of the strips on a subdetector to the backplane;
- capacitance of a strip to all its neighbours.

The measurement set-up used a multiplexed switch system and the strips on each subdetector were grouped into two sets, the central strip and the remaining 31 ones. This system allowed the full set of measurements to be performed for all the subdetectors at once.

The scheme used for the characterization of the detectors is shown in Fig. 2. It is based on an HP34970A switch mainframe housing three multiplexer boards HP34901A routing test signals to and from the device under test, an HP4284A LCR meter for capacitance measurements and a Keithley 237 high voltage source for the bias of the detectors.

One of the multiplexers is used to determine the leakage current for the different subdetectors from the measurement of the voltage drop across a 100 kΩ resistor and using the internal DVM in the switch unit. The other two multiplexers allow to make the connections necessary to measure backplane and interstrip capacitance. For each subdetector the interstrip capacitance was measured connecting the central strip to one of the inputs of the LCR meter and the remaining 31 strips to the other, with the backplane AC connected to ground through a 10 nF capacitor in order to suppress its influence on the measurement. The backplane capacitance was measured connecting the backplane to one input of the LCR meter and the 31 strips to the other. All instruments were connected to a PC via GPIB bus and controlled by a dedicated software written in NI LabVIEW program.

A multigeometry detector assembled for the characterization is shown in Fig. 3. To facilitate the handling, the detectors were fixed with silicone glue to carbon fibre or ceramic frames with readout strips facing up.[1] A large open window in the

[1] In the case of a carbon fibre frame the detector was insulated from the frame by a kapton foil.

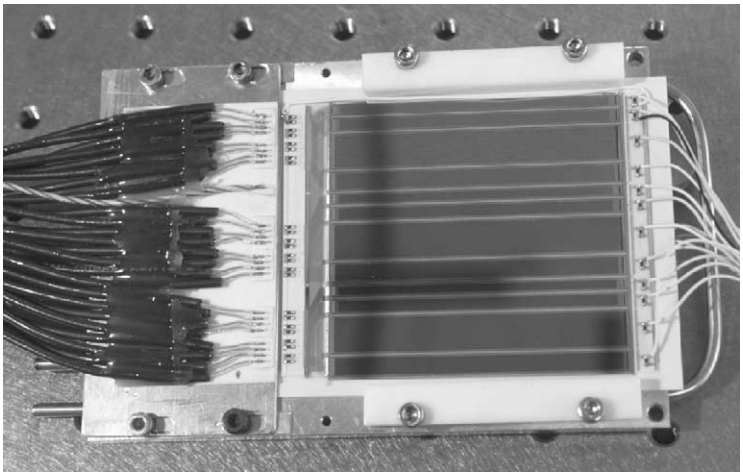

Fig. 3. A Hamamatsu multi-geometry detector assembled for characterization. From left to right: the leads to the input of the LCR meter, the measurement piece in ceramic carrying the 47 kΩ and 1 MΩ resistors, the glass pitch adaptor, the multi-geometry detector mounted on a ceramic frame and the ceramic piece with 100 kΩ resistors used for the measurement of the leakage current from the bias ring of their subdetector regions.

frame allowed access from the rear to the backplane. The bias voltage connection on the backplane was made with a wire glued with conductive epoxy. In addition, a 100 kΩ thermistor was glued to the backplane with silicone glue to monitor the temperature. The connection circuitry pieces needed for the measurement were glued on the upper face of the frame. Electrical connections among different pieces were provided by wire bondings. During the measurement the frame was mounted on an aluminium chuck both serving as mechanical support and providing the cooling to the detectors. This was especially necessary for the tests on irradiated detectors. More details on the measurement set-up can be found in Ref. [3].

On devices set at fixed bias voltage, we observed that the measured capacitances initially decreased with time before settling to a stable value. The effect was observed for both C_{int} and C_{back}, being one order of magnitude larger for the interstrip capacitance, both before and after irradiation, and for both $\langle 1\,1\,1 \rangle$ and $\langle 1\,0\,0 \rangle$ devices, being about twice larger in the former case. The time dependence could be described by the sum of two exponential components with time constants of about 1 h and 1 day, respectively. Therefore, measurements were performed starting from the highest bias voltage (typically 620 V) after waiting about 2 hours to reduce the effect below 10%. The bias voltage was then decreased in steps of 20 V measuring at each point the device temperature and, independently for each subdetector, the leakage current as well as the backplane and interstrip capacitance at four different frequencies: 5, 10, 100 kHz and 1 MHz, the maximum operating frequency of the LCR meter. Reference capacitors of 1.8, 10 and 150 pF, were also measured for all the four frequencies at each measurement point and these values were used to normalize the detector measurements. On the 10 pF reference capacitor, the typical value of the strip capacitance, the reproducibility of the measurement was found to be better than 0.2 pF.

The contribution of the pitch adaptor and of the measurement set-up pieces (cf. Fig. 3) to C_{int} and of the coupling capacitors to C_{back} were measured separately and subtracted in the offline analysis.

Capacitance measurements in semiconductor devices are sensitive to the frequency at which the measurements are performed [6].

Given the shaping time of the preamplifier [12], $\tau_{\text{shaping}} = 50$ ns, the maximum noise sensitivity is expected around $f = 1/2\pi\tau_{\text{shaping}} \approx 3$ MHz [13]. We take measurements at 1 MHz, the maximum

measurement frequency of the LCR meter, as a good representation of the effective capacitive load at the input of the read-out electronics.

In Section 5 the depletion voltage determined from the $1/C^2_{back}$ curves will be discussed. In this case the relevant frequency is determined by the mobility of the charge carriers in the bulk. Therefore, for the discussion of V_{dep}, measurements of backplane capacitances at 5 kHz frequency will be considered.

On irradiated detectors we found that C_{int} was reaching the asymptotic value at the highest measurement frequency, and that the measurement of C_{back} relevant for the determination of V_{dep} was still that done at the lowest frequency [3].

3.3. Irradiation facility

Detectors were irradiated at a facility developed and maintained at the CERN Proton Synchrotron (PS) jointly by the ATLAS and CMS collaborations using primary protons with a momentum of 24 GeV/c. The damage factor for this beam is 0.5 to 0.6, i.e. the equivalent 1 MeV-neutron fluence is about half the 24 GeV/c proton fluence.

Different irradiation cycles were performed with maximum fluence ranging from 3.1×10^{14}–4.3×10^{14} p/cm^2. During irradiation detectors were cooled to a temperature of about -5°C in an inert nitrogen atmosphere, with a bias voltage of about 150 V applied and with the aluminium strips kept at ground potential.

The particle fluence was continuously recorded using a secondary emission chamber upstream of the irradiation set-up. The absolute calibration was performed by the activation of aluminium foils inserted into the beam at the beginning of each irradiation cycle. The fluence received by the detectors was reasonably uniform throughout the detector surface, with the exception of the outer edges which were irradiated with only 70–80% of the nominal fluence.

After irradiation detectors followed an annealing cycle of 1 week at room temperature. This allowed for maximal beneficial annealing resulting in a minimum of the depletion voltage and a stable value of the leakage current. Apart from the annealing cycle, these detectors were kept below 0°C except for short periods, less than 12 h, when they were prepared for the measurement.

4. Qualitative overview of the measurements

An overview of the measurements of i_{leak}, normalized to the reference temperature of -5°C, C_{back} (5 kHz) and C_{int} (1 MHz) as a function of the bias voltage is shown in Fig. 4 for one detector subregion ($p = 80$ μm) of a high resistivity $\langle 1\,1\,1 \rangle$ and of a low resistivity $\langle 1\,0\,0 \rangle$ substrate from the GEOM1 batch. The curves are shown before and after the exposure to irradiation with 4.3×10^{14} p/cm^2.

4.1. Before irradiation

The interstrip capacitance is found to be similar for all the substrate types. The decrease of the backplane capacitance with voltage reflects the depletion of the bulk. According to Eq. (2) the depletion voltage scales with the square-root of the bias voltage, so that $1/C^2_{back}$ is expected to be a linear function of the bias voltage, reaching a plateau once full depletion is achieved. From the plots it can be seen that the depletion voltage for the high resistivity substrate is around 100 V, while in the low resistivity substrate full depletion is only reached at 300 V. At a bias voltage of 500 V the leakage current is below 0.1 nA/strip.

4.2. After irradiation

For both devices the leakage current has increased by more than 4 orders of magnitude. The depletion voltages determined from the backplane capacitance is about 300 V for the material with initial high resistivity while it is smaller, about 250 V, for that with initial low resistivity. For the $\langle 1\,1\,1 \rangle$ device, the value of C_{back} measured at 5 kHz is about 10% higher than before irradiation. While at 1 MHz the original value of C_{back} is recovered, it differs at lower frequency which can be attributed to a change in the mobility of the charge carriers. For $\langle 1\,0\,0 \rangle$ low resistivity, the interstrip capacitance saturates at a bias voltage below 100 V, and above 100 V the value of C_{int}

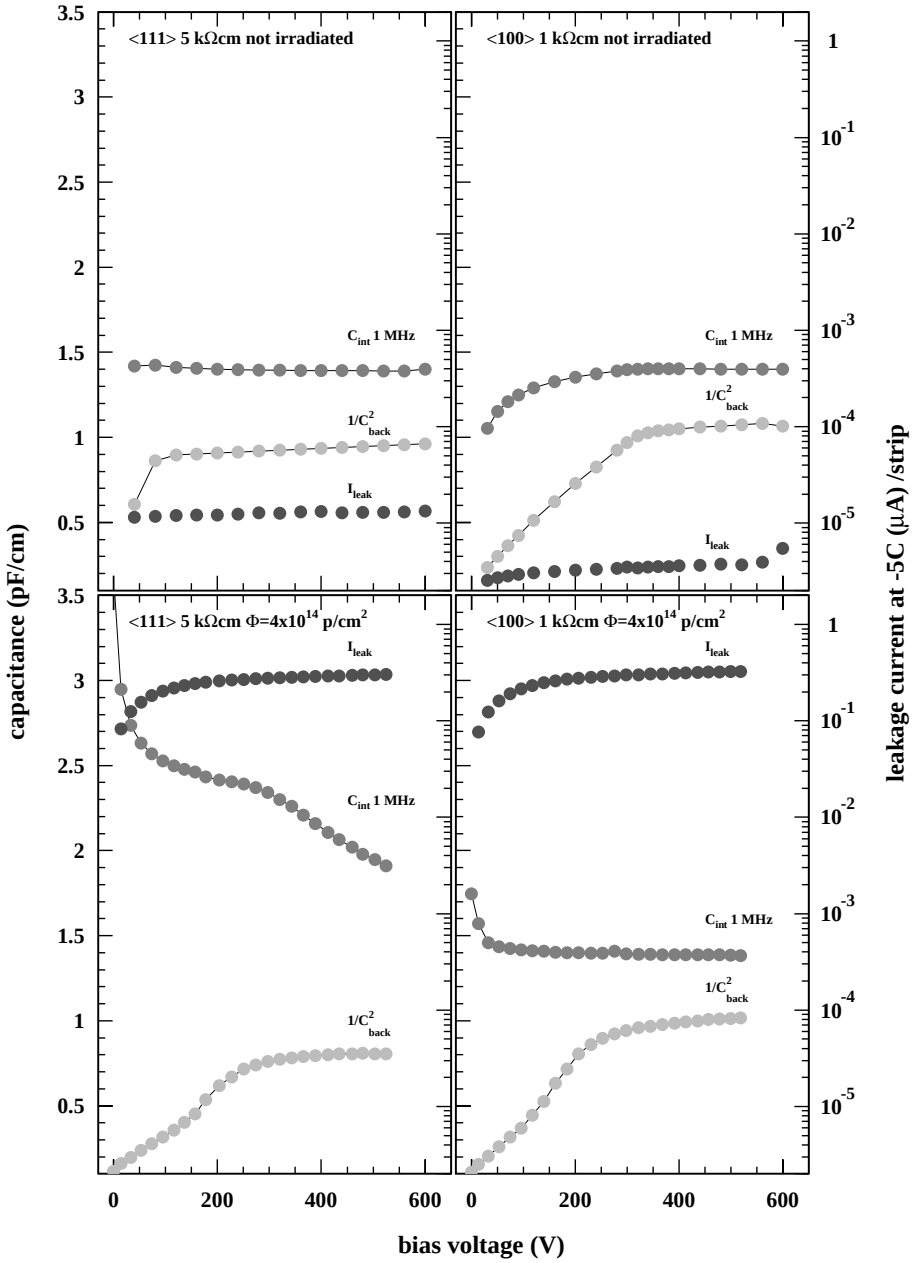

Fig. 4. Overview of the measurements in one of the subdetector regions ($p = 80$ μm, $w/p = 0.5$): non-irradiated high resistivity $\langle 1\,1\,1 \rangle$ (top left), non-irradiated low resistivity $\langle 1\,0\,0 \rangle$ (top right), irradiated high resistivity $\langle 1\,1\,1 \rangle$ (bottom left) and irradiated low resistivity $\langle 1\,0\,0 \rangle$ (bottom right). Measurements are shown as a function of the bias voltage. For each device are shown: interstrip capacitance (C_{int}) measured at 1 MHz, C_{back} measured at 5 kHz, $1/C^2_{\mathrm{back}}$ (arbitrary units in the plot) and i_{leak}. Measurements are calibrated using the appropriate values of the reference capacitances (10 pF for C_{int} and 150 pF for C_{back}) measured in the same characterization run.

recovers the value before the irradiation. No further decrease of C_{int} is observed with over-depletion. In the case of the $\langle 1\,1\,1 \rangle$ device we observe instead that C_{int}, after an initial drop, has a region of slow decrease up to the bias voltage at which the full depletion is reached. The value of C_{int} at full depletion is approximately doubled with respect to before irradiation. Beyond this point C_{int} decreases more rapidly with increasing over-depletion. This decrease, however, does not stop even at a bias voltage 200 V above the depletion voltage, where C_{int} still does not reach the value before irradiation. A similar, but more pronounced effect, is observed at lower measurement frequencies. We interpret this behaviour as being due to an increase in the charge of the electron accumulation layer below the oxide in-between strips, which is attracted by the fixed charges introduced in the oxide by irradiation. This electron layer can be repelled by the increasing negative potential on the strips, which decreases the interstrip capacitance.

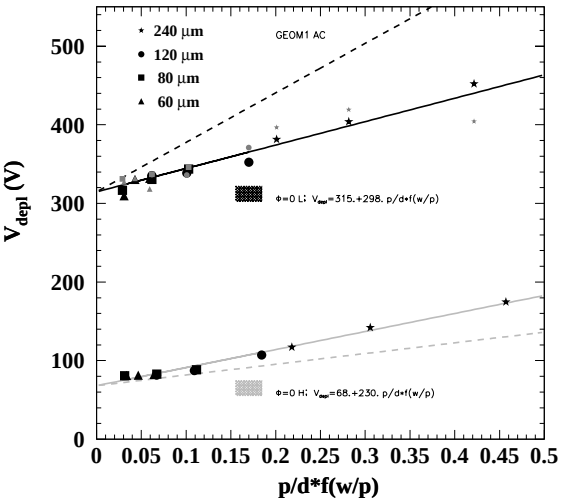

Fig. 5. Depletion voltage for non-irradiated GEOM1 detectors as a function of the geometrical parameter of Eq. (4): The solid lines represent the linear fit of V_{dep} as a function of the abscissa $p/df(w/p)$. The dashed lines are the predictions from Eq. (4) using for $V_{dep,diode}$ the intercept from the fit and the value 2 for the slope-to-intercept ratio. Results for the high resistivity detectors are shown in the lower part of the plot while those for the low resistivity ones in the upper part.

5. Depletion voltage

The dependence of the depletion voltage on the geometrical parameters, predicted for a segmented junction by Eq. (4), was tested on high and low resistivity detectors before and after irradiation. $1/C^2_{back}$ was plotted as a function of the bias voltage where the backplane capacitance was measured at 5 kHz. The point of inflection between the low voltage region and the high voltage asymptotic region was taken as the depletion voltage.

The results for the non-irradiated GEOM1 detectors are shown in Fig. 5. The dependence of V_{dep} on the geometrical correction factor $p/df(w/p)$ of Eq. (4) was found to be linear, but the observed slopes differ from the expectation both for low and high resistivity devices. In particular, we found a value for the slope-to-intercept ratio which differs significantly from the predicted one of 2. Moreover, the measured value for the slope-to-intercept ratio was found to vary significantly for the different samples.

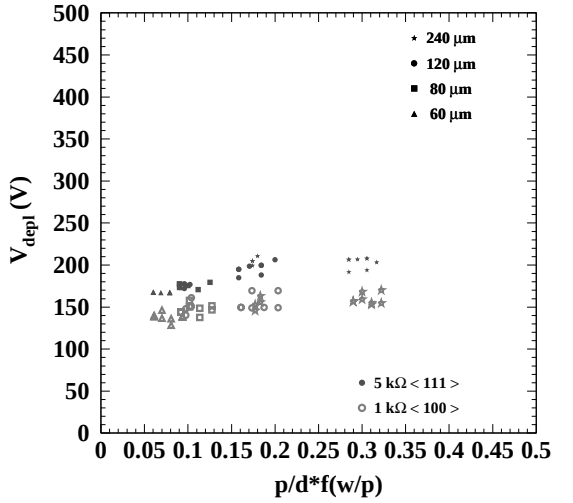

Fig. 6. Depletion voltage for GEOM2 AC detectors exposed to 3×10^{14} 24 GeV/c protons/cm^2 as a function of the geometrical parameter of Eq. (4). All detectors followed an annealing cycle at room temperature for 1 week.

The results for the GEOM2 detectors exposed to 3.1×10^{14} p/cm^2 are shown in Fig. 6. All the detectors followed an annealing cycle of 1 week

at room temperature. The correlation between the geometrical parameter $p/df(w/p)$ and V_{dep} is reduced. After type inversion the depletion voltage of the detectors of initially high resistivity is systematically larger than that of detectors of initially low resistivity.

6. Capacitances

The capacitance values discussed in this section refer to the measurements made at a bias voltage of 500 V, i.e. with the detector fully depleted both before and after irradiation, and at a frequency of 1 MHz, the one relevant for the noise figure.

In order to provide a unique parametrization for both regions without and with overmetal, for the latter an effective strip width was introduced. We found that 6 μm overmetal corresponded to an effective increase of 2.6 μm in the implant width.

We did not observe any relevant difference between the two sets of detectors with different depths of the p^+ implant.

6.1. Dependence on geometrical parameters

The measured backplane capacitance per unit length as a function of the geometrical parameter of Eq. (5) is shown in Fig. 7 for $\langle 1\,0\,0 \rangle$ low resistivity GEOM2 detectors. We found that the functional dependence of C_{back} on the geometrical parameters is in agreement with the expectation after introducing the function $f(w/p)$ of Eq. (6). In contrast to the prediction of Eq. (5) we observed a smaller value for the slope ($\varepsilon_0\varepsilon_{Si} = 1.05$ pF/cm) and a non-zero value for the offset. The measured C_{back} decreased with decreasing measurement frequencies leading to smaller values of both the offset and the slope. However, at the lowest measurement frequency of 5 kHz the offset was still 0.05 pF/cm, significantly different from zero. Similar results were also found for the other samples with substrates having different resistivities and orientations of the crystal lattice. The difference from the expectations could not be accounted for by the uncertainty on the wafer thickness alone, indicated in Tables 1 and 2.

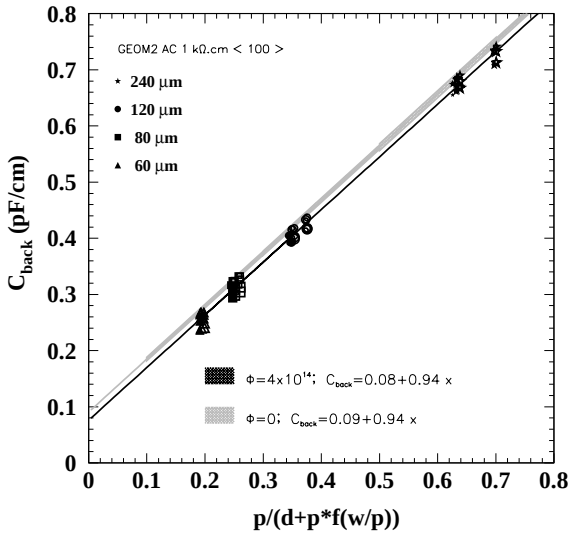

Fig. 7. Backplane capacitance per unit length, plotted as a function of the geometrical parameters of Eq. (5), for GEOM2 $\langle 1\,0\,0 \rangle$ low resistivity detectors measured at $V_{bias} = 500$ V and 1 MHz frequency before and after the exposure to irradiation. Linear fits to the data before irradiation are shown as a grey line, the width of the line indicating one standard deviation around the best fit. Points represent measurements after irradiation.

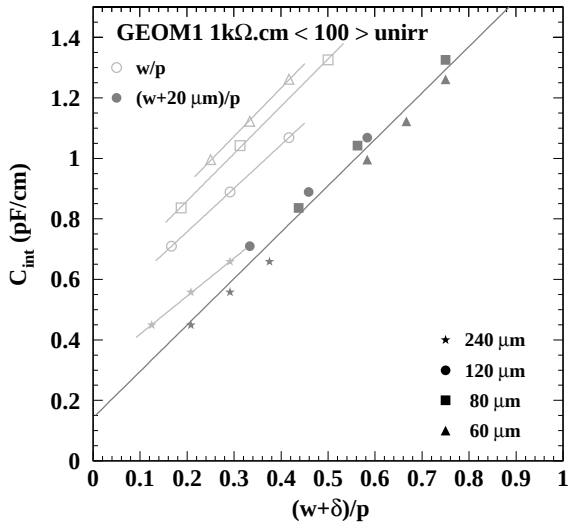

Fig. 8. Interstrip capacitance, plotted as a function of w/p ratio (light symbols) and as a function of $(w + 20\ \mu m)/p$ (dark symbols). The short lines in the upper left part of the figure connect regions of the same pitch.

The measured interstrip capacitance per unit length as a function of the w/p ratio is shown in Fig. 8 for a $\langle 1\,0\,0 \rangle$ low resistivity GEOM2 detector. We observed that when plotted against the w/p parameter, the interstrip capacitance of different regions with the same pitch were lying on straight lines with similar slope but different offsets. For a fixed value of w/p the interstrip capacitance decreased approximately linearly for increasing pitches, thus ruling out the infinite wafer thickness approximation of Eq. (7) already for pitches of 120 μm. On the other hand, the interstrip capacitances of regions of different pitches fell on the same straight line when they were expressed as a function of the variable $(w + 20\ \mu\text{m})/p$:

$$C_{\text{int}} = \left(0.1 + 1.5\,\frac{w + 20\ \mu\text{m}}{p}\right)\ \text{pF/cm}. \tag{10}$$

The parametrization found for the interstrip capacitance can be compared with the prediction obtained by subtracting the backplane capacitance, Eq. (5), from the total capacitance, Eq. (8):

$$C_{\text{int}} \approx \left(0.8 + 1.6\,\frac{w}{p} - 1.05\frac{p/d}{1 + (p/d)f(w/p)}\right)\text{pF/cm} \tag{11}$$

valid in the range $0.10 < w/p < 0.55$. This expression depends both on w/p and p and is rather complicated. It turns out that for $d = 300\ \mu\text{m}$, $0.18 < w/p < 0.36$ and $50\ \mu\text{m} < p < 200\ \mu\text{m}$ the following formula approximates Eq. (11) above to better than 10%:

$$C_{\text{int}} \approx \left(0.1 + 1.6\,\frac{w + 20\ \mu\text{m}}{p}\right)\ \text{pF/cm} \tag{12}$$

in excellent agreement with the result of Eq. (10).

The interplay between C_{int} and C_{back} is shown in Fig. 9. It shows the breakdown of interstrip and backplane capacitance contributions to the total capacitance in regions with the same value of $w/p = 0.15$ but with different pitches (60, 80, 120 and 240 μm) and in devices with three different thicknesses 320, 375 and 410 μm. It can be seen that the decrease of C_{int} is almost exactly compensated by the increase of C_{back} thus confirming the expectations of Section 2.3 that the total strip capacitance, the parameter relevant for the electronic noise figures, is a function only of the strip width-to-pitch ratio. Similar compensation was observed in the devices of GEOM1 and GEOM2 with a fixed wafer thickness but a larger range of w/p values. For the geometrical parameters investigated ($0.2 < p/d < 0.8$ and $0.1 < w/p < 0.5$) the total capacitance could be expressed linearly as a function of w/p with the following parametrization:

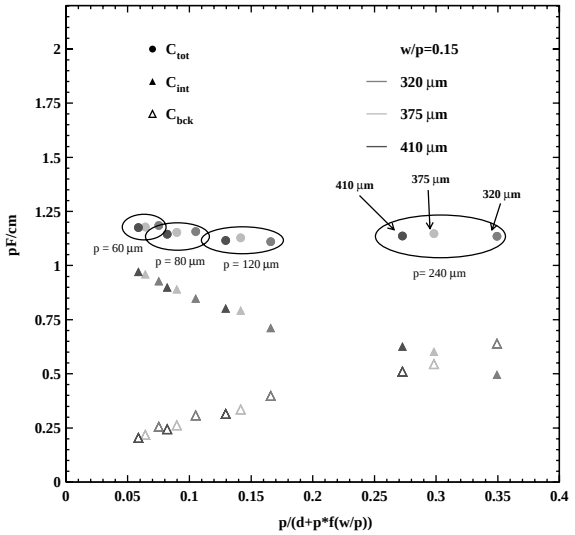

Fig. 9. Contributions to the total capacitance per unit length from backplane and interstrip capacitances for non-irradiated $\langle 1\,1\,1 \rangle$ high resistivity detectors of the three different thicknesses in the case of $w/p = 0.15$. The capacitances are plotted versus the factor from Eq. (5) which expresses the dependence of the backplane capacitance on the geometrical parameters.

$$C_{\text{tot}} = \left(0.8 + 1.7\frac{w}{p}\right)\ \text{pF/cm} \tag{13}$$

with the spread of the data points around the parametrization being about 0.05 pF/cm.

The measurements of C_{tot} against w/p for the three different thicknesses of GEOM3 detectors are shown in Fig. 10. The total capacitance is found to be linear with respect to w/p and independent both of the pitch and of the thickness of the detector.

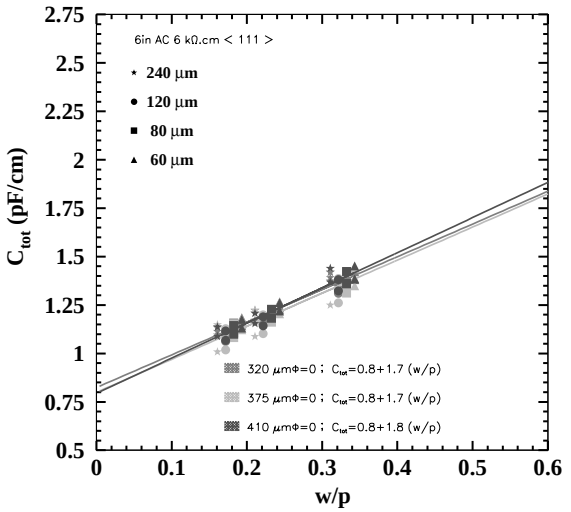

Fig. 10. Total capacitances per unit length measured at $V_{bias} =$ 500 V and 1 MHz frequency.

6.2. Effect of irradiation

As can be seen in Fig. 7, C_{back} is not affected by the exposure to irradiation. Therefore, changes in the total capacitance are determined by the behaviour of C_{int}.

Fig. 11 shows the interstrip capacitance per unit length measured on detectors with different combinations of initial resistivity and crystal orientation before and after the exposure to irradiation. Samples produced on both 4″ and 6″ wafers were measured. We found that in the case of devices with $\langle 1\,0\,0 \rangle$ crystal orientation C_{int} is not affected by the exposure to irradiation. On the other hand, in the case of $\langle 1\,1\,1 \rangle$ crystal orientation, the 4″ devices showed a significant increase in the interstrip capacitance bigger than 0.1 pF/cm while for detectors produced on 6″ wafer the discrepancy between the values before and after the irradiation was smaller. Moreover, the size of the effect differs among the various prototype batches.

The analysis of the voltage dependence of C_{int}, cf. Fig. 4, showed that in the case of devices with $\langle 1\,1\,1 \rangle$ crystal orientation, the interstrip capacitance does not reach a plateau value even at the highest bias voltage (600 V) while in the case of $\langle 1\,0\,0 \rangle$ devices the asymptotic value is reached within the first 50 V.

7. High voltage performance

We define breakdown as the departure from the normal I–V curve of a pn junction shown by an increase of the leakage current beyond the depletion voltage. Among the most critical regions where breakdown can originate are the guard ring and the strips. The geometry of the strip design could influence the high voltage stability, in particular the choice of the relative dimensions of the p^+ implant and of the read-out metal strip. In fact breakdown phenomena start at the edges of the implants where the electric field lines accumulate. Metal strip wider than the implant moves the critical point of maximum field from the bulk to the oxide region where the breakdown field strength is one order of magnitude larger than in the silicon [10].

Sensitivity of the measurement of breakdown originating in strips can be increased by exploiting the correlation between the behaviour of the second derivative of i_{leak} with respect to the voltage and the departure from the pn junction behaviour of the backplane capacitance [3].

Measurements of V_{bdwn}, the bias voltage at which the breakdown occurs, based on this behaviour of C_{back} are shown in Figs. 12 and 13 for the irradiated detectors. The GEOM2 devices allowed the comparison between regions with and without overmetal as both were present on the same device. All the regions with no overmetal showed breakdown below 550 V while the others were still stable at 600 V, the maximum bias voltage in the measurement procedure. In the regions without overmetal, detectors with deep implant showed better breakdown performances than those with shallow implant while no significant differences are observed in the regions with overmetal.

The GEOM3 devices, all of which have overmetal, allowed the comparison among regions with the same value of w/p but with different pitches. The effect of the overmetal is again beneficial but

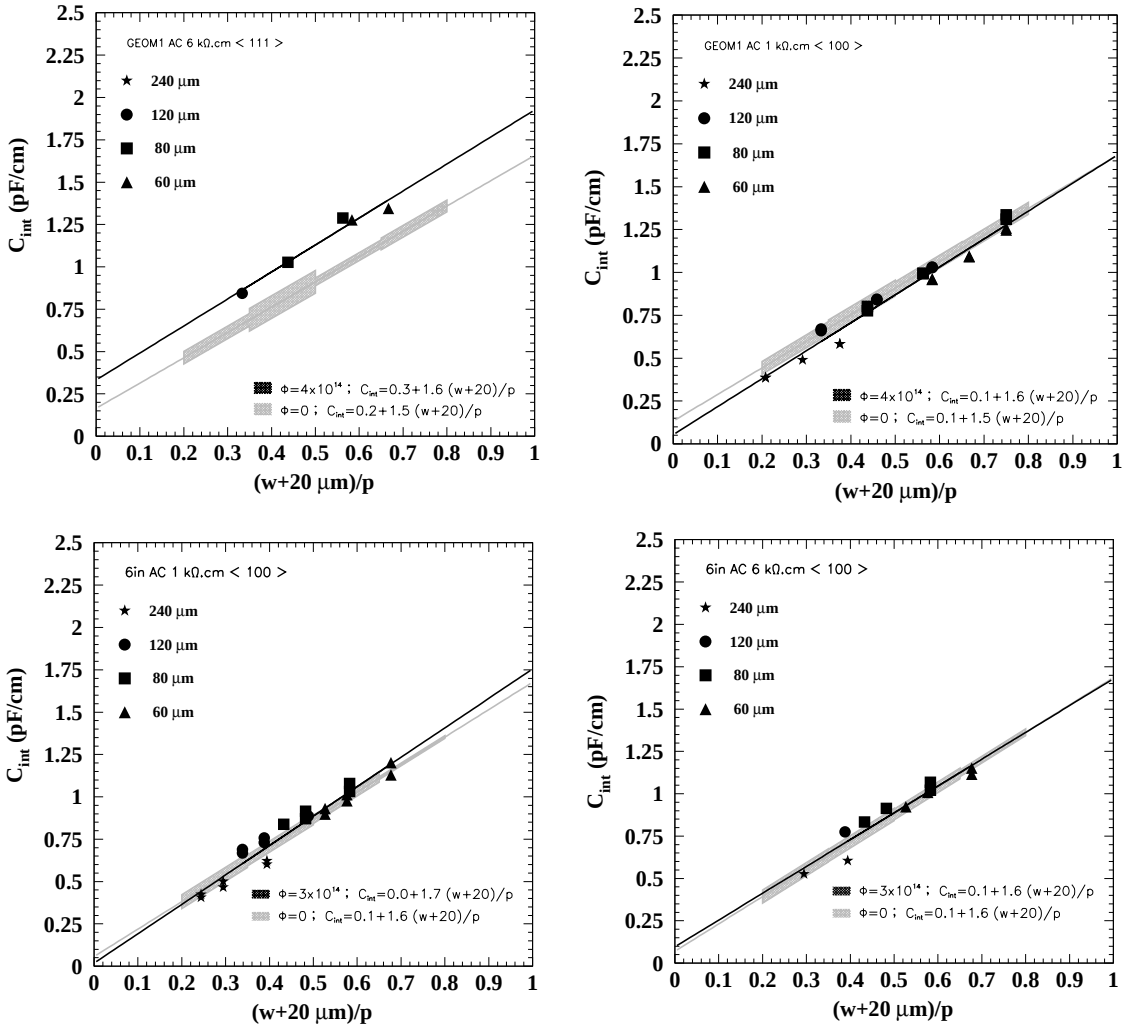

Fig. 11. Interstrip capacitance per unit length for detectors measured at $V_{bias} = 500$ V and 1 MHz frequency before and after the exposure to irradiation: GEOM1 $\langle 1\,1\,1 \rangle$ high resistivity (upper left), GEOM1 $\langle 1\,0\,0 \rangle$ low resistivity (upper right), 6″ $\langle 1\,0\,0 \rangle$ low resistivity (lower left) and 6″ $\langle 1\,0\,0 \rangle$ high resistivity (lower right). The shaded area represents the 1 standard deviation region around the best line fit of measurements before irradiation. Points represent measurements after irradiation.

the regions with 240 μm pitch showed breakdown at about 550 V for $w/p \leqslant 0.2$.

8. Implications on the detector design for the CMS silicon tracker

The results on depletion voltage, capacitance and high voltage behaviour shown in the previous sections allow to optimize the sensor design in order to maximize the signal-to-noise performance of a silicon microstrip detector to be used in an LHC experiment.

In the case of the silicon tracker for the CMS experiment, a large volume can be instrumented with a reasonable number of read-out channels, adopting a scheme where the strip length and read-out pitch both increase with the radial distance

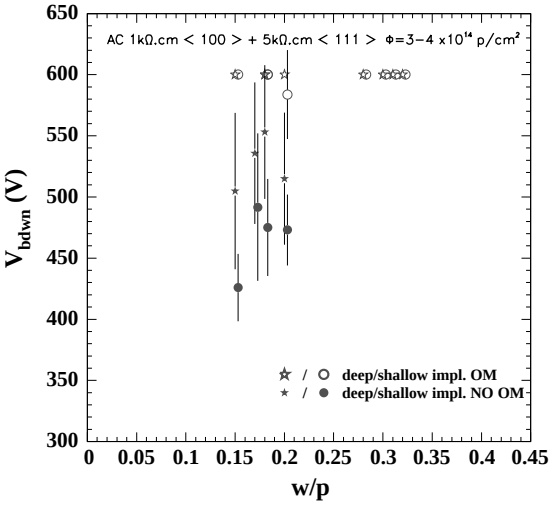

Fig. 12. Breakdown voltages as a function of the w/p ratio, for irradiated GEOM2 detectors (7 high resistivity $\langle 1\,1\,1 \rangle$ and 6 low resistivity $\langle 1\,0\,0 \rangle$ devices), with 320 μm thick substrate. Regions without (full symbols) and with (open symbols) overmetal were present. Results are shown separately for deep and shallow implant detectors. The error bars represent 1 standard deviation spread of the values around the average. Each data point combines the measurements over the range 60–240 μm over a given value of w/p. For the shallow implant detectors the values of w/p were slightly shifted to avoid overlap in the plot.

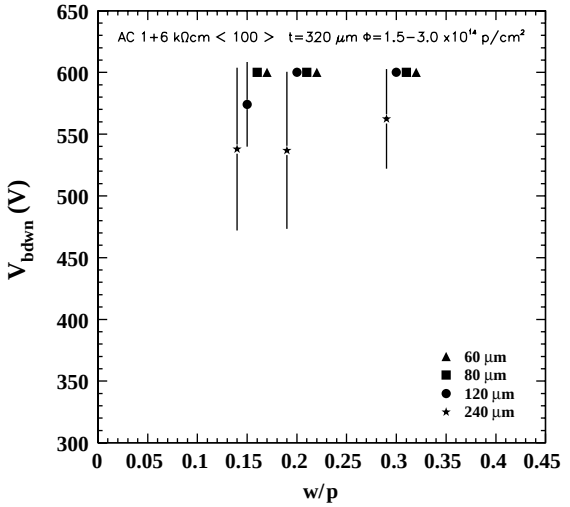

Fig. 13. Breakdown voltages as a function of the w/p ratio for GEOM3 irradiated detectors (4 high resistivity and 4 low resistivity devices all with $\langle 1\,0\,0 \rangle$ crystal orientation) with 320 μm thick substrate. All the regions had overmetal. The error bars represent 1 standard deviation spread of the values around the average. The four pitches are shown separately. The true values of w/p are 0.15, 0.20 and 0.30 for all the pitches. In the plot the points have been slightly shifted to avoid overlap.

from the beam, so as to maintain a constant granularity of the solid angle coverage.

To match the fast response of the silicon detector, channels will be read-out by the APV25 chip [12] ($\tau_{\text{shaping}} = 50$ ns) designed to operate in two sampling modes: peak mode and deconvolution mode.

The signal level is determined as the product of the charge produced by the minimum ionizing particles crossing the detector, about 3.8 fC in a 300 μm thick silicon detector, the efficiency of collecting this charge at the strip implant, which will be assumed to be equal to 100% before and 85% after irradiation (detectors operating in overdepletion mode), and the efficiency Q of collecting the charge through the coupling capacitor:

$$Q = \frac{C_{\text{AC}}}{C_{\text{AC}} + C_{\text{tot}}}.$$

For the detectors considered in this study, the coupling capacitance C_{AC} determined by the specification sheets is

$$C_{\text{AC}} \simeq 1.3w \ (\mu\text{m}) \ \text{pF/cm}.$$

The contributions to the noise from the capacitive load to the preamplifier, expressed in terms of Equivalent Noise Charge (ENC), for the APV25 are [12]:

$$\text{ENC} = 246 + 36C_{\text{tot}} \ (\text{pF}) \ \text{peak mode}$$
$$\text{ENC} = 396 + 59C_{\text{tot}} \ (\text{pF}) \ \text{deconvolution mode}.$$

The other main contribution comes from leakage current parallel noise [14]:

$$\text{ENC} = 107\sqrt{i_{\text{leak}}\tau_{\text{shaping}}(\mu\text{A ns})} \ \text{peak mode}$$

$$\text{ENC} = 107\sqrt{i_{\text{leak}}\tau_{\text{shaping}}(\mu\text{A ns})} \times 0.45 \ \text{deconvolution mode}.$$

Finally, a noise contribution of $600e$ has been included due to the analogue optical link used in the read-out chain [15].

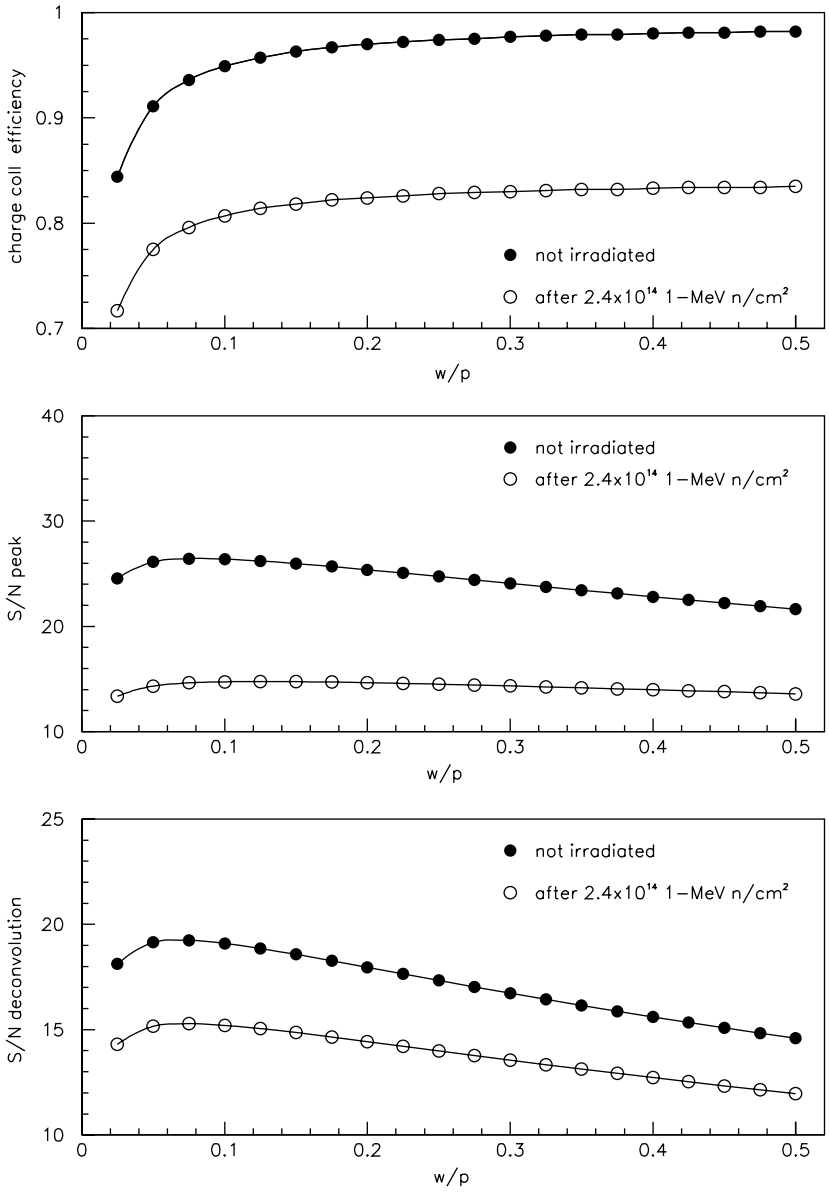

Fig. 14. Predicted charge collection efficiency (top), signal-to-noise ratio in peak (centre) and deconvolution (bottom) mode, as a function of the w/p ratio for a detector with 140 μm pitch, 300 μm thickness and 12 cm long strip. The filled symbols are the predictions for the non-irradiated detectors while the open symbols represent the predictions after an absorbed dose equivalent to 2.4×10^{14} 1 MeV-neutron/cm^2.

The predicted values of Q and of the signal-to-noise ratio for the two operation modes of the APV25 chip are shown in Fig. 14 for a realistic detector design with 12 cm long strips, a read-out pitch $p = 140$ μm and a thickness $d = 300$ μm. Predictions are shown as a function of the w/p ratio both for non-irradiated detectors and after an absorbed fluence of 2.4×10^{14}

1 MeV-neutron/cm^2, which corresponds to 1.5 of the expected maximum absorbed fluence inside the tracker volume. The total capacitance was computed according to Eq. (13). The curves after irradiation are relevant only for devices with $\langle 1\,0\,0 \rangle$ crystal orientation for which the parametrization holds before as well as after irradiation. For irradiated detectors the contribution of the leakage current parallel noise was computed assuming a substrate temperature during operation of -10°C and using Eq. (9) for the leakage current. For a given pitch, the lower the width the lower is the noise figure, while the charge collection efficiency through the coupling capacitor decreases for decreasing strip width. The maximum in the signal-to-noise ratio is reached at about $w/p = 0.06$. On the other hand, such a small value of w/p is not desirable for what concerns the stability at high voltage. The loss in the signal-to-noise ratio for a choice of detector geometry with $w/p = 0.25$ is less than 15% compared to the maximum. If the shot noise is negligible, i.e. before irradiation, the signal-to-noise curves obtained for detectors of different thicknesses just scale vertically since C_{tot} depends only on w/p.

The above results are reflected in the following choices for the detectors for the CMS silicon tracker:

- a substrate with $\langle 1\,0\,0 \rangle$ crystal orientation to guarantee that the interstrip capacitance is not increased by irradiation;
- two different initial substrate resistivities, about 1 kΩ cm for the sensors to be used where the expected fluence is higher and about 5 kΩ cm for those where the expected fluence is lower, to be able to achieve sufficient signal-to-noise ratio with a bias voltage not exceeding 400 V, during the entire LHC lifetime;
- a range of strip pitches of 80–200 μm with a constant value of w/p around 0.25 to optimize the signal-to-noise performance, while maintaining good high voltage stability;
- two different substrate thicknesses, 320 μm for the sensors used in the shorter inner modules and 500 μm for the larger outer ones, but with the same w/p. This allows to compensate with a higher signal, owing to the increased charge collected in the thicker detectors, the increase in the noise, due to the longer strips;
- a metal strip wider than the implant to improve the stability of the detectors at high voltage.

9. Conclusions

Results of an R&D activity to develop radiation hard silicon microstrip detectors for the CMS Tracker have been presented. We found that the total strip capacitance per unit length is a function of the width-to-pitch ratio w/p only, i.e. for a fixed value of w/p it depends neither on the thickness nor on the pitch. Therefore, the noise due to the capacitive load to the read-out electronics, which increases linearly with the strip length, can be compensated with the larger signal collected in thicker detectors, while the total strip capacitance per unit length is kept constant as it depends on the w/p ratio only. This allows to instrument a larger volume with a limited number of channels using longer strips, a larger pitch and thicker detectors. The use of a metal read-out strip wider than the implant ensures stability to the highest voltage (400 V) required for an efficient charge collection after irradiation. Finally, the choice of $\langle 1\,0\,0 \rangle$ crystal orientation for bulk guarantees the stability of interstrip capacitance after the exposure to irradiation. These results represent the baseline for the choice of the silicon sensors for the CMS Tracker.

References

[1] CMS Collaboration, The Tracker Project Technical Design Report, CERN/LHCC 98-6, 1998;
CMS Collaboration, Addendum to the CMS Tracker TDR, CERN/LHCC 2000-16, 2000.
[2] E. Gatti, P.F. Manfredi, La Rivista del Nuovo Cimento 9 (1986) 1;
V. Radeka, Ann. Rev. Nucl. Part. Sci. 38 (1988) 217.
[3] S. Braibant et al., CMS Note 2000/011, 2000.
[4] E. Barberis, et al., Nucl. Instr. and Meth. A 342 (1994) 90.
[5] D. Husson, IEEE Trans. Nucl. Sci. 41 (4) (1994) 811.
[6] R. Sonnenblick, et al., Nucl. Instr. and Meth. A 310 (1991) 189.

[7] RD48 Status Report, CERN/LHCC 2000-009, December 1999.
[8] A. Chilingarov, et al., Nucl. Instr. and Meth. A 360 (1995) 432.
[9] L. Adam, A. Holmes-Siedle, Handbook of Radiation Effects, Oxford University Press, Oxford, 1994.
[10] S.M. Sze, Physics of Semiconductor Devices, Wiley, 2nd Edition, 1981.
[11] Hamamatsu Photonics Co., Hamamatsu 435, Japan.
[12] L.L. Jones et al., in: Proceedings of the Fifth Workshop on Electronics for LHC Experiments, CERN/LHCC 99-33, 1999, p. 162.
[13] E. Nygård, et al., Nucl. Instr. and Meth. A 301 (1991) 506.
[14] S. Gadomski, et al., Nucl. Instr. and Meth. A 320 (1992) 217.
[15] F. Vasey et al., in: Proceedings of the Sixth Workshop on Electronics for LHC Experiments, CERN/LHCC/2000-041, 2000, p. 289.