SiLC R&D: design, present status and perspectives

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representing SiLC collaboration

Introduction

Over the last decade the feasibility and the potential of an electron positron linear collider with a centre of mass energy between a few hundred GeV and a TeV has been studied intensely. A consensus has emerged in the community of particle physicists that a high-luminosity high-energy electron–positron collider (now known as ILC - International Linear Collider) is an essential step on the road of understanding the standard model of particle physics and its limitations.

Detector Design for the ILC

The enormous statistical power of the ILC machine and the favourable background conditions should be matched by a precision detector which is capable of taking collision data with the least possible introduction of biases and systematic errors. Given the relatively low interaction rates, it will be possible to construct a data acquisition system without any hardware trigger. The required resolutions to achieve the statistically possible resolution are challenging for most of the subsystems. In particular the reconstruction of hadronic final states requires an unprecedented jet energy resolution. In order to achieve this goal, the **particle flow concept** has been chosen by most studied detector designs.

This concept is guided by the idea that the optimal jet energy resolution is achieved if all particles originating from the primary e^+e^- collision are fully reconstructed individually.

Currently several overall detector concepts are studied. The main differences are in the choices for charged particle tracking and in the magnetic field and inner radius of the electromagnetic calorimeter. The SiD concept employs a 5 T magnetic field and an all-silicon tracking system. The LDC concept has a 4 T field and relies on a large time projection chamber (TPC) supplemented by few layers of silicon detectors for tracking. In the GLD concept a 3 T magnetic field is compensated by an even larger calorimeter radius. While both in SiD and LDC a Silicon-Tungsten electromagnetic calorimeter (ECAL) with 1 cm^2 cells is foreseen, GLD relies on a Scintillator-Tungsten ECAL with crossed 14 cm^2 Sc-Tiles. Recently 4^{th} concept was presented differing namely in calorimetry and muon system.

R&D on the crucial detector components has started in a world-wide effort. In most cases the R&D on the sub-detectors is independent of the specific detector design concept in which it would be implemented.

High precision **vertex detectors** are mandatory at the ILC for the tagging of bottom and charm hadron as well as measuring the impact parameters of tau lepton decays products. There is a general consensus that a four to five layered fine-grained ($<20\times20$ μm^2) silicon pixel detector will be used.

In the context of the particle flow concept, the requirements for **charged particle tracking** are mainly high efficiency, robustness, and good double track resolution. Here momentum resolution is less important. However for some important physics channels very high momentum resolution ($\sigma\ (1/p_t\ ) = 5\times10^{-5}$ GeV^{-1}) has to be achieved, approximately a factor five better than achieved at LEP. Two complementary approaches to achieve this are pursued: Silicon strip detectors which give a small (5) number of very precise (few micrometers) space points or a huge Time Projection Chamber with at least 200 space points of moderate (< 100μm) point resolution. In the case of Silicon tracking the major challenges are to achieve the desired point resolution with a minimum of material to reduce multiple scattering and photon conversions.

The calorimetry will consist of a fine-grained electro-magnetic and hadronic sampling calorimeter optimized for particle flow analysis.

Silicon Tracking

The existing detector concepts for the ILC detector differ to a certain extent in design of the tracker. The SiD concept intends to use purely silicon as a sensor technology for most subdetector systems. The other 3 concepts propose to use gaseous tracker (TPC) enveloped by silicon sensors in the forward region (FCH), in front (SIT) and behind (SET) the TPC.
Silicon layers surrounding a TPC could provide for improved momentum resolution, improved interfacing to the calorimeter and vertex detector, and act as a robust fiducial for the calibration of the gaseous TPC tracker (see Fig. 1). On the other hand, current all-silicon tracking designs are expected to exhibit a precision fully competitive with that of gaseous tracking options, while offering the potential for a substantial savings in material (particularly in the forward direction), a more straightforward calibration procedure, and greater resistance to backgrounds and aging.

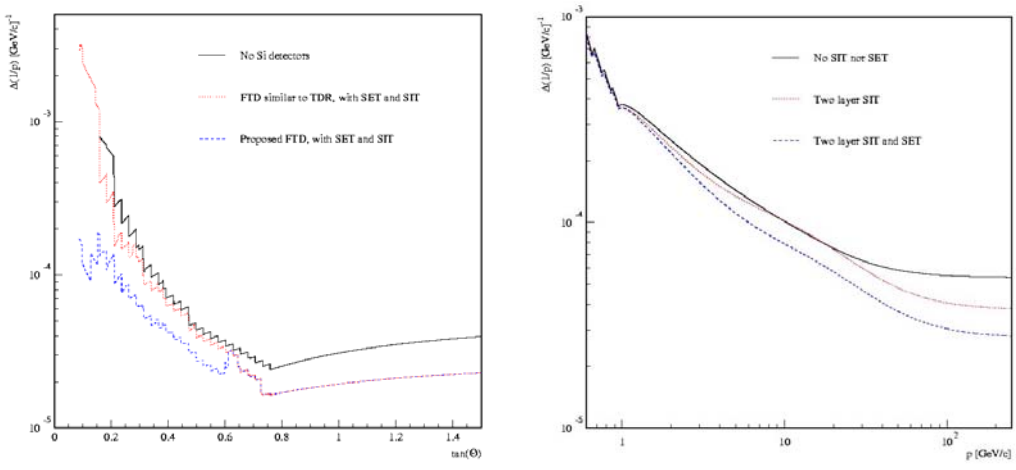

Fig. 1 Effect of supplementary silicon tracking on the momentum resolution as a function of angle (left) and momentum (right)

The development of the silicon tracking idea has been the main objective of **SiLC collaboration** [1]. Here institutes from 3 continents (America, Europe and Asia) collaborate in preparing detailed proposal of silicon technology used in a tracker.
The current concept of a silicon tracker utilizes state-of-the-art technologies in all

aspects of the design.

Sensors

SiLC assumes usage of long ladders consisting of strip sensors made out of 8 inch wafers). Thickness of sensors planned for ILC is a matter of studies, and minimal value allowing for reasonable S/N ratio will be chosen in order to minimise the amount of material added. However, new pixel technology might be of interest in particular for the second layer near the vertex detector in the central inner part.
Currently similar sensors fabricated for Glast and CMS are being used for module building. Design and production of dedicated SiLC sensors is planned for 2007.

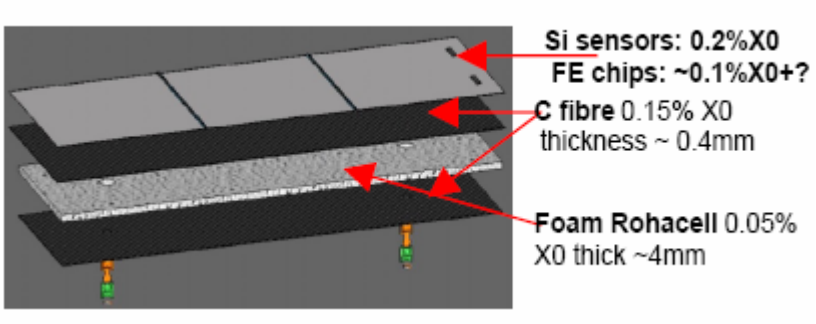

Fig. 2: Construction of prototype modules

Electronics

The readout electronic system should not degrade significantly the intrinsic detector performance within the environment of the ILC detectors, matching therefore several constraints: comply the duty cycle of the ILC machine, ensure an electronics MIP to noise ratio of 25 at 3 µs shaping time, provide a continuous stream of lossless compressed digital data at the end of each bunch train. At the same time the electronics should dissipate a total average power under 15 Watts, minimize the on-detector total material regarding transparency to radiation and ensure the reliability of the whole system.
The general architecture of the front end chip is based on a low noise preamplifier, a pulse shaper, a zero suppression decision, a sampling analogue pipe-line, an analogue to digital converter, a digital buffer, an internal calibration, and a power switching circuitry for power cycling.
The front-end architecture is shown in Fig. 3. Two ranges of shaping times are implemented, namely a “slow” shaping time between from 500 ns and a few µs, and a “fast” shaping time focusing on a few tenths of ns, in order to obtain a rough measurement of the z coordinate along the beam axis. This fast shaping time could also be used to provide a fine BCO tagging in case of high occupancy in some regions.

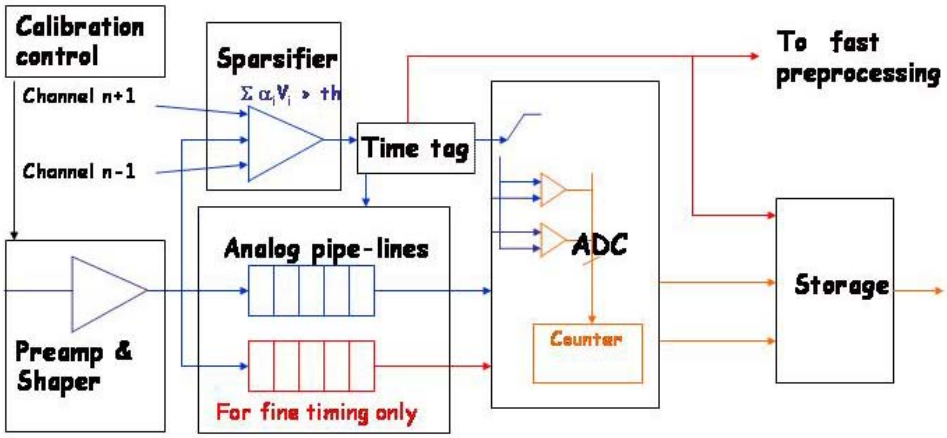

Fig. 3: Front End Architecture

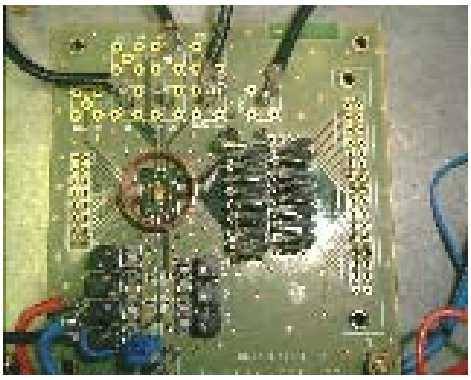

Fig. 4: Chip on Board test card for the CMOS 180 nm prototype

As first results of the SiLC R&D program, a test chip in 180 nm CMOS technology has been designed and tested (see Fig. 4). Results have been encouraging concerning the main specifications such as noise and power. It confirms that a power dissipation below 1 mW/channel for the system from the preamplifier to the end of the front-end chain describes above is achievable. The development on 130nm technology is ongoing.

Mechanics and alignment

The aims of the R&D on mechanics are low material budget, easiness of construction (simple modular structure, transfer to industry), robustness, low cost and easy integration issues. Various geometry options are under studies with the help of simulation systems.
Simplicity of construction is foreseen to be achieved thanks to several innovative features (the large size of the sensors, the front-end chip directly sitting on the detector).
The conceptual design of infrared laser alignment system is built on its successful application to the AMS-1 tracking system [2], and on the current developments for the CMS silicon tracker alignment. According to the AMS experience few micron precision can be achieved.

Test beams, module testing

Modules built using various sensor and chip generations are thoroughly tested using signal generated from beta source or laser stimuli.

First results obtained by Paris and Prague group in 2005 show that S/N of 56 cm strips is around 12 (see Fig 5).
Testing SiLC modules in the beam in DESY will start in autumn 2006. Here namely signal-to noise measurements using monoenergetic beam will be performed. Timing aspects of the readout electronics will be studied as well.
Further detailed studies of the detector performance (spatial resolution, cluster size, etc.) will be realised at CERN high energy beam in 2007

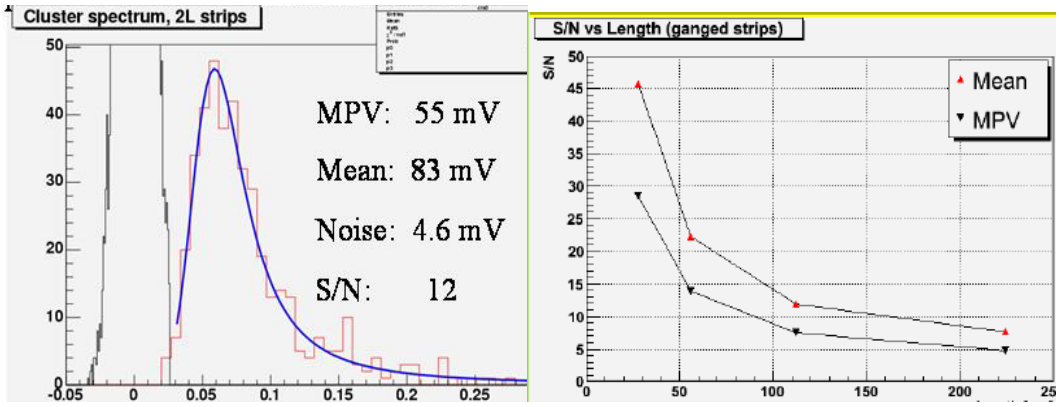

Fig. 5 Source tests: left: Signal spectrum for 56 cm sensor, right: Signal-to-Noise ratios for different strip lengths

Acknowledgment

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References

[1] SILC Collaboration, http://silc.in2p2.fr
[2] W. Wallraff, Nuclear Instruments and Methods in Physics Research A 511 (2003) 76–81