Simulation and test of 3D silicon radiation detectors

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Abstract

The work presented here is the result of the collaborative effort between the University of Glasgow, ITC-IRST (Trento) and IMB-CNM (Barcelona) in the framework of the CERN-RD50 Collaboration to produce 3D silicon radiation detectors and study their performance.

This paper reports on two sets of 3D devices. IRST and CNM have fabricated a set of single-type column 3D detectors, which have columnar electrodes of the same doping type and an ohmic contact located at the backplane. Simulations of the device behaviour and electrical test results are presented. In particular, current-voltage, capacitance-voltage and charge collection efficiency measurements are reported. Other types of structures called double-sided 3D detectors are currently being fabricated at CNM. In these detectors the sets of n and p holes are made from opposite sides of the device. Electrical and technological simulations and first processing results are presented.

1. Introduction

3D silicon detectors consist of a three-dimensional array of p and n electrodes that penetrate into the detector bulk instead of being implanted on the wafer surface like in the standard planar detectors. These devices combine traditional VLSI processing and MEMS technology [1].

The 3D structure has several advantages over planar technologies. The distance between adjacent electrodes is determined by the desired spatial resolution, and is independent of the substrate thickness. Thus, the charge pulse in a 3D detector is much faster as the charge generated only has to traverse the short distance between electrodes rather than the full thickness of the substrate [1]. This enhances the radiation resistance of the devices, because the reduction in lifetime due to the radiation-induced traps will have a smaller influence on the signal pulse height. Similarly, because 3D devices only have to be depleted across the distance between the electrodes, their depletion voltage is low. 3D detectors also have advantages in terms of charge sharing as their design provides self-shielding of the electrodes, separating out the electric field region of each pixel [2].

However, the fabrication of 3D detectors is full of technological challenges. One of the main difficulties is to integrate the etching and doping of the n and p columnar electrodes into the fabrication sequence. This work presents two different approaches to simplify the fabrication process of the devices: single-type column and double-sided 3D detectors.

2. Single type column 3D detectors

The Single-Type Column 3D (STC-3D) detectors have been proposed and designed by ITC-IRST (Trento). These devices consist of columnar electrodes of the same doping type implanted in the silicon substrate, so that the column etching and doping is performed only once. The columns are not filled. Instead, they are etched away, doped with phosphorous from a solid source, and a layer of oxide is grown inside them for passivation. Also, the electrodes do not go all the way through the wafer, so there is no need for a support wafer during the fabrication. The ohmic contact is achieved by a uniform implant at the back surface of the wafer, so the process is single-sided. The details of the technology can be found in [3].

2.1. Electrical simulation

Simulations of the electrical behaviour of the devices were carried out in the University of Glasgow with ISE-TCAD 7.0. The simulated device has n^+ columnar electrodes implanted on a p-type silicon substrate. For simplicity, the columns are not hollow but made of silicon doped with phosphorous with a concentration of 10^{19} cm^{-3}. The column depth is 150 μm, the diameter is 10 μm, the pitch is 80 μm and the wafer thickness is 500 μm. The substrate resistivity is 5 kΩ·cm, which corresponds to a boron doping concentration of $2.6 \cdot 10^{12}$ cm^{-3}. There is an oxide layer with a positive charge of 10^{11} cm^{-2} on the top surface, although no isolation structures (p-stop or p-spray) were defined for simplicity of the mesh.
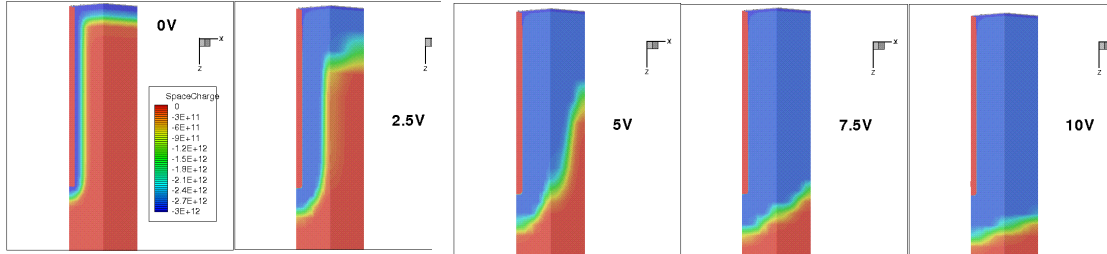

Fig. 1. Simulation of the depletion behaviour of a STC-3D detector. The colour red indicates zero and positive space charge, and the spectrum up to blue indicates increasing negative charge. The side of the figure is 40 μm, half the distance between two adjacent electrodes. The back p^+ contact is not shown.

Figure 1 shows the depletion of the simulated device as the voltage difference between the electrodes is increased. It takes place in two stages: first, the depleted region grows laterally from the n^+ electrodes until at 7.5 V the region between the columns is fully depleted, and then progresses like in a planar device towards the back contact. The detector volume is fully depleted at an approximate voltage of 300 V, compared to 500 V for the equivalent planar detector. Naturally, the depletion voltage will vary with doping concentration and substrate thickness.

Charge collection in those devices is relatively slow due to the zero field regions in the centre of four columns where the charge carriers move only by diffusion. According to the simulation results, the peak of the pulse produced by an incident particle in this region will arrive to the readout electrode in 2.5 ns, although the complete collection of charge will take 10 ns.

2.2. Devices

ITC-IRST (Trento), with the collaboration of IMB-CNM (Barcelona), have fabricated a set of STC-3D detectors. The wafers include pad and strip-like 3D detectors, some planar diodes and other test structures.

As in the simulations, the fabricated devices consist of 150 μm columns implanted on a p-type substrate. Two types of wafers were processed: float zone (FZ) silicon, with a minimum nominal resistivity of 5 kΩ·cm and a thickness of 500 μm, and magnetic Czochralski (MCZ) silicon, with a minimum resistivity of 1.8 kΩ·cm and a thickness of 300 μm. The dimensions and substrate characteristics of the diodes fabricated on the FZ substrate match the used in the simulation.

The STC-3D pad detectors consist of a 10×10 matrix of interconnected holes connected together to the bias line. A guard ring of holes surrounds the active area. Different p-stop geometries were used to isolate the n^+ electrodes. Type 3D1 detectors have a single p-stop ring around each hole. Devices 3D3 and 3D5 have a strip-like p-stop between the lines of holes plus a p-stop separating the active area from the guard ring. Finally, devices 3D2 and 3D4 have a single p-stop between the active area and the guard ring. The distance between columns is 80 μm in all devices except for the 3D4 diodes, where it is 100 μm.

2.3. Test

The electrical characterisation of the pad STC-3D detectors was performed at the facilities of the University of Glasgow by current-voltage (I-V), capacitance-voltage (C-V) and charge collection efficiency (CCE) measurements.

The capacitance-voltage characteristics were measured at 10 kHz with an HP 4284A LCRMeter. The samples were placed in a Cascade Microtech probe station to avoid electromagnetic interferences. The guard rings of the devices were not biased for the C-V measurements.

Figure 2 shows the C-V curves of the STC-3D diodes fabricated on the FZ wafers. The characteristics of a standard planar diode fabricated on the same substrate and of the simulated device are also shown. The characteristics of devices 3D1, 3D3 and 3D4 show a kink at about 8 V that is due to the isolation of the p-stop from the backplane when the region between the columns becomes fully depleted. This kink is more visible in devices 3D3 and 3D5, which have wider p-stops. Detectors 3D2 and 3D4, with no p-stops in the

active area, show a smooth depletion behaviour, similar to the shown by the simulated device. For voltages higher than 10 V, the volume between columns is fully depleted and the depleted volume progresses towards the backplane, so the C-V curves of the 3D diodes become similar to the characteristic of the planar diode. Due to setup limitations the characterization could only be performed up to 40 V, so the full depletion voltage of the detectors could not be estimated from the measured C-V curves.
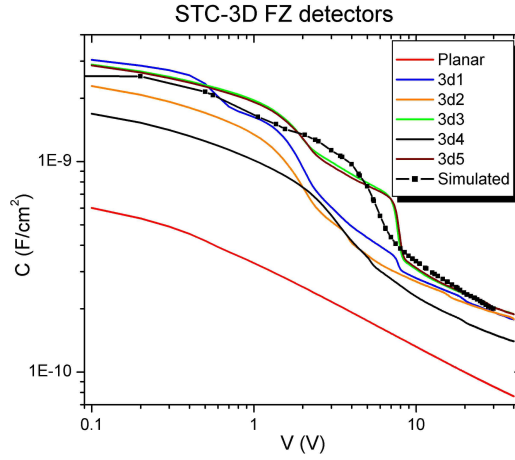

Fig. 2. Capacitance-voltage curves of the 3D detectors. The characteristics of a planar diode and of the simulated device are also shown for reference.

The I-V characteristics were obtained with a Keithley 4200-SCS Semiconductor Characterization System. The guard rings and the active area were biased simultaneously. The results for FZ and MCZ silicon are shown in Figure 3. The current levels are low and similar for both substrates. 3D4 samples, with larger pitch, have lower currents, comparable with the current of a planar device. It is also clear that the p-stop geometry has an effect on the breakdown voltage: 3D1 samples, with a single p-stop around each hole, show an earlier breakdown due to the close proximity of the p^+ implants to the n^+ electrodes. However, the breakdown voltage is sufficiently high to allow safe operation of the devices.

Table 1 shows the volume current density and the current per column for each type of device, measured 20 V above the full depletion voltage. V_{FD} was assumed to be 180 V for the FZ diodes and 35 V for the MCZ, according to the results reported in [4]. The current per column at $V_{FD}+20$ V is less than 2 pA in the case of the FZ detectors, except for the 3D1 sample, and 350-630 fA for the MCZ devices.
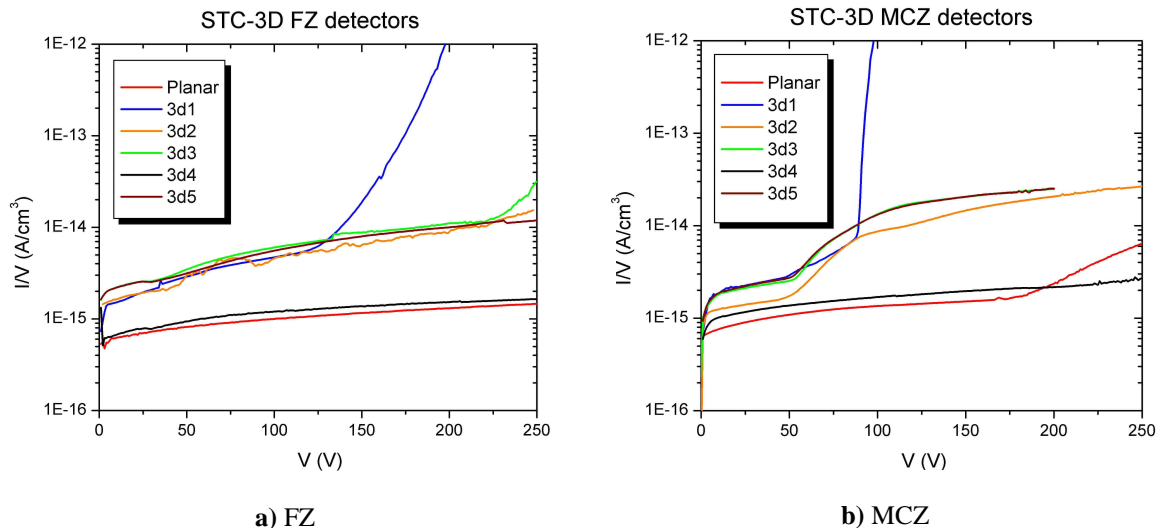

a) FZ   **b)** MCZ

Fig. 3. Current-voltage curves of the FZ and MCZ 3D pad detectors. The characteristic of a planar diode is also shown for reference

The charge collection efficiency measurements were carried out with β^- particles from a ^{90}Sr source. Figure 4 shows the CCE curve for a 3D5 detector fabricated in MCZ silicon. The charge collected is normalized to the value expected by an ideal detector 300 μm thick, 3.5 fC. Three different stages can be clearly distinguished. At low biases, the efficiency increases very rapidly with the applied voltage thanks to the fast depletion of the region between columns. The change on the slope of the CCE curve at about 8 V indicates

that the volume between the electrodes has became completely depleted. This is followed by a second stage where the charge collected increases more slowly with the voltage as the depletion progresses towards the backplane. All the charge generated by the incoming particle is collected for voltages higher than 25 V, which indicates that all the detector volume has reached full depletion. Another interesting feature of these devices is that there is non-zero charge collection at 0 V, due to the depleted region already present around the columns in the unbiased device, as can be seen in Fig. 1.

	Per column (A)		Per unit volume (A/cm^3)	
	FZ	MCZ	FZ	MCZ
3d1	6.68×10^{-10}	5.66×10^{-13}	2.58×10^{-12}	3.64×10^{-15}
3d2	2.60×10^{-12}	3.80×10^{-13}	1.00×10^{-14}	2.44×10^{-15}
3d3	2.86×10^{-12}	5.83×10^{-13}	1.10×10^{-14}	3.75×10^{-15}
3d4	6.21×10^{-13}	3.49×10^{-13}	1.53×10^{-15}	1.44×10^{-15}
3d5	2.72×10^{-12}	6.32×10^{-13}	1.05×10^{-14}	4.06×10^{-15}
planar	--	--	1.34×10^{-15}	1.16×10^{-15}

Table. 4. Current measured at $V_{FD}+20$ V, per column and per unit volume, in the STC-3D pad detectors.
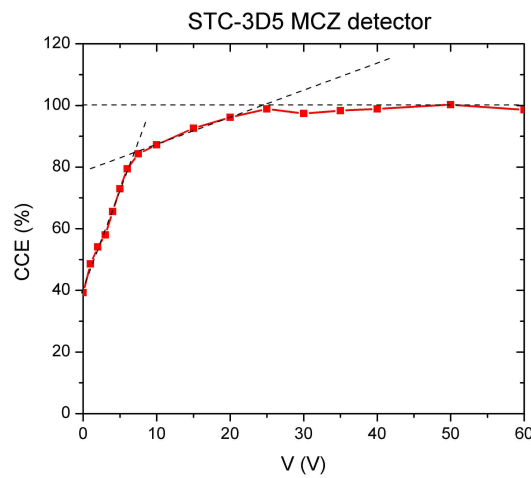

Fig. 4. Charge collection efficiency of a STC-3D pad detector with 3D5 geometry. The substrate is MCZ silicon with a thickness of 300 μm.
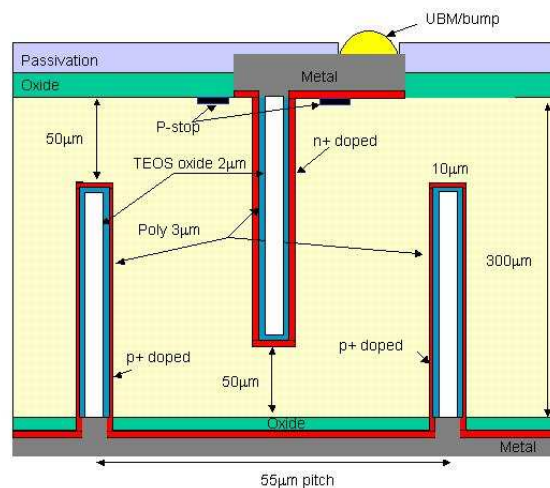
3. Double-sided 3D detectors

Fig. 5. Design of the "double-sided" 3D detector.

Designed by IMB-CNM (Barcelona), the "double-sided" 3D structure is a different approach aimed to simplify the fabrication process. In this case, the columnar electrodes are drilled from different sides of the wafer. This design constitutes a close approximation to the ideal 3D detector with a simpler technology, as it

avoids the difficulty of doping the two different kinds of holes on the same side of the wafer. Furthermore, with this configuration it is not necessary to bond the wafer to a support wafer for mechanical strength.

Figure 5 shows the proposed structure. The readout electrodes are n^+ columns etched from the top surface of the wafer and isolated by means of a p-stop implant. The p^+ columns are etched from the back side and are all shorted together. The pitch is 55 μm and the columns are 250 μm deep with a wafer thickness of 300 μm.

3.1. Electrical simulation

The depletion behaviour of this type of detector, simulated with ISE-TCAD 7.0, is shown at Fig.6. The simulation was done for a p-type substrate with a resistivity of 18 kΩ·cm, which corresponds to a boron doping concentration of $7·10^{11}$ cm^{-3}. There is an oxide layer at the top and bottom surfaces with a positive charge of 10^{11} cm^{-2}.

The depletion region grows horizontally and vertically outwards from the n^+ columns, so that the region where the columns overlap is fully depleted at voltages lower than 5 V. The detector volume is fully depleted at 10 V, while for a standard planar detector of the same thickness the full depletion voltage is an order of magnitude higher. In the volume between columns the charge carriers generated by radiation will be swept away horizontally by the electric field to the electrodes and collected in a few ns like in an ideal 3D detector [1]. At 20 V, for a particle arriving midway between the electrodes, 92% of the charge generated will be collected in 3 ns, and 97% of the charge in 5 ns. This is five times faster than a standard planar silicon detector which takes about 25 ns.
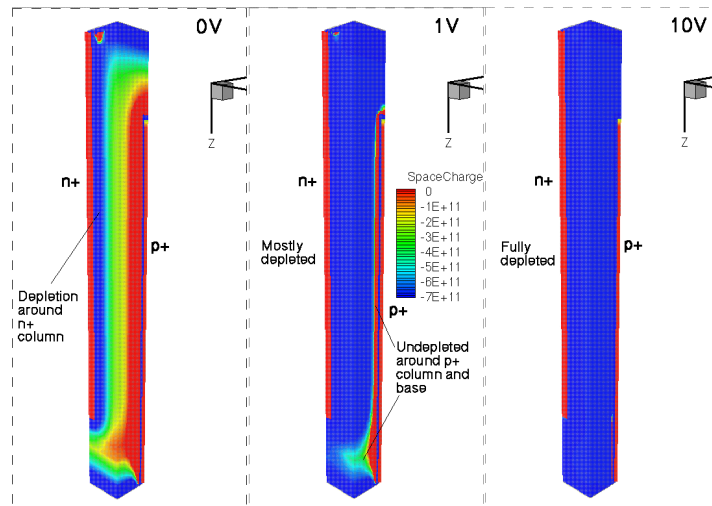

Fig. 6. Simulation of the depletion behaviour of a "double-sided" 3D detector. The side of the figure is 27.5 μm, half the pitch between two electrodes. Colours are the same as in Figure 1.

3.2. Technology

The fabrication process has been designed and checked by means of technological simulations with ISE-TCAD and dedicated test runs. The holes are etched with an Alcatel 601-E DRIE machine. A maximum aspect ratio of 24:1 has been achieved using an Al/Cu mask. Then the holes are filled with a polysilicon layer and doped from BN dopant wafers in the case of boron, and in a POCl$_3$ ambient for the phosphorous. Finally, they are passivated with a TEOS oxide layer. Figure 7 shows a SEM micrograph of the bottom of a high aspect ratio hole etched on n-type silicon. It can be seen that both the TEOS oxide and the polysilicon layer are uniform and have reached the bottom of the hole. The p^+ doped silicon can be clearly distinguished as a shadowed area around the hole. The boron profile is smooth at the corners.

A study of P and B doping has been performed to check the characteristics of the junction for different diffusion temperatures and times. Figure 8 shows the boron profile, measured with the spreading resistance technique, obtained with a diffusion of 10 min at 1050° C through a 3 μm polysilicon layer. The figure also shows the profile obtained with the technological simulation of the fabrication process. The simulation fits well with the measured profile. The depth of the p-n junction, for a n-type silicon with a resistivity 7.5 kΩ·cm (P concentration $5.7·10^{11}$ cm^{-3}), will be 2.4 μm, an acceptable value for detector applications. The sheet resistance of the doped polysilicon is $(0.98 ± 0.03)$ Ω/sq.

A set of masks has been designed for the fabrication of prototype double-sided 3D detectors. The wafers will include 3D detectors with Medipix2, ATLAS pixel and Pilatus geometry, simple pad and strip-like 3D detectors and test structures. The production of a set of detectors on n-type silicon wafers is already started.
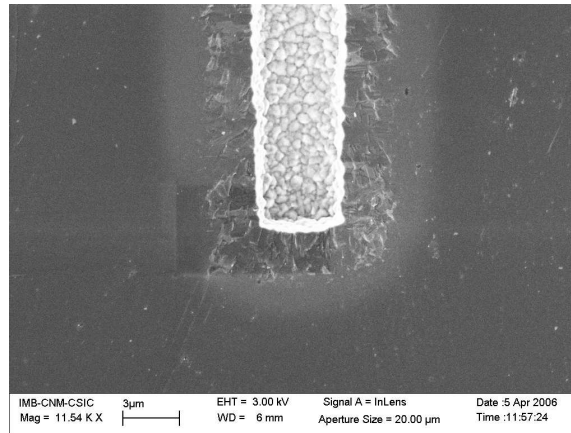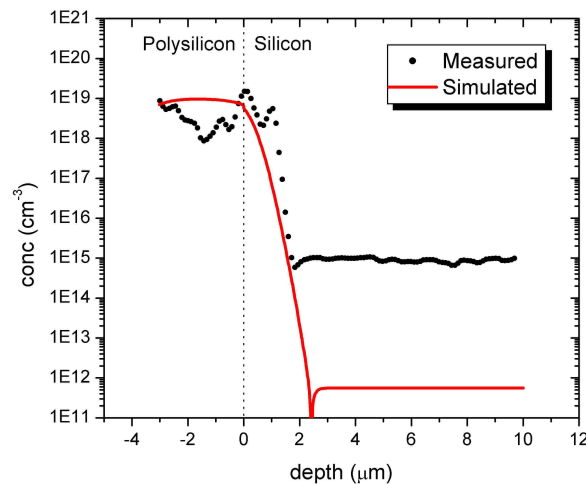
Fig. 7. SEM image of the bottom of a hole.

Fig. 8. Simulated and measured profile for a boron diffusion of 10 min at 1050$^{\mathrm{o}}$ C.

4. Conclusions

Two different 3D detector designs have been presented. The single-type column 3D detectors feature columnar electrodes of the same doping type at the front side of the wafer, with the ohmic contact located in the backplane. For a pixel pitch of 80 μm the volume between electrodes becomes fully depleted at less than 10 V, and then the depletion progresses towards the back contact like in the planar devices. The leakage currents are low and the breakdown voltage is high enough to safely operate the detectors. The CCE measurements show that all charge is collected at about 25 V for a detector thickness of 300 μm. These devices are a good alternative to conventional planar detectors for experiments that do not need a fast response.

A second design, closer to the ideal 3D detector, is the double-sided detector, where the columns are etched from opposite sides of the wafer. Electrical simulations show that the whole volume of the silicon is fully depleted at 10 V and that charge collection is five times faster than in planar detectors. Technological simulations and test runs have been used to optimize the hole etching and doping technology. The fabrication of the first set of double-sided 3D devices is ongoing.

References

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