Total Dose Dependence of Oxide Charge, Interstrip Capacitance and Breakdown Behavior of sLHC Prototype Silicon Strip Detectors and Test Structures of the SMART Collaboration

H. F.-W. Sadrozinski, C. Betancourt, R. Heffern, I. Henderson, J. Pixley, A. Polyakov, M. Wilder
SCIPP, UC Santa Cruz, CA 95064 USA
M. Boscardin, C. Piemonte, A. Pozza, and N. Zorzi
ITC-irst, Divisione Microsistemi, Via Sommarive 18,
I-38050 Povo (Trento), Italy
G.-F. Dalla Betta
DIT, Università di Trento,
Via Sommarive 14, I-38050 Povo (Trento), Italy
M. Bruzzi
Dipt. Energetica, Univ. of Florence
Via S. Marta 3, I-50139 Firenze, Italy
A. Macchiolo
INFN Florence
Via G. Sansone 1, I-50019 Sesto F., Italy
L. Borello, A. Messineo
INFN Pisa
Largo B. Pontecorvo, 3, I - 56127 Pisa, Italy
D. Creanza
INFN Bari,
Via E. Orabona 4, I-70126 Bari, Italy

For the SMART Collaboration

Abstract
For the future luminosity upgrade proposed for the Large Hadron Collider (LHC) silicon strip detectors (SSD) and test structures were fabricated on various high-resistivity substrates (p-type MCz and FZ, n-type FZ) within the INFN funded SMART project. They were irradiated with ^{60}Co to test total dose (TID) effects, in order to study the impact of surface radiation damage on the detector properties (interstrip capacitance and resistance, break-down voltage). Selected results from the pre-rad and post-rad characterization of detectors and test structures are presented, in particular interstrip capacitance, break-down voltage, flatband voltage and oxide charge. They show saturation at about 150 kRad. Annealing are performed both at room and at elevated temperature.

1. Motivation

The future luminosity upgrade proposed for the Large Hadron Collider (LHC) requires a critical evaluation of the radiation hardness of the silicon strip detectors (SSD) proposed as main tracking detectors in the Inner Detector (ID) of the upgraded LHC detectors [1]. The CERN R&D collaboration RD50 was formed to investigate radiation damage in semiconductor detectors and develop radiation-tolerant tracking detectors [2]. The INFN funded SMART project, that involves several Italian institutes belonging to RD50, has fabricated silicon strip detectors and test structures on various high-resistivity substrates [3]. The aim of this activity is to thoroughly characterize the different design/technology options so as to understand the details of fabrication steps which will permit the fabrication of radiation-tolerant SSD.

As far as bulk radiation damage is concerned, which is the main problem to face, promising results have already been reported [4]. However, surface damage effects should also be considered, especially for detectors built on p-type substrates, for which isolation structures (p-stop or p-spray) are needed in between the n^+ strips to interrupt the inversion electron layer induced by the positive fixed oxide charge. In fact, simulation studies have clearly evidenced the strong impact of surface effects (oxide charge, surface states) on the interstrip capacitance and the breakdown voltage, as well as on the isolation properties of the p-

stop/p-spray regions [5]. This paper describes experimental results from the electrical characterization of detectors and test structures irradiated with ^{60}Co to test total dose (TID) effects.

2. Devices

Identical test structures were fabricated together with SSD on the different wafers. Of them, as shown in Table I, short SSD of varying strip width and pitch, circular MOS capacitors with aluminum top electrode, and Capacitance test structuresTS (mini strip detectors) are considered for this study, and results are presented for a subset of the available SMART wafers, as listed in Table II. Table III lists the details of the SSD investigated.

Table I: Structures Investigated

Type	Dimension	Measurements	Frequency
MOS Capacitor	Circular Area =3.14mm^2	C-V	10 kHz
Capacitance TS	Length = 1.15 cm Pitch = 50, 100 um Implant = 15, 25 um Poly width = 10 um Metal = 23, 33 um	Cint-V C-V i-V	~ 1 MHz 10 kHz n.a.
SSD	Length = 4.46 cm Pitch = 50, 100 um Implant = various	Cint-V C-V i-V	~ 1 MHz 10 kHz n.a.

Table II: Wafers Investigated

Wafer Type	Wafer #	Thickness [um]	P-spray Dose [cm^{-2}]	SSD / TS / MOS
n FZ	W1254	300	n.a.	TS, MOS
p FZ	W084	200	$5*10^{12}$	TS, MOS
p FZ	W014	200	$3*10^{12}$	SSD
p FZ	W037	200	$5*10^{12}$	SSD
p MCz	W044	300	$3*10^{12}$, no passivation	TS, MOS
p MCz	W253	300	$5*10^{12}$, no passivation	TS, MOS
p MCz	W066	300	$3*10^{12}$, no passivation	SSD
p MCz	W182	300	$5*10^{12}$, no passivation	SSD

Table III: Silicon Strip Detectors (SSD) Investigated

SSD	Substrate	P-spray Dose [cm^{-2}].	Pitch (μm)	# strips	Implant Width (μm)	Poly Width (μm)	Metal Width (μm)
14-5	FZ 200	$3*10^{12}$	50	64	15	10	27
14-8	FZ 200	$3*10^{12}$	100	32	35	30	43
37-5	FZ 200	$5*10^{12}$	50	64	15	10	27
37-8	FZ 200	$5*10^{12}$	100	32	35	30	43
66-8	MCz	$3*10^{12}$	100	32	35	30	43
182-5	MCz	$5*10^{12}$	50	64	15	10	27
182-8	MCz	$5*10^{12}$	100	32	35	30	43

3. Sample Preparation

The test structures are comprised of 9 AC coupled strips, of which the inner-most three allow the measurement of the interstrip capacitance from the central strip to its pair of next neighbors, and the outer

three strips on each side are connected together to allow bonded connections to a shield, for which we used the bias ring. We compared the interstrip capacitance of a test structure with the one of a 4.45 cm long mini-SSD, where the interstrip capacitance was measured to 3 pairs of next neighbors, with the next 3 strips on each side grounded to shield. The expected ratio of 1.2 between the capacitance to the next pair and to the next three pairs is seen. In addition, pre-rad the effect of bonding the shield strips to the bias ring is large. This difference disappears post-rad.

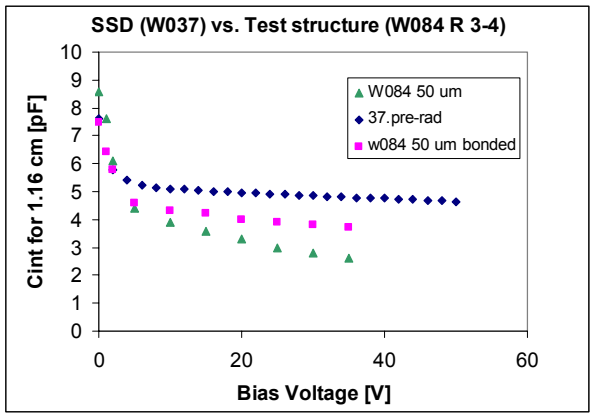

Fig. 1 Measurement of the interstrip capacitance (Cint) for p-type MCz pre-rad. For the mini-SSD W037, the capacitance to the 3 pairs of next neighbors are measured, while for the test structure W084 R 3-4, the capacitance toonly the pair of next neighbors is measured. The expected ratio of 1.2 is measured. For the test structure W084 R 3-4, the effect of bonding out the shield strips to the bias ring are is shown, The capacitance is scaled to a length of 1.15 cm.

4. Data

a. Irradiations

Irradiations were performed in the UC Santa Cruz ^{60}Co source in steps of approximately 70 krad, corresponding to one day irradiation at a dose rate of 3.15 kRad/hr. The parts were irradiated with their electrical terminals floating.

b. Annealing

With the devices being irradiated with their terminals floating, a certain amount of room temperature annealing has to be expected. This is shown in the graphs as double-valued parameters for the same dose. A more thorough annealing at elevated temperature was performed at the end of the irradiation, lasting for one week at 60^{o}C.

c. Measurements

Frequency dependent C-V characterizations using an HP 8241 LCR meter were performed before the irradiation, and within a few days after each step. At the end, the capacitance-voltage (C-V) data at 10kHz were analyzed for the MOS capacitors, while the interstrip capacitances (Cint-V) were analyzed at the highest frequency used, e.g. 800 kHz or 1 MHz.

The bias dependence of currents and capacitances Cint could be determined only partially pre-rad because of breakdown which occurred in some cases before depletion. A dramatic increase in breakdown voltage after irradiation can be observed (see below). In fact, before irradiation, detectors with high-dose p-spray isolation had a breakdown voltage in the 50-150V range, depending on the width/pitch value. On the contrary, after 210krad, a much larger reverse bias can be applied without the risk of breakdown.

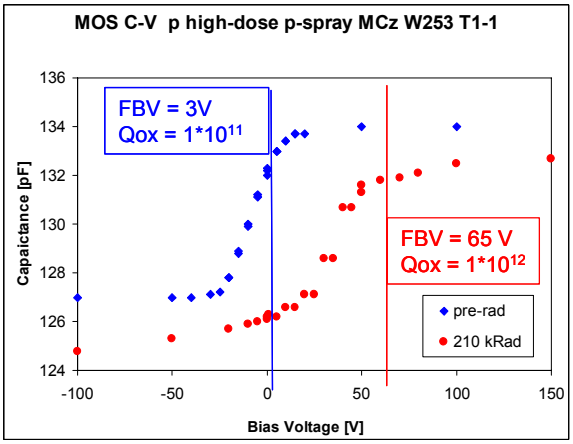

Fig. 2 Capacitance – voltage (C-V) characteristics of a MOS capacitor fabricated on a p-type MCz wafer with high-dose p-spray, both pre-rad and after a total dose of 210 krad of ^{60}Co gammas. The flatband voltage increases from about 3 V pre-rad to about 65 V after a total dose of 210 krad.

During data taking on the MOS capacitors, several observations were made which limits the accuracy of the extraction of flatband voltage and the oxide charge. First the C-V curves display hysteresis (Fig. 2). The capacitance values for ramping up the voltage differ from the ones ramping down, for the same value of the bias voltage. This is due to extremely slow charge-up and discharge of the capacitor, and presumably could be avoided with much longer waiting time. Second, the C-V curves show "notches" in the C-V curve and/or bi-stable capacitance values at certain voltages. The reason is not understood yet.

d. Results on MOS capacitors

The C-V measurements on MOS capacitors are being analyzed to extract the flatband voltage and the oxide charge and their evolution through the irradiation [6]. The doping density can be extracted as part of the process and is of the order 10^{16} to 10^{17} cm^{-3} for p-type and 10^{11} to 10^{12} cm^{-3} for n-type, as predicted from process simulations [5]. Figs. 3 and 4 show the evolution of the flatband voltage and the oxide charge with dose. Saturation is observed after about 150 kRad, and strong annealing reduces the effect during the irradiation process and after the elevated anneal. Such a strong annealing effect has been observed before, also on MOS structures processed at ITC-irst and irradiated with X-rays [7].

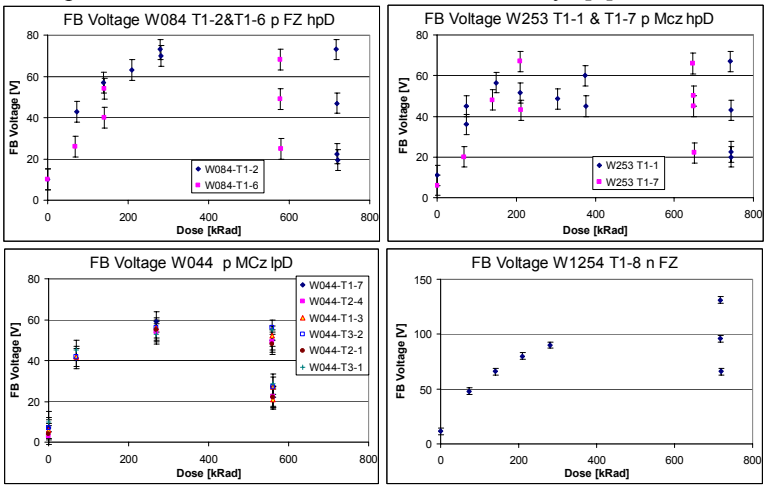

Fig. 3 Evolution of the flatband voltage with total dose for four different wafers: p-type FZ high-dose, p-type MCz high-dose, p-type MCz low-dose, n-type FZ. Data at the same dose indicate annealing: the first value is right after irradiation, the second after one week of room temperature annealing and the third after additional on week of annealing at 60 ^{o}C.

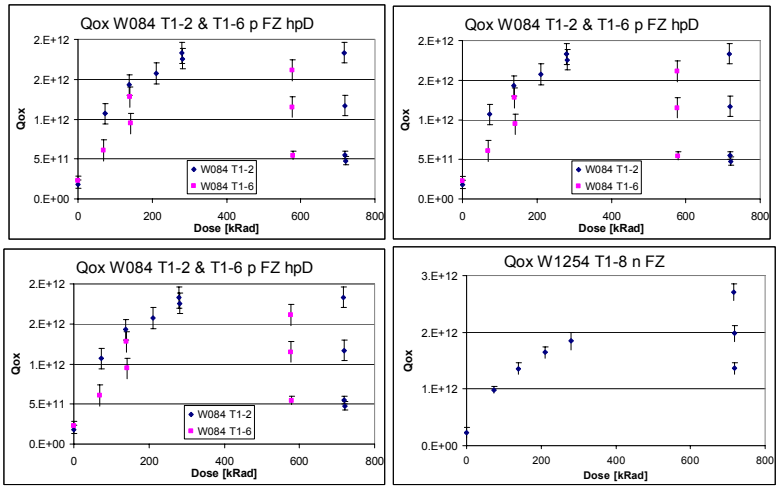

Fig. 4 Evolution of the oxide charge with total dose for four different wafers: p-type FZ high-dose, p-type MCz high-dose, p-type MCz low-dose, n-type FZ. Data at the same dose indicate annealing: the first value is right after irradiation, the second after one week of room temperature annealing and the third after additional on week of annealing at 60 °C.

e. Results on SSD and SSD test structures

The I-V curves at different doses (Fig. 5) reveal a dramatic increase in breakdown voltage after irradiation. In fact, before irradiation, detectors with high-dose p-spray isolation had a breakdown voltage in the 50-150V range, depending on the width/pitch value. On the contrary, after 210krad, a much larger reverse bias can be applied without the risk of breakdown. Large annealing effects lower the breakdown voltage again at intermediate irradiation steps and at the post-radiation elevated annealing step. Table IV shows the breakdown voltage at several steps in the irradiation campaign.

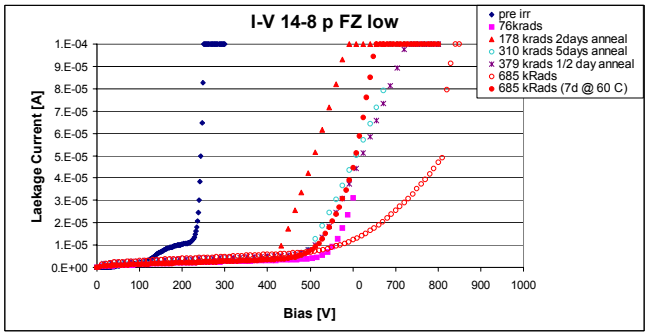

Fig. 5 Leakage current – voltage (I-V) curves for several irradiation steps.

Table IV Breakdown Voltage

Device	Breakdown Voltage [V]				
	pre-rad	75 kRad	300 kRad	~650 kRad	~650 kRad +7d @60 °C
66-8 p MCz low	250	550	900		
182-8 p MCz high	70	>200	350	>1000	500
14-8 p FZ low	240	600	600	700	600
37-8 p FZ high	70	200	300		

The results from capacitance measurements on test structures show a saturation trend similar to the MOS capacitors (Figs. 6 and 7). The irradiation lowers Cint drastically for p-type SSD, and the Cint geometrical value is approached as the voltage is increased. This result is in good agreement with simulation

predictions, and is due to the depletion region widening inside the p-spray at the surface [5]. Saturation is reached at a dose between 70 and 150 kRad. The wafer with low-dose p-spray isolation reaches the saturation already with 70 kRad, with very little residual voltage dependence of the interstrip capacitance. As observed before, the n-type test structures show increased interstrip capacitance with increased dose, while the p-type test structures exhibit reduced interstrip capacitance. There is no dependence of wafer type, i.e. MCz and FZ behave exactly the same, separately for high and low p-spray dose, respectively. The amount of annealing is very limited.

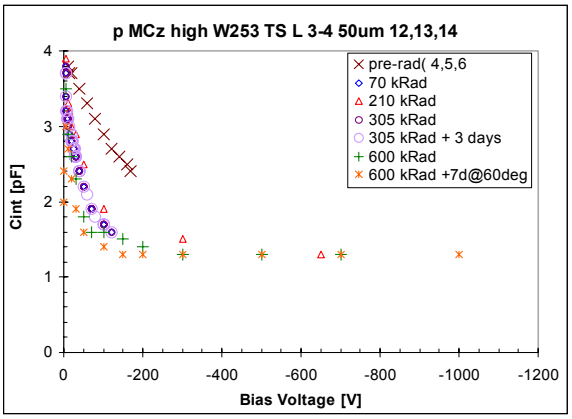

Fig. 6 Evolution of the interstrip capacitance of the 50 um pitch test structures with total dose for p-type MCz high-dose wafers. The remaining p-type test structures behave the same way, including the absence of strong annealing effects.

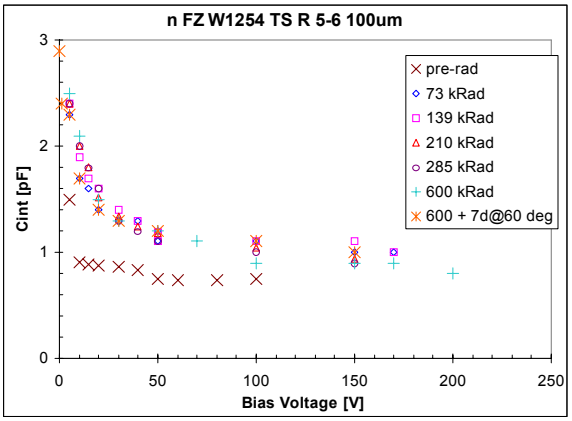

Fig. 7 Evolution of the interstrip capacitance of the 100 um pitch test structures with total dose for the n-type FZ wafer. Saturation is seen at about 100 kRad, and annealing is limited.

The same trends are seen with the mini-SSD. Fig 8 compares the interstrip capacitance vs. bias voltage for two p-type wafer types (MCz and FZ) and two p-spray doses. There is no difference between MCz and FZ, but large differences due to the surface treatment, i.e. between low- and high-dose p-spray.

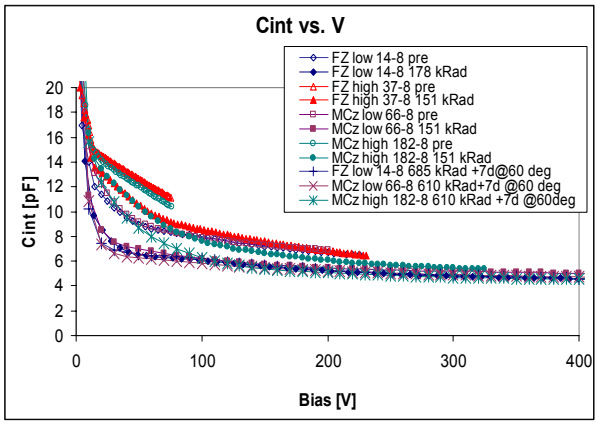

Fig. 8 Comparison of the interstrip capacitance of the 100 um pitch mini-SSDs, pre-rad and after saturation. Wafers 14 and 37 are FZ, wafers 66 and 182 MCz. There is little difference between different wafers, but large dependence on the p-spray dose. Again, saturation below 150 kRad and only limited annealing are observed.

5. Conclusions

The investigation of surface effects showed no dependence on the p-type wafer type (FZ vs. MCz), but large dependence on the surface treatment (high vs, low p-spray dose).
Saturation was observed for the interstrip capacitance at about 100 kRad, with very little annealing.
The flatband voltage and the oxide charge showed also saturation at about 150 kRad, but in addition a very large annealing by a factor 3.
The breakdown voltage was increased by the gamma irradiation, but also showed very strong annealing.

6. Acknowledgements

We thank the ITC-irst team for production of the devices and Forest Martinez-McKinney for help with the bonding.

7. References

[1] F.Gianotti *et al.,* Eur. Phys. J. **C 39**, 293 (2005)
[2] M. Moll, "Development of radiation hard sensors for very high luminosity colliders - CERN-RD50 project", Nucl. Instrum. Methods, vol. A 511, pp. 97-105, 2003.
[3] M. Bruzzi *et al*., "Processing and first characterization of detectors made with high resistivity n- and p-type Czochralsky silicon", Nucl. Instrum. Methods, vol. A 552, pp. 20-26, 2005.
[4] A. Macchiolo *et al*., "Radiation hardness of high resistivity n- and p-type magnetic Czochralski silicon", 7th Conference on Position Sensitive Detectors PSD07, Liverpool, UK, Sept. 2005, submitted to NIM A.
[5] C. Piemonte, "Device simulation of isolation techniques for silicon microstrip detectors made on p-type substrates", IEEE Trans. Nucl. Sci., vol. 53, no. 3, pp. 1694-1705, June 2006.
[6] E. H. Nicollian, J. R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology", Wiley-Interscience, 2002.
[7] M. Boscardin *et al.,*" An improved termination structure for silicon radiation detectors with all-p-type multiguard and cut-line implants", IEEE Trans. Nucl. Sci., vol. 50, no. 4, pp. 1001-1007, Aug. 2003.