Radiation Hardness Evaluation of SiGe Technologies for the Front-End Electronics of the ATLAS Upgrade

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1. Introduction

The microelectronic technology currently being used for the Front-End chip in the Inner Detector modules of the ATLAS experiment has been submitted to an extensive radiation assurance program, and it is known to be sufficiently radiation-hard for the radiation levels expected during the LHC life-span. Nevertheless, these studies have also revealed that this technology would not be valid for its application in the ATLAS Upgrade, given the ten-fold increase expected in radiation levels for the Super-LHC. In the search for new technologies that can be used for detector readout in the future upgraded modules, two possibilities have emerged: Deep Sub-Micron CMOS (DSM) and SiGe BiCMOS technologies. SiGe technologies are showing very good power/speed performances at relatively low consumptions in modern applications like mobile phones, wireless systems, or communications, that could give them some advantage as candidates for the ATLAS Upgrade Front-End chip. However, the radiation hardness of these technologies up to the high radiation levels expected in the Super-LHC experiment, is still to be verified.

In this framework, we have studied several SiGe HBT technologies from IHP (Innovation for High Performance Microelectronics, Germany) [1] in order to compare among them and with other manufacturers in the search for the best technological option. We have performed gamma and neutron irradiations to study separately ionization and displacement effects. We present the effect of these irradiations on different bipolar transistors from these technologies, and the implication of these effects on the suitability of these technologies for their use in the ATLAS Upgrade.

2. Experiments

Three different IHP technologies have been selected according to several criteria. Initially, their bipolar transistors have different vertical designs which can lead to variations in their radiation hardness. On the other hand, the alternatives that they present in terms of performance (speed, breakdown voltage), transistor types, passive components availability, and costs, give a wide range of options for the Front-End electronics of the ATLAS Upgrade. The characteristics of the three IHP's technologies are the following:

- SG25H1: f_T = 190 GHz, BV_{CEO} = 1.9 V, Beta = 200; This is the flagship of IHP's SiGe technologies, the one with highest frequency transistors.
- SG25H3: f_T = 120 GHz, BV_{CEO} = 2.3 V, Beta = 150; This is an alternative technology with more variety of transistor types and higher breakdown voltages.
- SGB25VD: f_T = 45 GHz, BV_{CEO} = 4.0 V, Beta = 190; This is a low cost technology, although with still quite high performance and high breakdown voltage transistors.

We have decided to use the minimum transistors of all the technologies as the most representative devices, plus larger transistors to account for possible emitter size

influence. The use of larger transistor has not been possible in all the cases because we have not used purposely designed test chips.

The test chips have been irradiated with gamma particles in order to study the ionization damage effects on the SiGe bipolar transistors. Two total doses have been reached: 10 Mrad(Si) and 50 Mrad(Si). In order to reach this very high doses in a reasonable time, a high dose rate of 342 rad(Si)/s have been used. This means that LDRE studies will have to be carried out in the future in order to assess the behavior at lower dose rates. The irradiations have been carried out in the Nayade facility at CIEMAT (Madrid, Spain) which is a water well Co60 irradiator.

The dosimetry has been performed by means of a Fricke system [2], and all irradiations have been performed using a PbAl shielding to avoid the dose enhancement effects due to secondary photons and to reach charge particle equilibrium at the samples, according to standards [3]. Transistors have been irradiated in a biased condition, with VBE ≈ 0.7 V and VCB = 0 V, to ensure a forward active bias, similar to the operation of the devices in the real life.

Neutron irradiations have also been performed in order to account for displacement damage. The transistors have been irradiated up to two total fluencies: 5 x 10^{14} cm^{-2} 1 MeV neutron equivalent and 1 x 10^{15} cm^{-2} 1 MeV n eq. The irradiations have been performed in the TRIGA reactor in Ljubljana, Slovenia, using a Cd shield to avoid thermal neutrons that can enhance excessively the damage on the transistors [4]. The transistors have also been irradiated under bias conditions as the ones described above.

3. Results and analysis

All devices have been measured first on wafer in order to make the selection of samples for the irradiations. Then, the wafers have been cut and the selected test chips glued and wire bonded to the purposely fabricated biasing boards. The devices have been re-measured on board to make sure that their characteristics have not changed or any devices have died during the bonding process. The forward Gummel plots of the transistors have been obtained, and the following figures of merit for the radiation damage have been extracted: *Final gain* (β_F) defined as the transistor current gain after irradiation at V_{BE} = 0.7 V; *Normalized gain* (β_N) defined as the common emitter current gain at V_{BE} = 0.7 V normalized to its value before irradiation; and $I_C(\beta = 50)$ as the minimum current to be applied on the collector at V_{CB} = 0 V for the transistor current gain to reach the value of 50 after irradiation. This last parameter is less common in the literature, but it is a good figure for the designers to know to what extent will they have to force their transistors (in the amplifier input stages) for them to keep working as expected.

Several measurements have been taken after some time periods in which the devices have been left for annealing. The annealing has been performed at room temperature and in a biased configuration for the gamma irradiated devices, and grounded configuration for the neutron irradiated devices. A beneficial annealing has been consistently observed in all the cases, with a saturation of the recovery after 10-15 days annealing period, as can be seen in Figure 1.

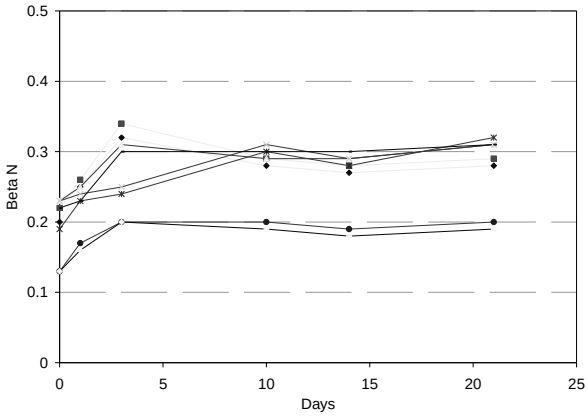

Figure 1: Annealing behavior of the transistors after irradiation.

3.a. Gamma irradiations

The effects of gamma irradiations on the Gummel Plot and current gain of transistors irradiated can be seen in Figure 2. The transistors are highly damaged after the maximum dose of 50 Mrad(Si) with a considerable increase of the base current with respect to the pre-irradiation value in the whole range of base-emitter bias, and the consequent large degradation of the current gain. As expected, no significant changes in the collector current can be observed in any transistor.

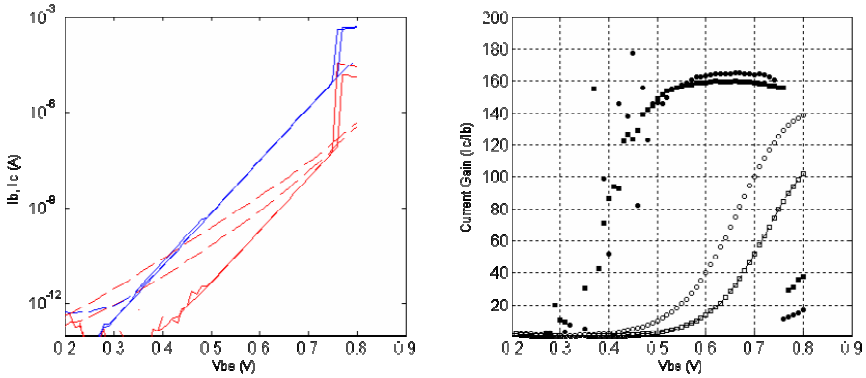

Figure 2: Gummel Plot and gain plot of an example transistor of technology SG25H3 irradiated up to 10 and 50 Mrad(Si) gamma dose.

Figure 3 shows the normalized current gain for the transistors of the 3 technologies studied in this work versus total dose. All three technologies suffer a similarly heavy damage from the gamma irradiation, although the results seem to reveal a heavier damage in the transistors from technology SG25H1 than in the ones from the other two technologies. Nevertheless, these differences are somehow enhanced in Figure 3 because the starting current gain of the transistors from technology SG25H1 irradiated up to 50 Mrad(Si) was higher than for the rest of transistors. If one compares the final current gains of all transistors, as shown in Table I, the tendency shown in Figure 3 remains the same, but with smaller differences among them.

Table I: Transistor gain values V_{BE} = 0.7 V for gamma irradiations

	SG25H1	SG25H3	SGB25VD	SG25H1	SG25H3	SGB25VD
PRE-IRRAD	133	164	201	266	159	199
10 Mrad(Si)	42	94	92			
50 Mrad(Si)				37	51	61

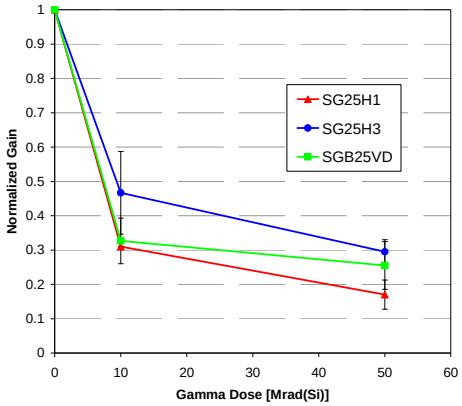

Figure 3: Normalized current gain results for the gamma irradiations on transistors of the 3 technologies studied as a function of total dose.

3.b. Neutron irradiations

Neutron irradiations have been performed only on technologies SG25H1 and SG25H3. As in the case of gamma irradiations, transistors show heavy damage after irradiation, as can be seen in the example Figure 4. No significant change in collector current has been seen either after the neutron irradiation.

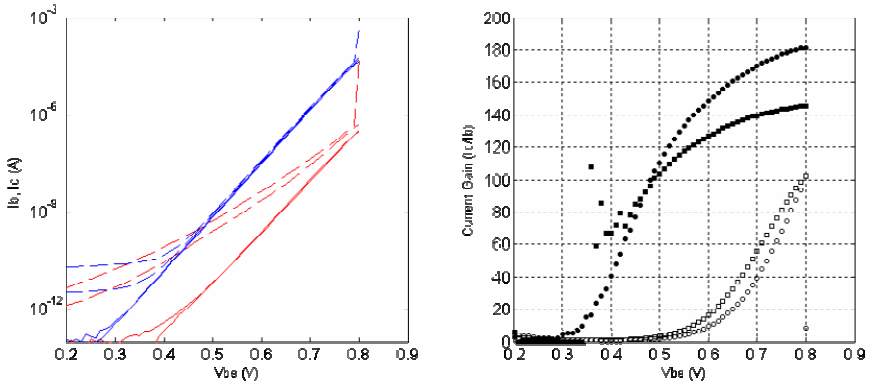

Figure 4: Gummel Plot and gain plot of an example transistor of technology SG25H3 irradiated to $5x10^{14}$ and $1x10^{15}$ equivalent 1 MeV neutrons.

The results from these irradiations on transistors of both technologies can be seen in Figure 5 for the normalized current gain, and summarized for the absolute final gain value in Table II. As can be seen in the graph, both technologies behave very similarly under irradiation. Nevertheless, a close look at the final beta values of transistors from technology SG25H3 in Table II, reveals values too low to be satisfactory for the experiment. However, it can also be seen that the starting gains of those transistors was too low (80-100) due to problems in the selection of the samples. Figure 5 suggests that satisfactory post-irradiation gain values would be obtained for this technology if the samples were selected from transistors with the typical gain value (150 for this technology). It is also necessary to notice here that the data shown here corresponds to measurements taken on the neutron-irradiated transistors after only 2 days of annealing at room temperature. It is expected that the final gain values will rise some more after more annealing time, as observed for the gamma-irradiated transistors.

Table II: Transistor gain values at V_{BE} = 0.7 V for neutron irradiations

	SG25H1	SG25H3
PRE-IRRAD	137	88
5 x 10^{14} cm^{-2}	54	30
1 x 10^{15} cm^{-2}	42	25

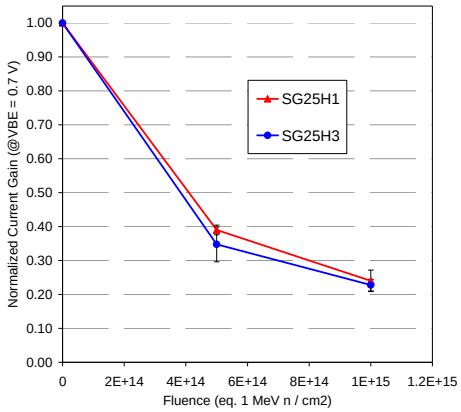

Figure 5: Normalized current gain results on transistors of the 2 technologies irradiated with neutrons versus equivalent 1 MeV neutron fluence.

Finally, Table III shows the values of the $I_C(\beta = 50)$ figure of merit for all technologies under gamma and neutron irradiation. It can be seen that, with the exception of transistors from technology SG25H3 irradiated with neutrons, for the same reason mentioned above, all the rest are in the order of the microamperes. This suggests that these transistors would remain operational after the 10 years of operation of S-LHC.

Table III: Collector current needed for transistor gain to reach a value of 50 in irradiated devices.

	Gammas		Neutrons	
	10 Mrad(Si)	50 Mrad(Si)	5 x 10^{14} cm^{-2}	1 x 10^{15} cm^{-2}
SG25H1	2.80E-06	1.71E-06	1.86E-06	3.75E-06
SG25H3	4.31E-07	1.51E-06	1.11E-05	1.39E-05
SGB25VD	9.23E-07	2.00E-06		

4. Conclusions

More statistics are needed to derive final conclusions on the selection of technology for the design of the FE electronics of the ATLAS Upgrade. Nevertheless, the results shown here suggest that, although very damaged, transistors from the three technologies studied would survive to 10 years of operation of the S-LHC. Only small differences can be observed among them with respect to their radiation hardness, that should be evaluated in more detail for a final technology selection.

References

[1] http://www.ihp-microelectronics.com

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[3] "Standard Practice for Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices Using Co-60 Sources", Annual Book of ASTM Standards, American Society For Testing And Materials (ASTM), E 1249–00, 2005.

[4] I. Mandic, et al. "Bulk Damage in DMILL npn Bipolar Transistors Caused by Thermal Neutrons Versus Protons and Fast Neutrons". IEEE Tran. on Nucl. Sci., Vol. 51, No. 4, 2004.