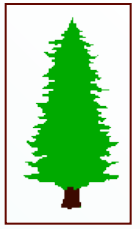
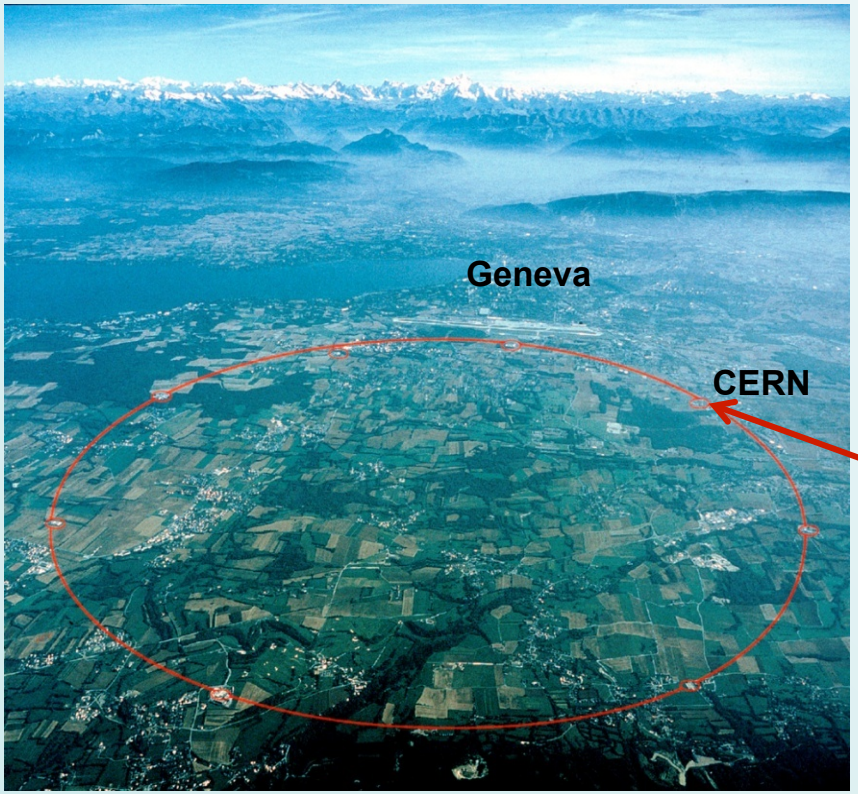


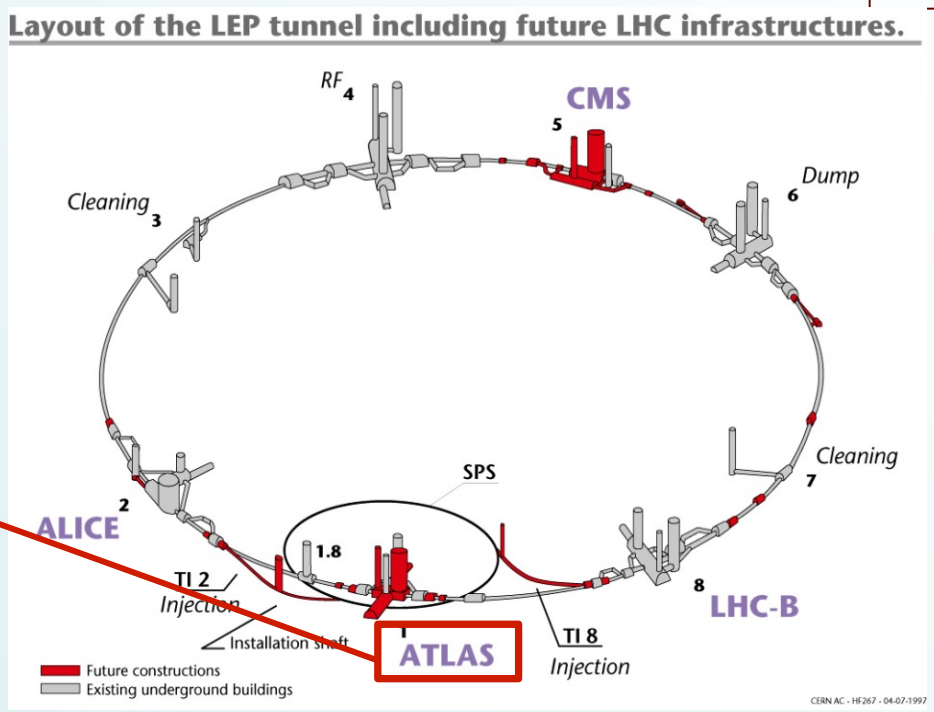
The ATLAS Experiment Upgrade Program

V. Fadeyev, A.A. Grillo, J. Nielsen, E. Spencer
SCIPP - UCSC

December 14, 2010

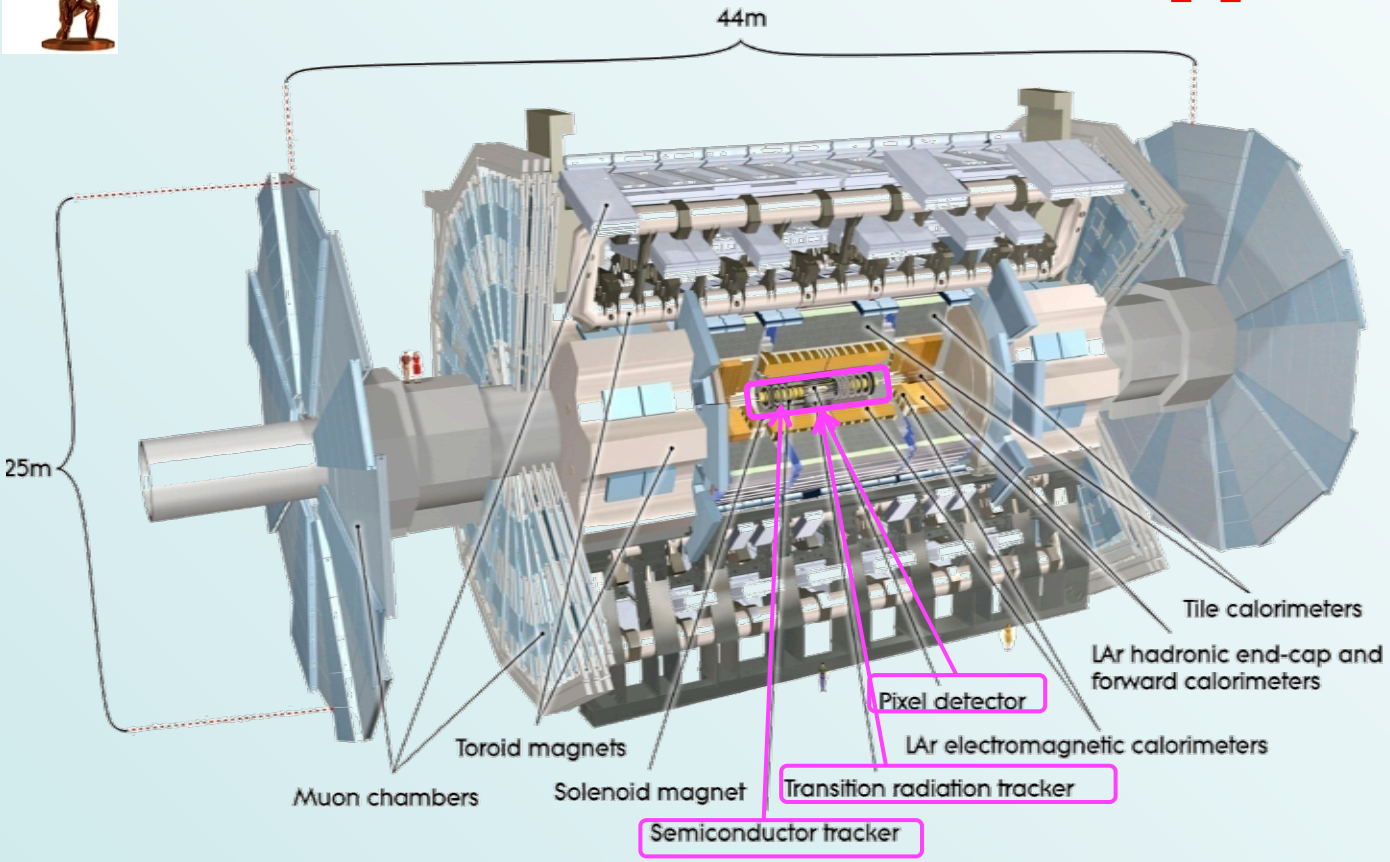
The Large Hadron Collider (LHC) at CERN





- The world's largest and most powerful particle accelerator
- An underground ring of superconducting magnets
- 27 km in circumference
- 2010-11: p-p collisions at **7 TeV** CM energy
- Instantaneous luminosity (L) = $10^{31} - 10^{34}$ cm^{-2} s^{-1}
- Long shutdown necessary to reach design energy or 14 TeV

A Toroidal LHC ApparatuS



4 major components:

- **Inner Detector**
- **Calorimeters**
  - Electromagnetic
  - Hadronic
- **Muon Spectrometer**
- **Magnet System**
  - central solenoid
  - muon toroids

- A general purpose LHC detector
- The largest particle detector of its kind in the world
- **44 m** long and **25 m** high, **7000 tons** (same as the Eiffel Tower)

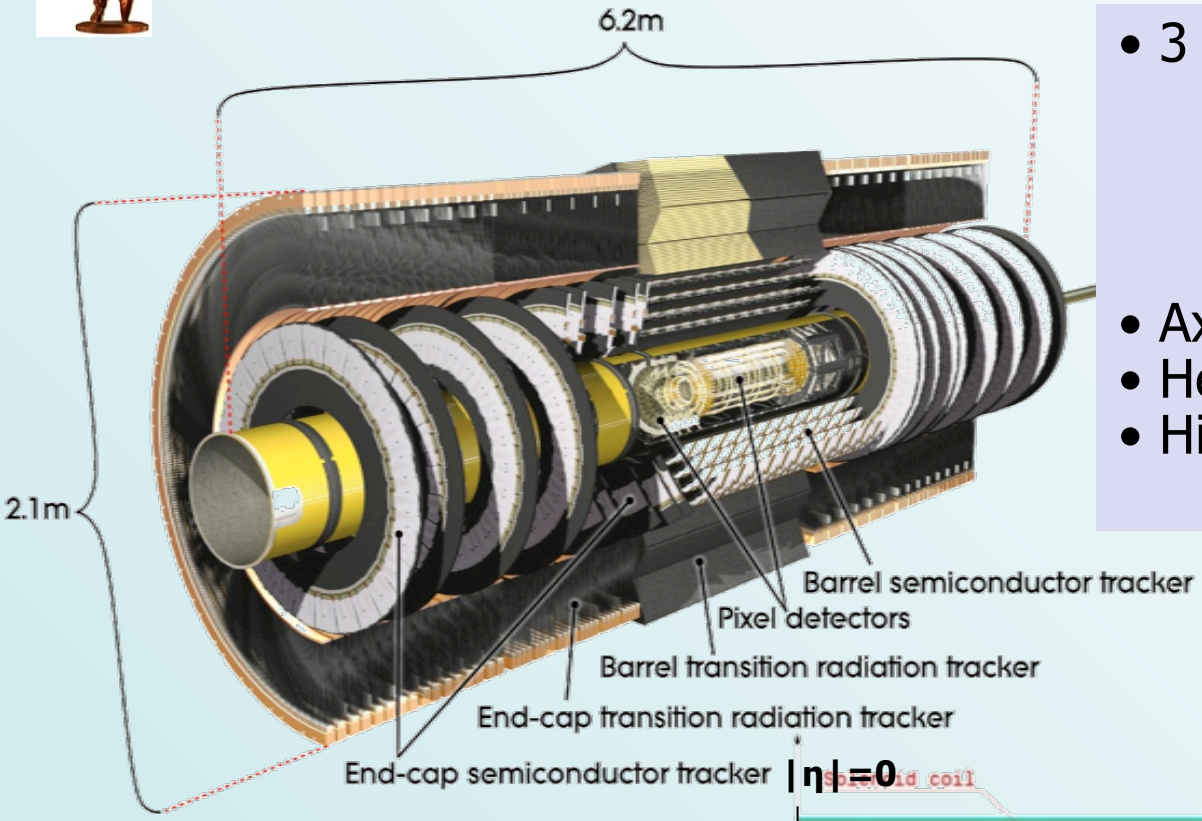
Search for new physics:

- **Search for the Standard Model Higgs particle.**
- **Search for Supersymmetric particles.**
- **New surprises at a new energy regime.**

Detailed studies of known sectors at higher energies with high luminosity:

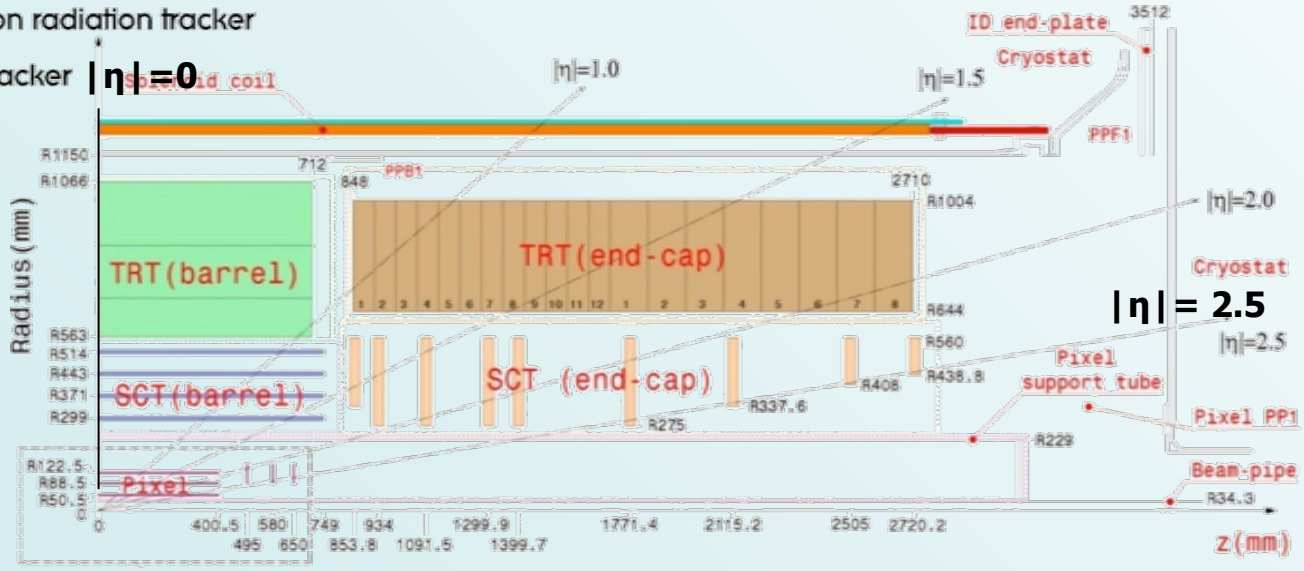
- **Study Top-quark Physics & B-quark Physics.**

ATLAS Inner Detector



- 3 technologies:
  - Silicon Pixels
  - Silicon micro-strip layers (**SCT**)
  - Straw tube elements
    (**T**ransition **R**adiation **T**racker - **TRT**)
- Axial Magnetic field 2 Tesla
- Hermetic coverage
- High granularity at $|\eta| < 2.5$
  - $\eta = \ln \tan \theta/2$, θ polar angle

Plan view of a quarter-section of the ID



SCIPP played a major role in the construction of the SCT.
Now contributing to the operations of the SCT and Pixels.

LHC Upgrade Plans

The LHC machine is still working to achieve design specifications:

- Critical superconducting splices must be fixed around the ring of magnets to allow operations at design energy of 14 TeV.
- Luminosity is slowly increasing towards design of 1×10^{34} $cm^{-2}s^{-1}$.
- Improvements to collimators likely needed to reach full luminosity.

We expect these targets to be reached by 2013-2014.

The LHC is then planning a series of upgrades:

- Increase luminosity to 2 or 3 x 10^{34} $cm^{-2}s^{-1}$ by roughly 2017.
- Increase luminosity to 5×10^{34} $cm^{-2}s^{-1}$ by roughly 2021.

Why? Increase "reach" for new physics.

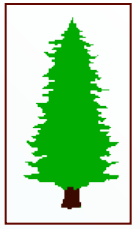
Would be nice to increase the CM energy but that requires all new magnets.

- This will have to wait for our grandchildren (~2030)

In proton-proton collisions, quark momentum distributions imply only rare events involve quarks near full CM energy.

Increasing luminosity increases the number of these rare events, consequently increasing the effective energy reach.

ATLAS Upgrade Plans



The ATLAS experiment is also planning several upgrades.

- Some to accommodate upgrades to the LHC.
- Some to improve present detector performance.

Phase I Upgrades:

- Add some small muon wheels that were staged out of original construction.
- Improve Trigger/Data-Acquisition system to original specification.
- Add new inner most pixel layer with smaller diameter beam pipe.
  - Named the “Insertable B Layer” (IBL).
  - Improves measurements of decay vertices and conversions.
  - Takes the place of present “B Layer” as it suffers radiation damage.

Phase II Upgrades:

- Replace/improve LAr on-detector electronics.
- Possibly improve muon on-detector electronics.
- New Trigger/Data-Acquisition hardware & software.
- Completely replace the Inner Detector!!!

Why Replace the Inner Detector

The increase in LHC luminosity to 5×10^{34} $cm^{-2}s^{-1}$ in roughly 2021 exceeds the design specifications of the present Inner Detector.

- The number of charged particles produced per event will exceed the ability of the TRT to track them (occupancy approaching 100%).
- The occupancy of the Pixels and SCT will require data transmission bandwidth in excess of present electronics.
- The radiation damage to Pixel and SCT sensors and electronics will exceed total dose and total fluence design specifications soon after the move to the higher luminosity.

Plans are to replace the full Inner Detector with an all silicon detector:

- 4-5 layers of Pixel and 4-5 Strip layers.

SCIPP's Contributions to Upgrades

SCIPP is participating in both the IBL & the later Inner Detector replacement.

For IBL:

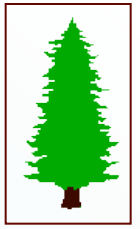
- Evaluation of possible sensor technologies.
- Prototyping and construction of electrical services.

For new Inner Detector:

- Evaluation of possible sensor technologies for Pixels and Strips.
- Studies of data transmission technologies inside the detector.
- Development of on-detector readout electronics.
- Simulation studies of detector performance and layout options.

Given the complexity and size of the Inner Detector replacement, development work has already started.

We will hear about several of these activities today.



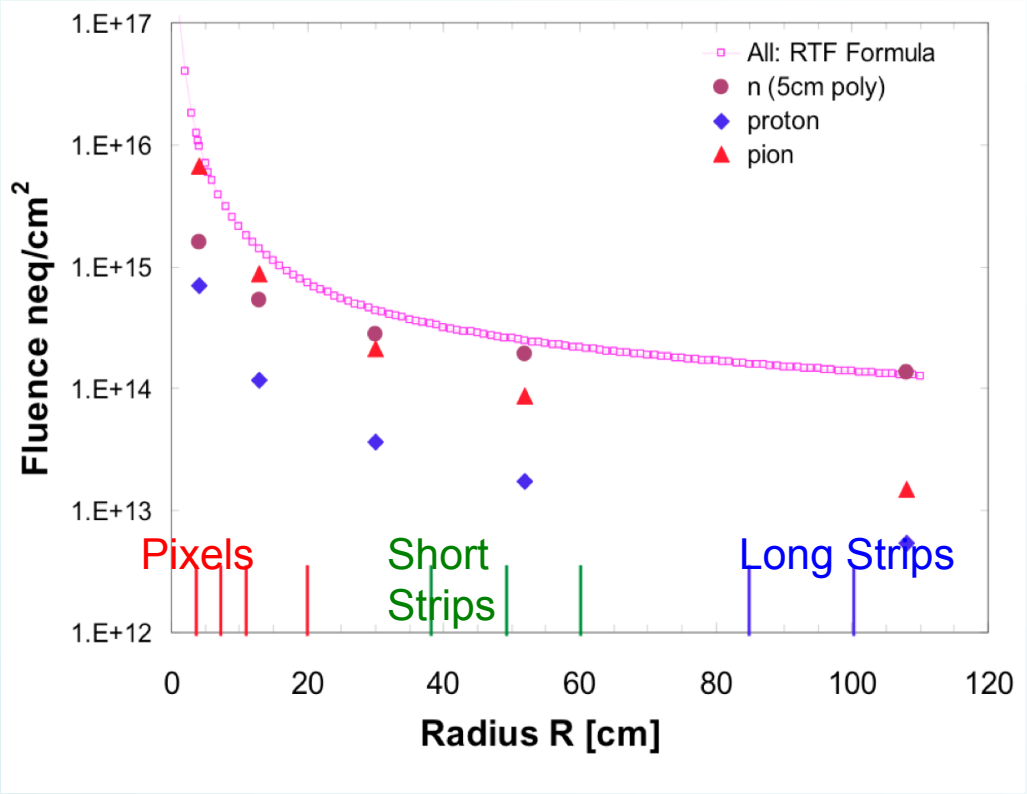
Sensor Work on IBL and SLHC

C. Betancourt, J. Wright, A. Bielecki, Z. Butko, C. Parker, N. Ptak, V. Fadeyev, H. F.-W. Sadrozinski

Motivation

- The planned high luminosity upgrade to the LHC, the sLHC, will have ~x10 luminosity increase, to 5×10^{34} cm^{-2} s^{-1}
- Will have to upgrade the tracker
- New system will have to reconstruct ~x10 higher track multiplicity =>
  - no TRT, increased scope of strip system,
  - increased importance and scope of the pixel system:
    - 4 (or 5) layers with ~x3 larger total area
    - ~x10 increase in fluences, up to 10^{16} n_{eq}/cm^2

- There is a natural dichotomy between high-radiation inner layers with small area and lower-radiation outer layer with large area.



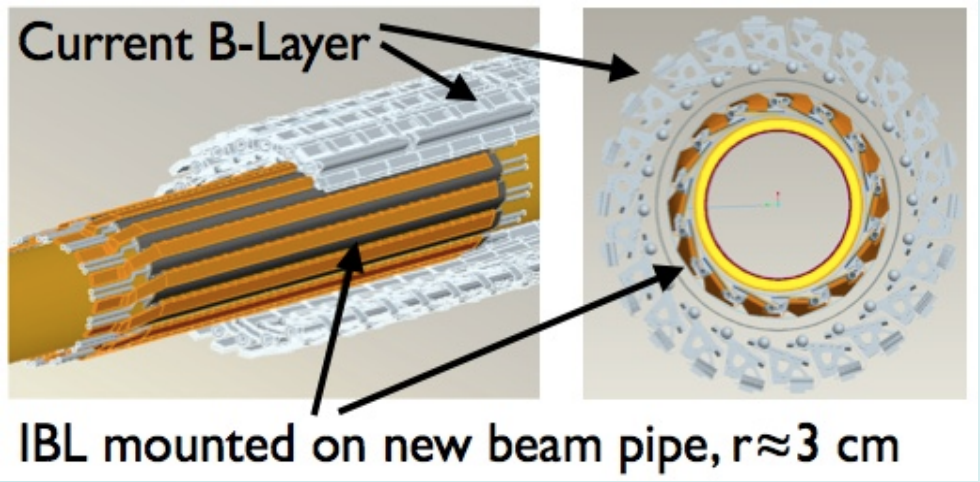
ATLAS Radiation Taskforce [ATL-GEN-2005-01] & H. Sadrozinski [IEEE NSS 2007]

Sensors	Design Fluences (2x safety factor included)
Inner Pixel	1-1.6x10^{16} neq/cm^2= 500 Mrad
Outer Pixel	3x10^{15} neq/cm^2 = 150 Mrad
Short Strips	1x10^{15} neq/cm^2 = 50 Mrad
Long Strips	4*10^{14} neq/cm^2 = 20 Mrad

N.B. Fluences and luminosity numbers are subject to Brown motion, but general picture is the same.

Insertable B-Layer (IBL)

- A special layer to be inserted in existing detector in ~2016, **before the full-tracker replacement**
- Both insurance against radiation effects, and enhancement of physics performance.
- Design for 5×10^{15} neq/cm^2, 250 Mrad, similar to outer layers of full tracker upgrade.
- Special spatial requirements (no shingling, minimal dead periphery).
- Approved by ATLAS Collaboration Board on Oct 8th.
- Abe is the leader of NSF-funded Multi-campus IBL work.



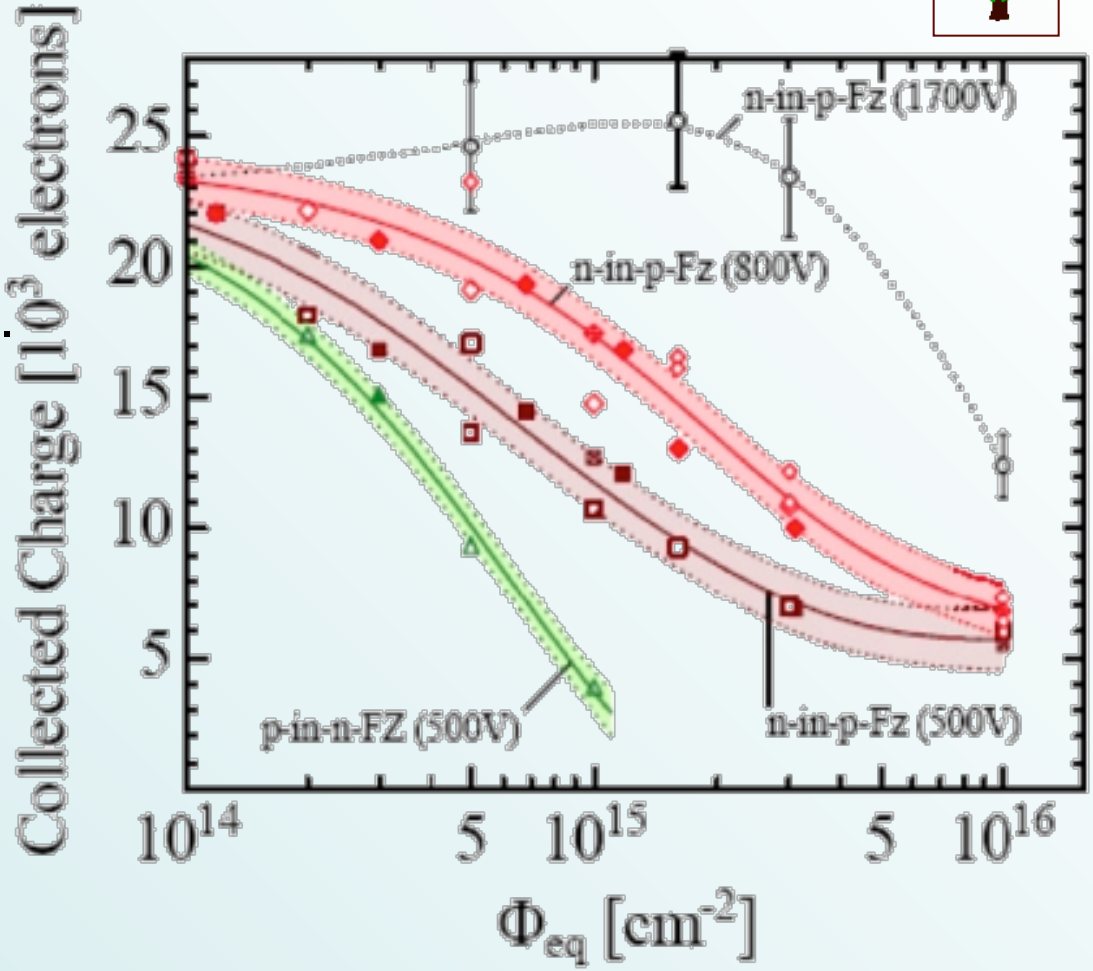
- Why a new Insertable B-Layer (IBL):
  - B-Layer suffers highest radiation damage
  - performance significantly degraded: *b*-tagging, impact parameter, pileup
  - add new layer:
    - closer to Interaction Point, smaller space, higher radiation...
    - 3 technologies under study: Diamond, new Planar, 3D

Sensor Type

The sensor type will change for strips: from current p-on-n to n-on-p.

For pixel system, it's an open question. The contenders are:

- Diamond sensors
- 3D sensors
- Planar pixel sensors:
  - n-on-n (more rad-hard)
  - n-on-p (cheaper single-sided processing)



Collected charge as a function of 1MeV neutron-equivalent fluence (Φ_{eq}).
[From Hartmut's SPIE article: DOI: 10.1117/2.1201010.003272]

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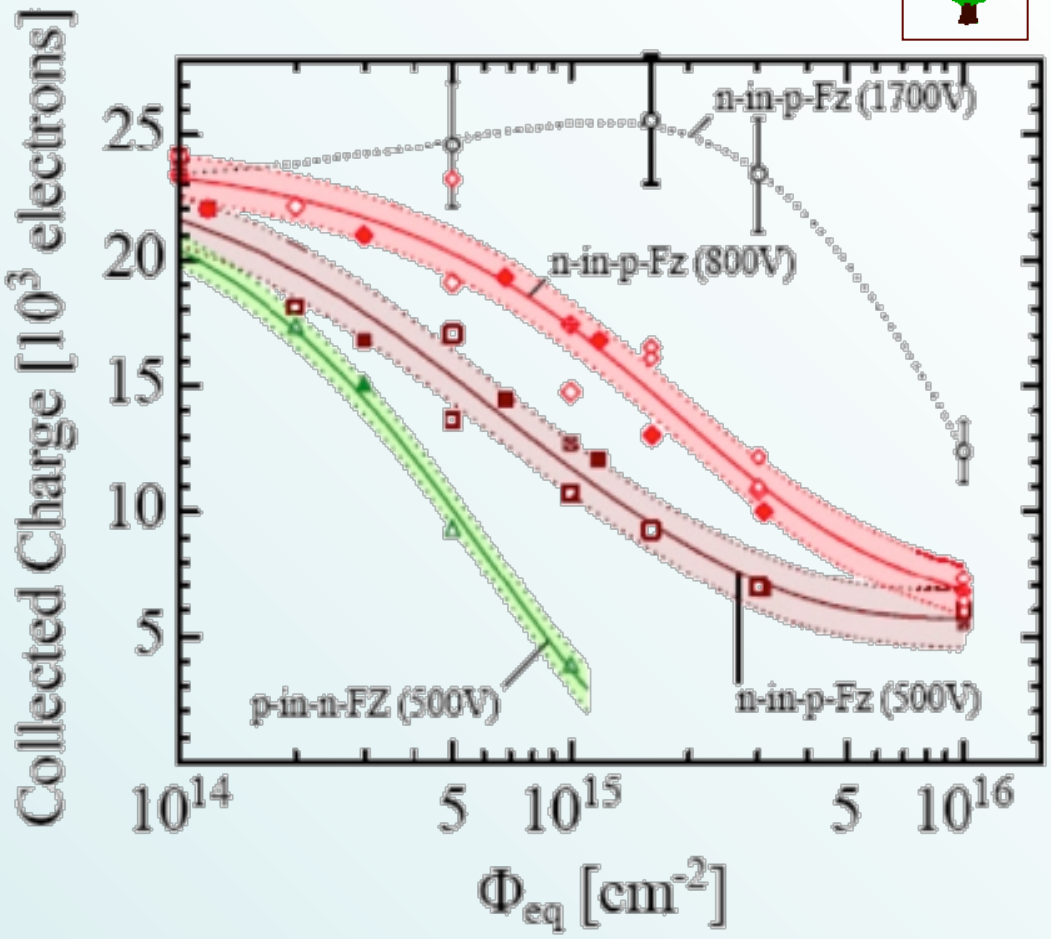

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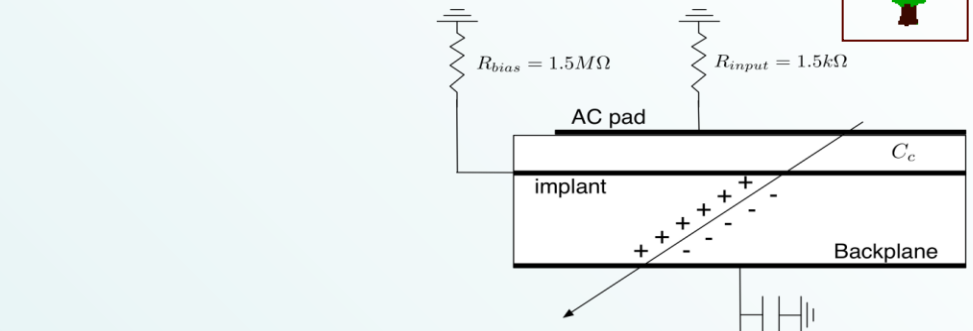
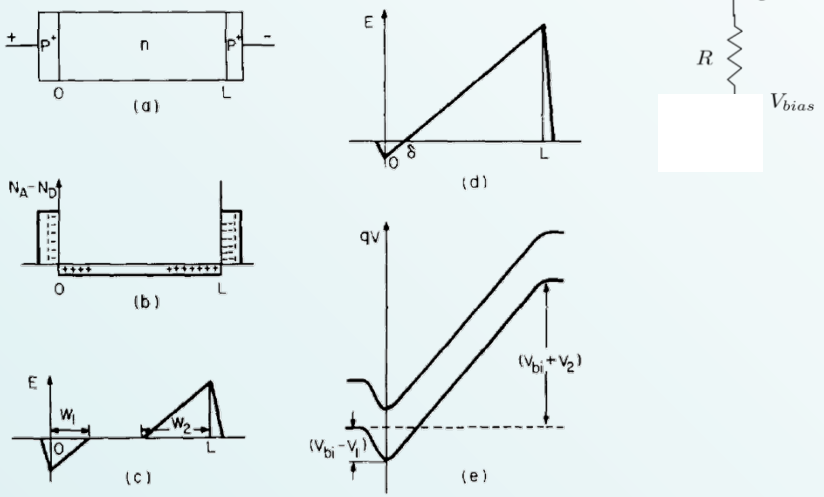
Strips

The sensor type is chosen. Recent work is on punch-through protection.

Damage from Beam Losses to AC-coupled SSD





- ALEPH at LEP observed break-down of the coupling capacitors on AC-coupled SSD in a beam accident. The Al readout trace of AC coupled sensors are held at ground by the readout ASIC.
- We proposed that this was due to the breakdown of the field inside the sensor when the deposited charge made the sensor conductive. At that point, the bias voltage can reach into the sensor bulk and can impart large voltages to the implants.
- To check this, we used IR lasers to mimic the beam loss and we indeed observed large voltages on the implants

T. Dubbs et al., IEEE Trans. Nuclear Science 47, 2000:1902 – 1906.

- The reach-through (punch-through) effect was considered an elegant and effective way to limit the voltages on the implants. Special punch-through protection (PTP) structure can be designed where the geometrical layout determines the voltage limits on the implants.

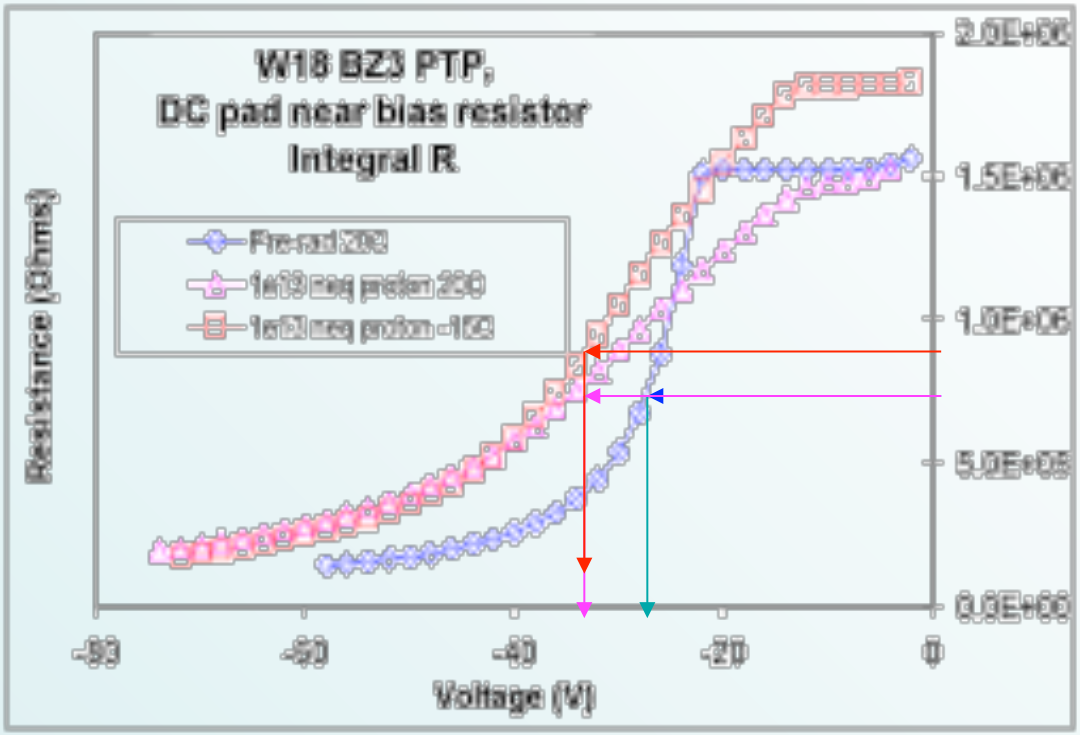
J. Ellison et al., IEEE Trans. Nuclear Science, 36, 1989: 267 - 271.

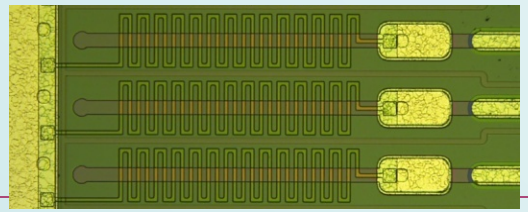
- PTP structures were implemented in the p-on-n SCT sensors.
- But the PTP structure in SCT sensors were shown not to guarantee protection against large voltages across the coupling capacitors when IR laser pulses were used.

K. Hara, et al., Nucl. Instr. and Meth. A 541 (2005) p. 15-20.

PTP Structure Effectiveness

- The effectiveness of PTP structures is determined in DC i-V measurements between the strip and the bias ring. One measures the “integral” effective resistance R_{eff}, which is the bias resistor R_{bias} in parallel to the PTP resistor R_{PTP}.
- The measure of the effectiveness of the PTP structure is the punch-through voltage V_{PT} , defined as the voltage at which
  $R_{PTP} = R_{bias}$, i.e. R_{eff}, = 0.5* R_{bias} .
- The PT voltage V_{PT} was measured to be a few 10’s of Volt, which gives a large safety margin to the specification that the coupling capacitors are tested to hold off 100V.

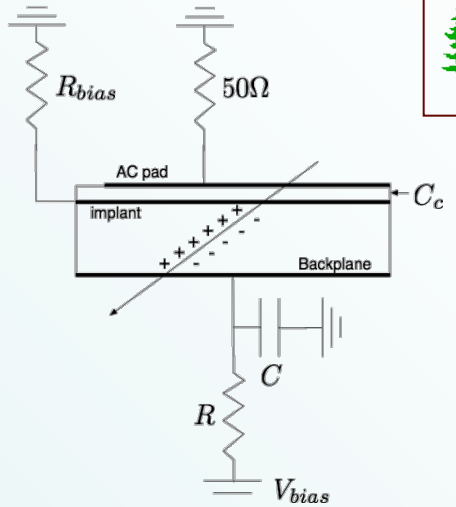




Note that this a n-on-p HPK mini
with common p-stop and NO explicit PTP structure.
The distance n-implant to n-bias ring is 70 μm.
Effect radiation dependent,
but independent of leakage current (or T).

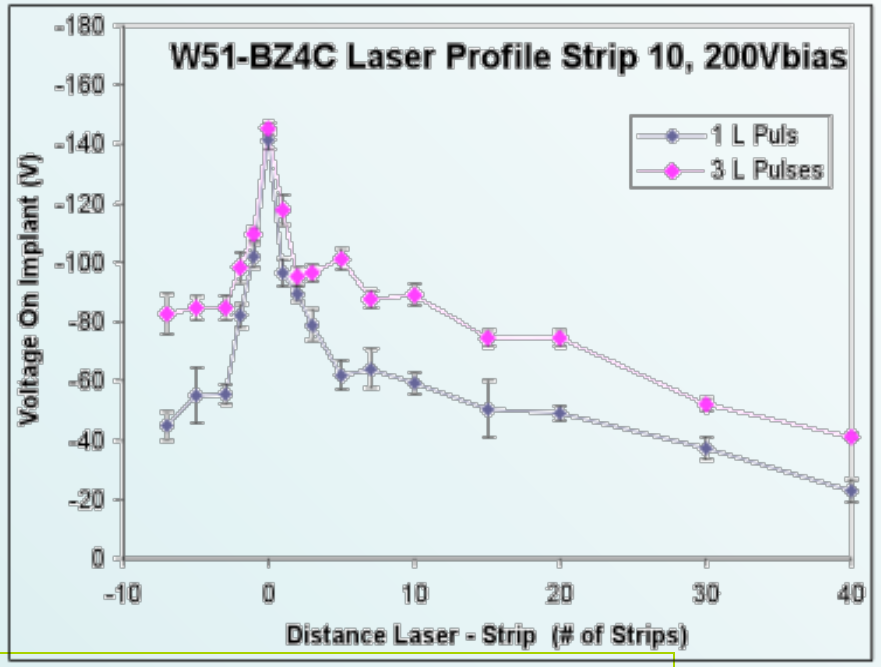
Puzzle #1:
The Effectiveness of the punch-through-protection (PTP) has been shown with DC measurements, yet they do not protect against dynamic charge pulses.

Testing Large Implant Voltages with Laser



• Bias ring is held to ground, and the voltage on a DC pad and/or AC pad are read out via a high impedance voltage divider into pico-probe or digital scope.
• DC pad reflects biasing of strips, AC pad reflects instantaneous collected charge (~ depleted region)

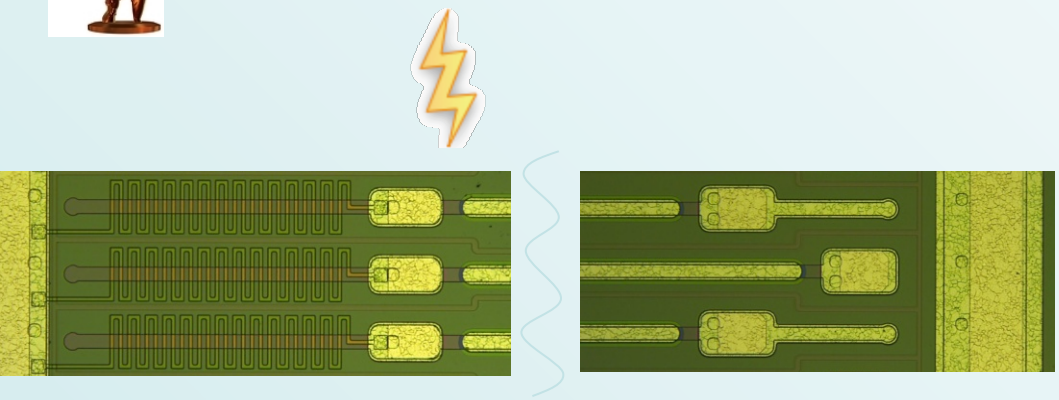
• Alessi LY1 cutting laser (1064 nm) deposits large amounts of charge inside the detector which collapses the field
(>10^{10} e/h pairs ~ 10^6 MIPs ~ 1 Rad / pulse).
• Intensity given by number of laser triggers ~ 4 μsec apart (we used up to 3).
• Laser spot ~ 10 μm, but large DC voltages extend over few mm.
• Peak voltage independent of laser intensity.



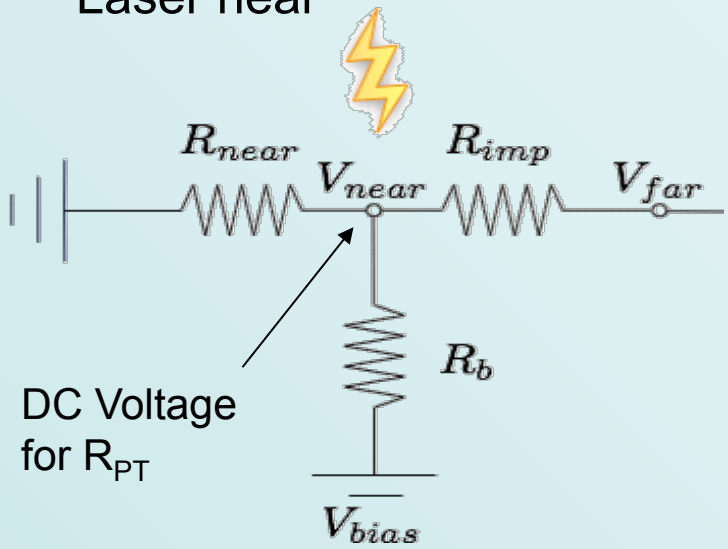
Observation #1: Voltages are large, comparable to bias voltage.
→ the PTP structures must have a finite resistance to ground after punch-through!

***R_{PT}* is the important parameter, NOT *V_{PT}*!**

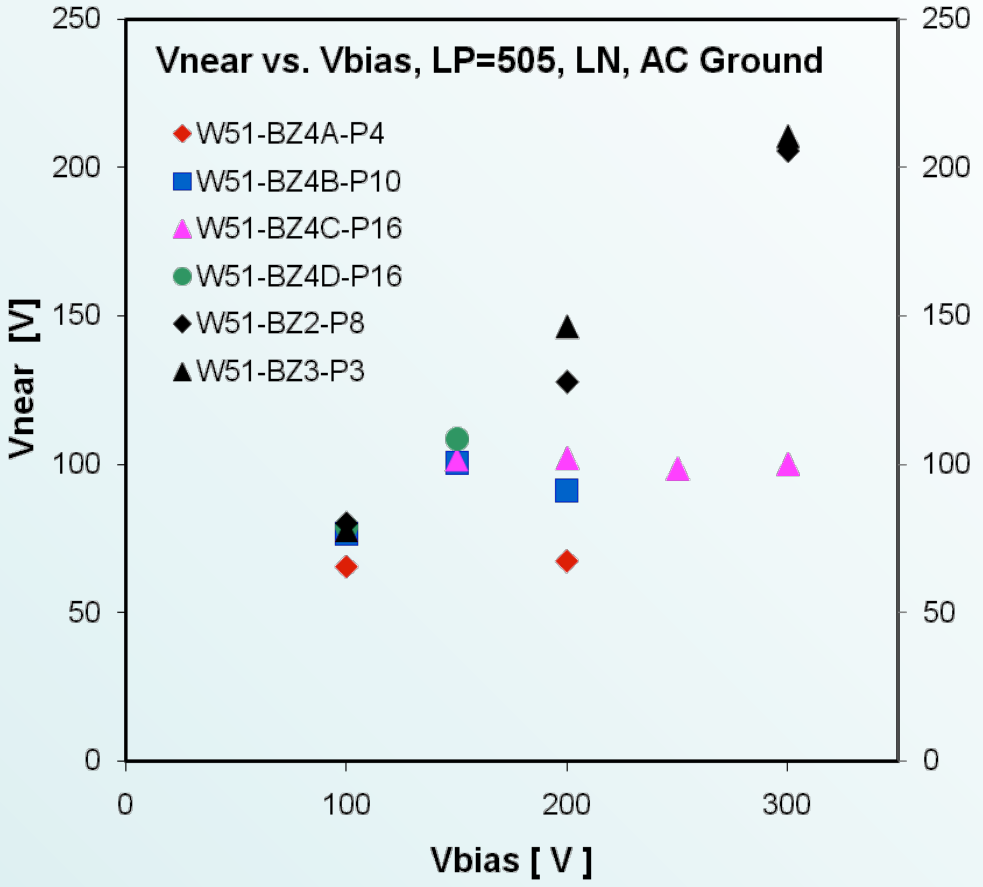
Implant voltages near R_{PT} vs. Bias



Laser near



DC Voltage for R_{PT}



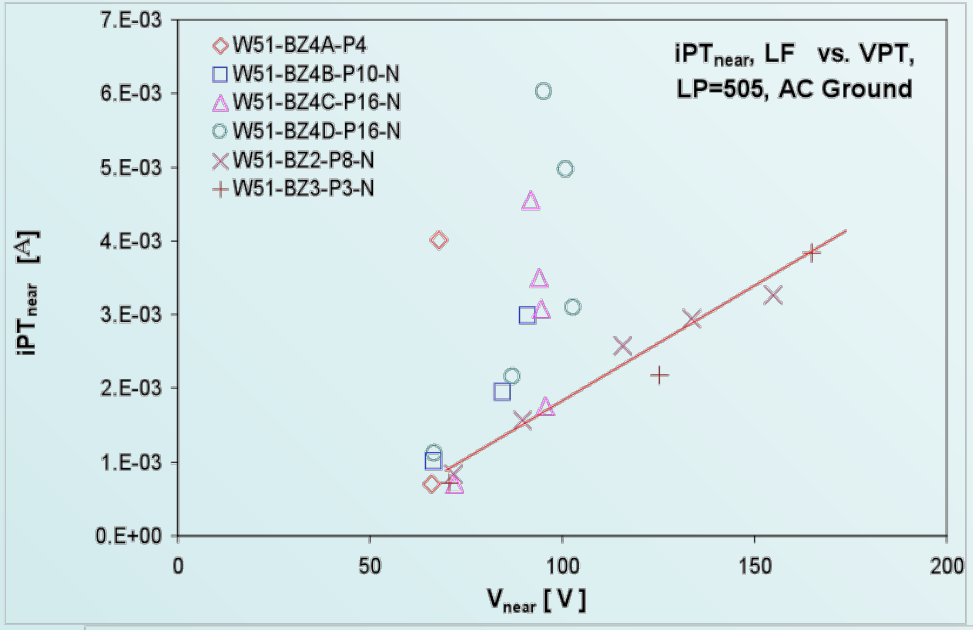
Observation #2: At high bias voltages, for some PTP structures $V_{implant}$ saturates at different values, but always at V >> V_{PT}.

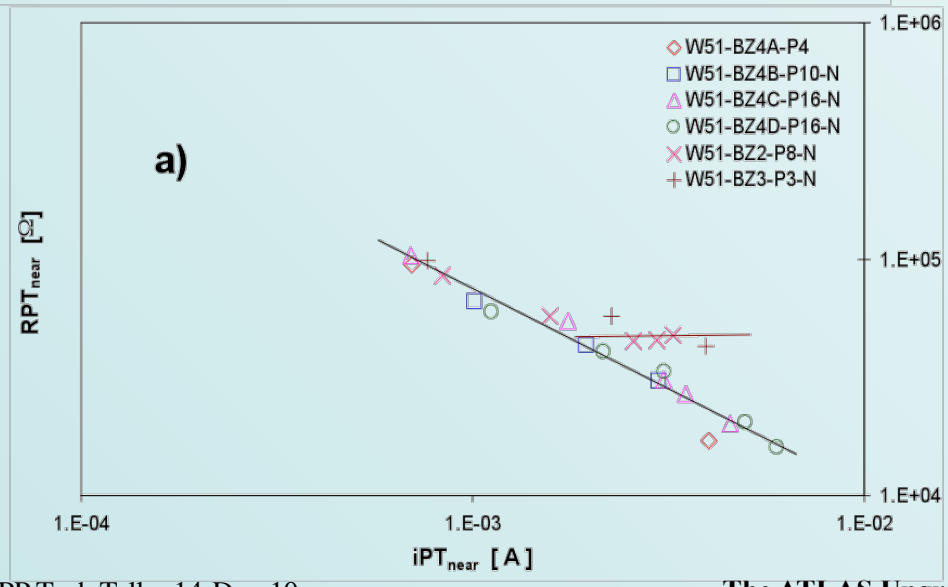
Can this be explained by the DC voltage dependence of R_{PT} ?

Space-Charge Limitation in PTP Structures

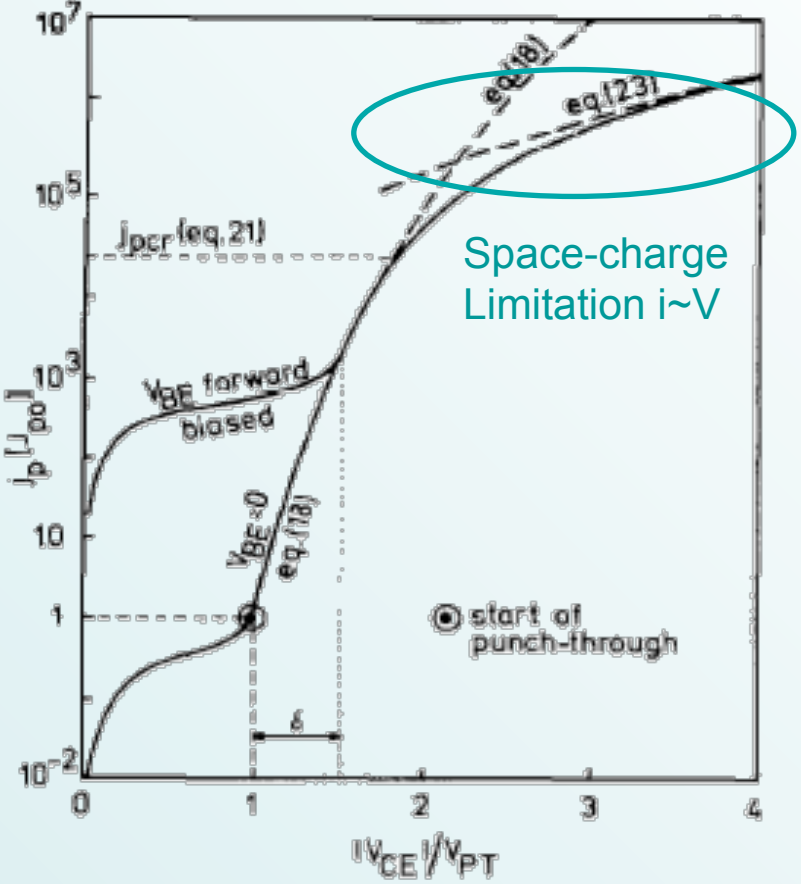
Literature:

- J.I. Chu, G. Persky, and S.M. Sze, J. Appl. Phys., Vol. 43, No.8, August 1972
- J. Lohstroh et al. Solid-State Electronics, Vol. 24, No. 9, pp. 805-814, 1981



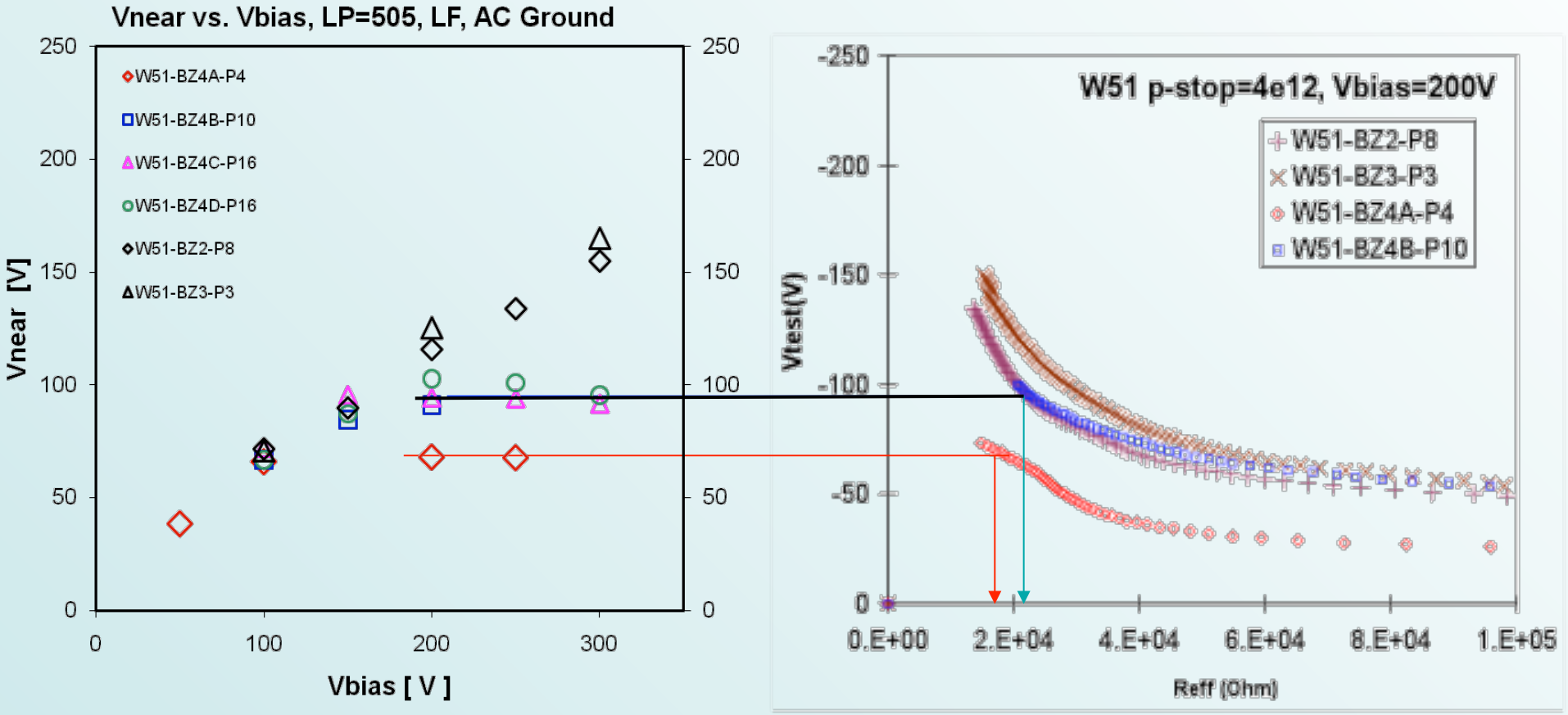


I_{PT} vs. V_{PT}



I –V curve indicates space-charge limited region at high voltages, when $R_{min} = L^2 / (2 \varepsilon v_s A)$ [for a planar sandwich geometry].
A fundamental limit of the PTP technique?

Implant Voltages with Laser vs DC PTP

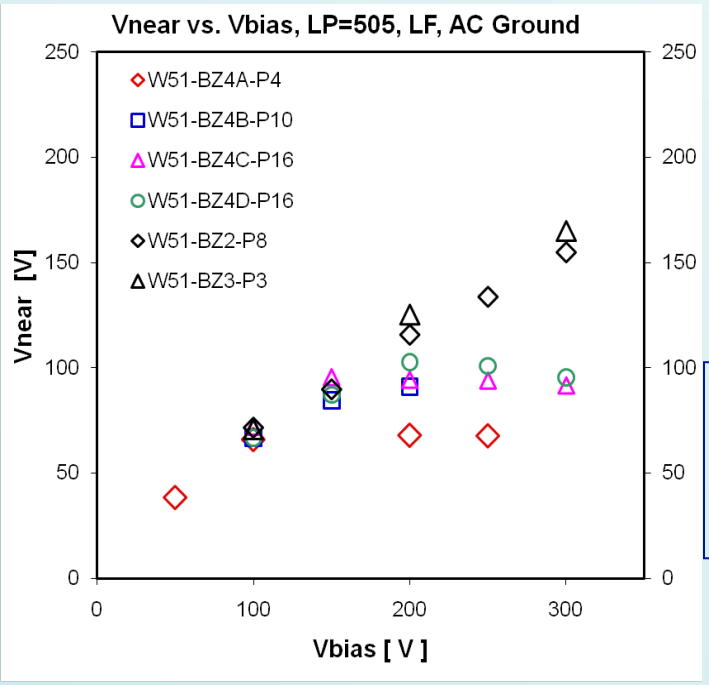


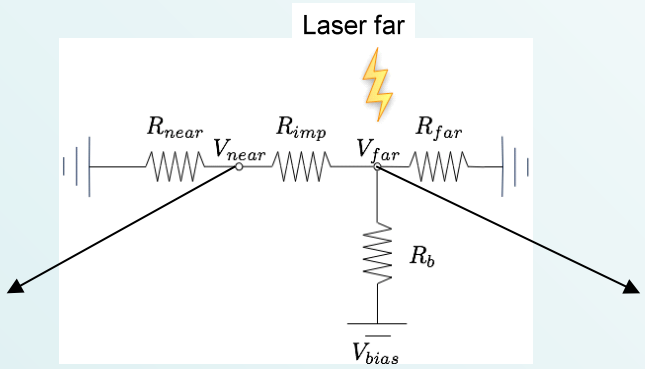
Observation #4:

Voltage on implant saturates when $R_{PT} \approx 20\ k\Omega$

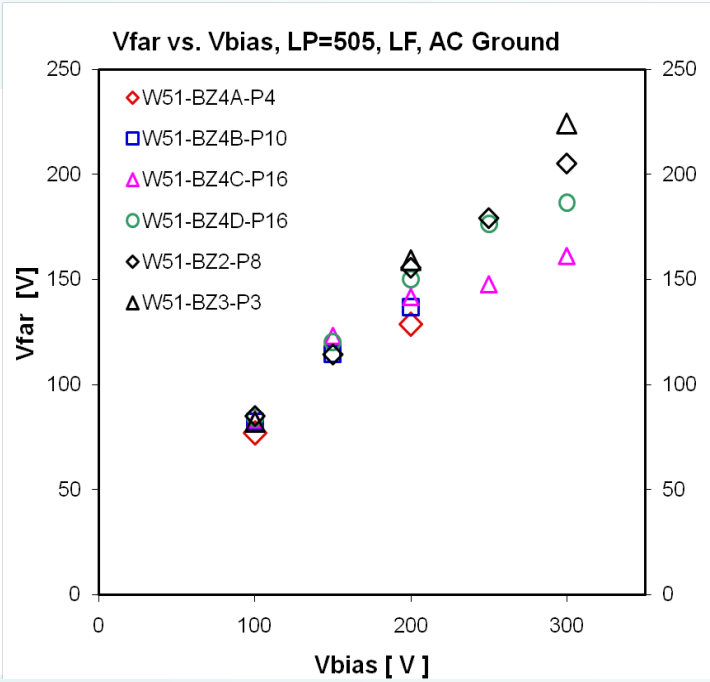
Effect of Finite Implant Resistance R_{imp}

Fire laser at the far end of the 1 cm strip, measure both V_{near} and V_{far}





$V_{far} > V_{near}$
No saturation
PTP structure not effective



Observation #5:

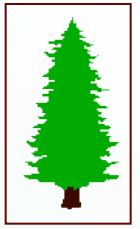
Implant Voltages do not saturate at high bias voltages, if finite implant resistance R_{imp} isolates PTP structure from breakdown region.

Conclusions

- Some PTP structures help, but still see large voltages with the laser simulation.
- The observations are consistent with having 4 key resistors of the same magnitude:

  R_{PTP}(near), R_{PTP}(far), R_{bulk} , $R_{implant}$.
- $R_{implant}$ is very important: the current value, ~15 kΩ/cm, can effectively isolate the collapsed field from the PTP structure, increasing the implant voltages by 100's of volts.

  => need low $R_{implant}$!
- The changes with radiation damage, different strip isolation schemes (p-stop, p-spray, and dozes), and effect of the R-C biasing network at the backplane will be studied next.



Pixels

We are participating in Planar Pixel work.

- Current studies are on “slim edges”. Mostly for n-on-p, although some results are relevant for n-on-n.
- Past attempts on “temporary interconnect”. Technically still possible in my opinion. Other interests of co-creators, and possibly, FE-I4 performance might call this off.

We are getting a lot of mileage by collaborating with people with access to the sensor producers and nano-fabrication facilities:

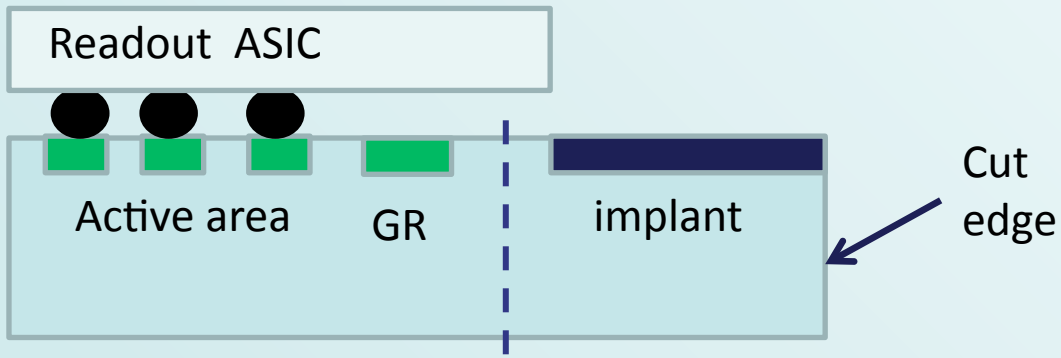
- ATLAS collaborators (HPK, Micron, CIS)
- N…
- VTT and edgeless sensors

Possible collaboration with DISCO.

Motivation for Edge Studies

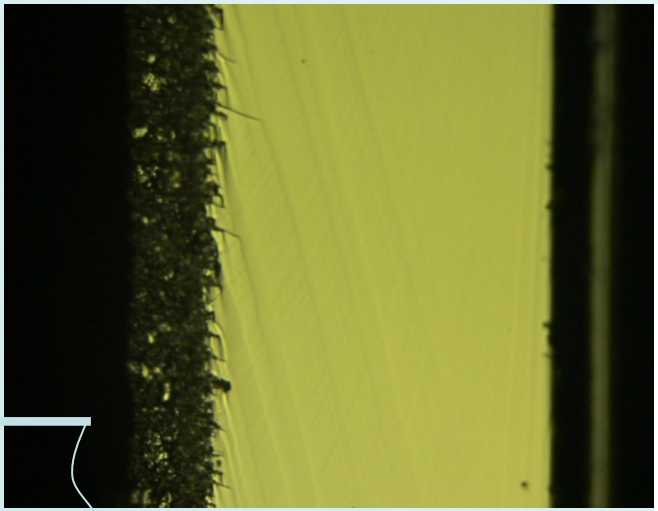
- "Slim" edges, if work, lead to a larger fraction of active sensor area.

- Investigation of necessity of implant on top surface of n-on-p.
  - Proximity of HV and readout ASICs as a system engineering concern.
  - Possibly higher pre-rad leakage current, since the field gradient is not confined to the bulk of silicon.

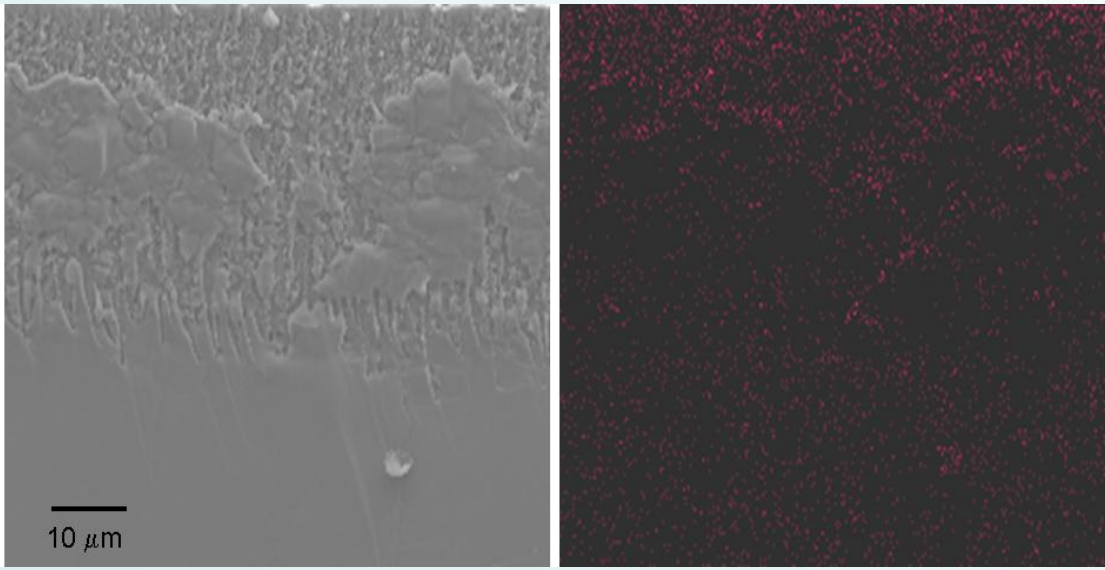


Scribe-and-Cleave Method

- Two-step process:
  - Scribe the surface to create a “trench”. Done with E-Series laser from Oxford Laser Systems at NRL.
  - Break off the rest of the bulk.
- The trench is roughly aligned with the lattice orientation.
- In practice, the cleaved edge will still have some imperfections, although it is hard to detect sometimes.



Edge illumination
of the cleaved surface

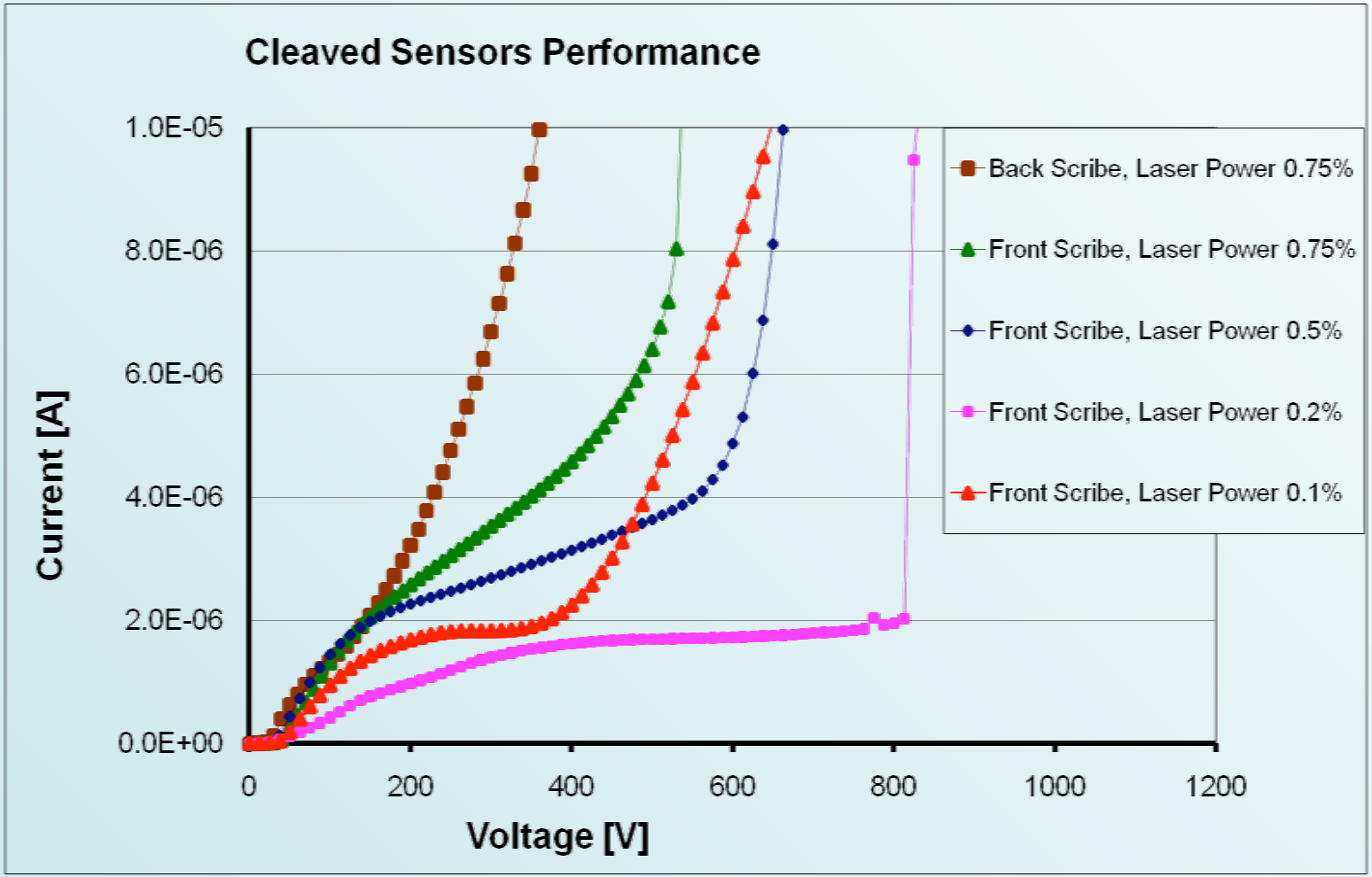


Oxygen distribution with EDX imaging at NRL

Laser scribe/incision

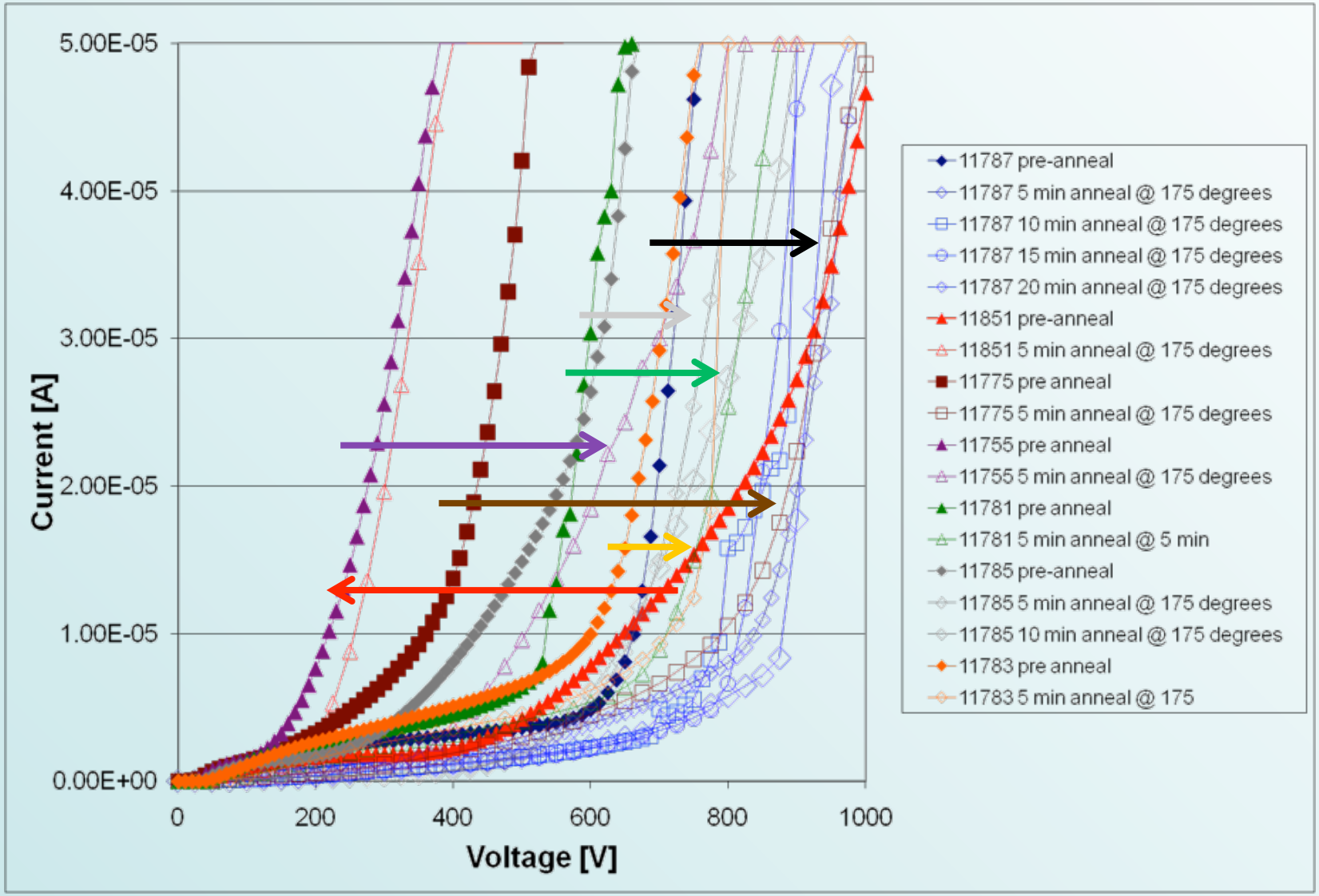
Process Optimization

- Optimization with n-type HPK sensor. Scribe at 100 um from the guard ring.
- Front-side scribe seems to be preferential to back-side one (field geometry?) Lower laser power is preferential.



Post-cleaving Treatments (n-type)

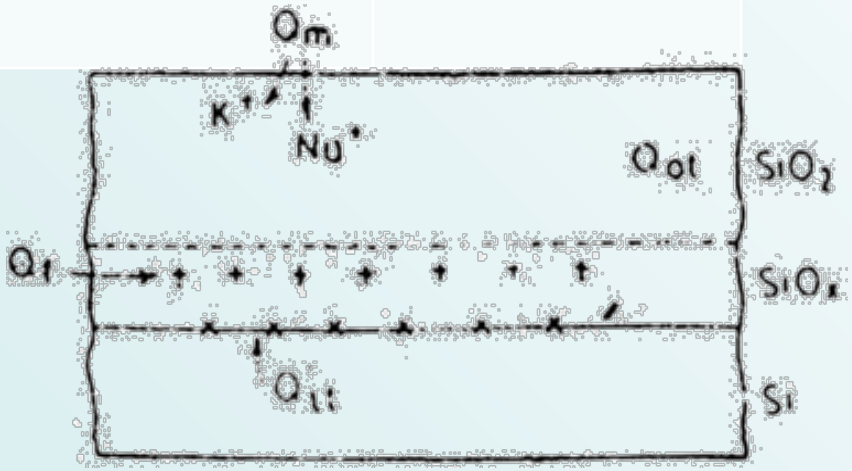
- Attempted to treat cleaved sensors with UV irradiation and high-temperature “annealing”. High-T treatment results:



Summary of scribe-and-cleave evaluations

Manufacturer	Type	Breakdown voltage	Thermocycling change	Comments
CIS, 8 GR	P-type	20 V	Insignificant	
HPK, 1 GR	N-type	100s of V	Significant	
HPK, 1 GR	P-type	Few V	Worsen ?	Difficult to break.
Micron, 8 GR	N-type	10-35 V		
Micron, 8 GR	P-type	20-100 V	No change	

Bulk type difference:
likely due to the “native oxide”
and it’s built-in charge polarity.

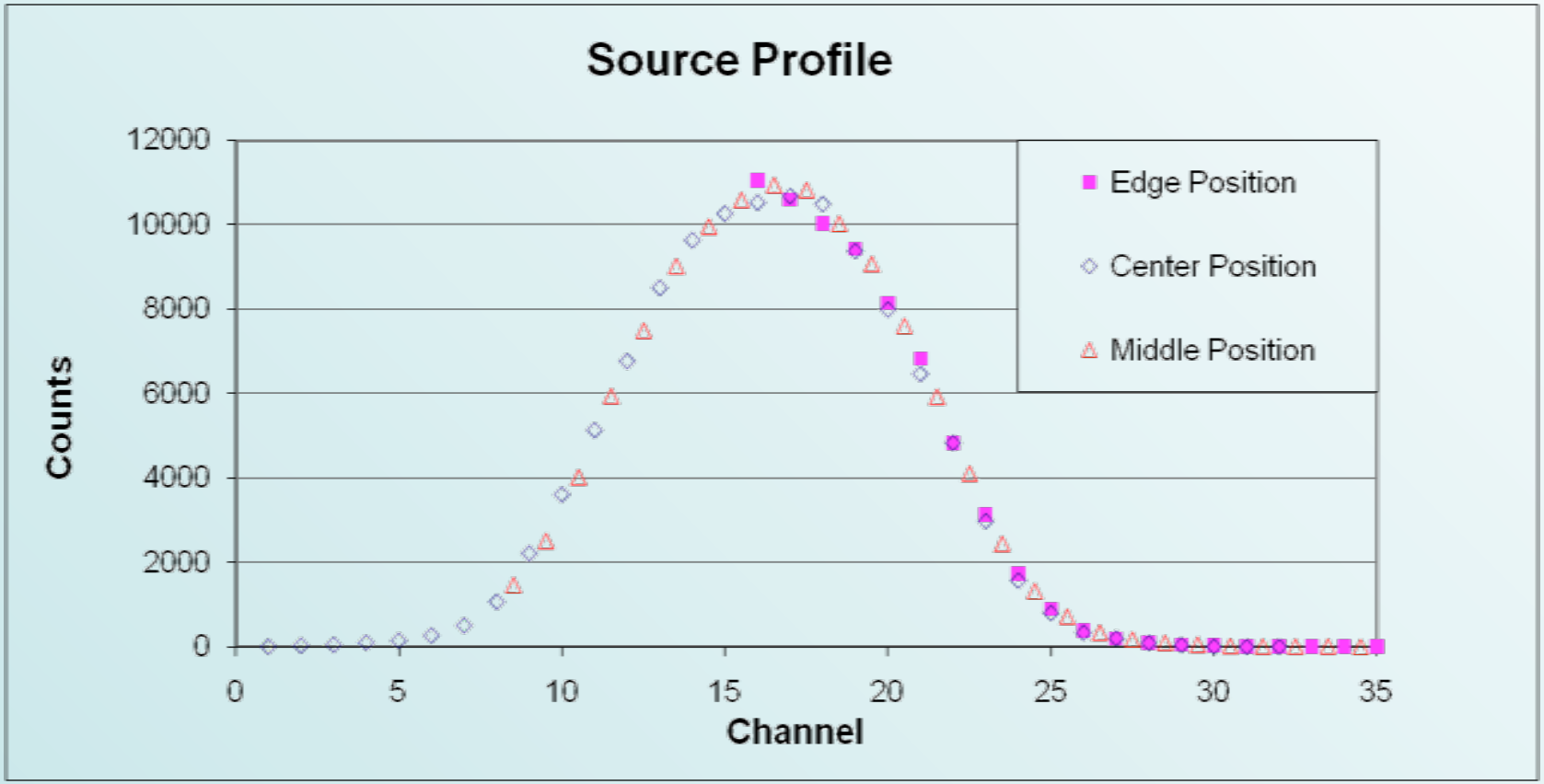


Charge Collection Efficiency (n-type)

- Used existing setup with source and scintillator-based coincidence trigger to check relative collection efficiency.
- Used one of the cleaved n-type sensors (HPK, 1 GR).

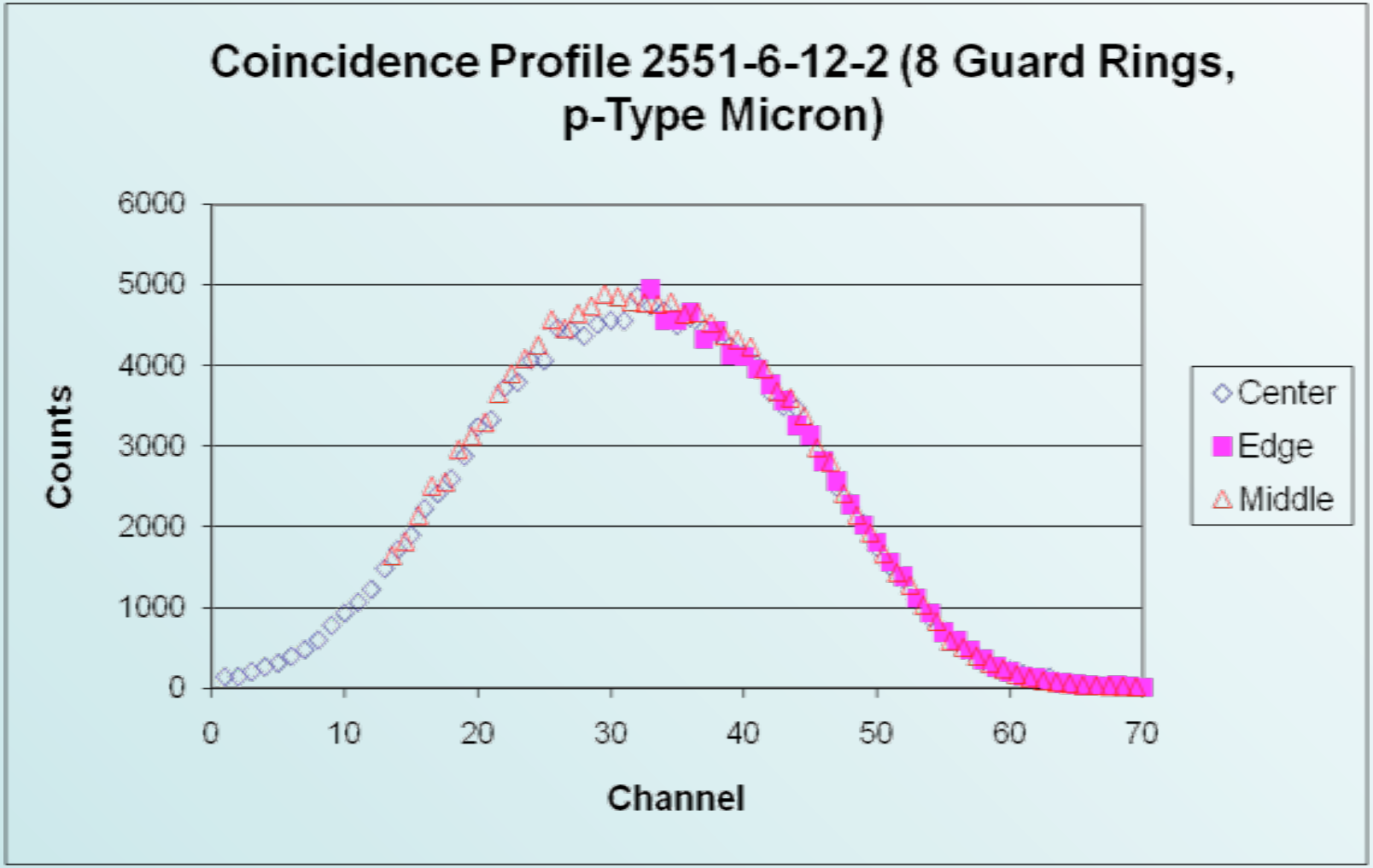
D = 180 um between bias ring and the edge.

- Several runs with shifted sensor position wrt source-scintillator axis.
- See a consistent efficiency of the edge strips (within 5%).



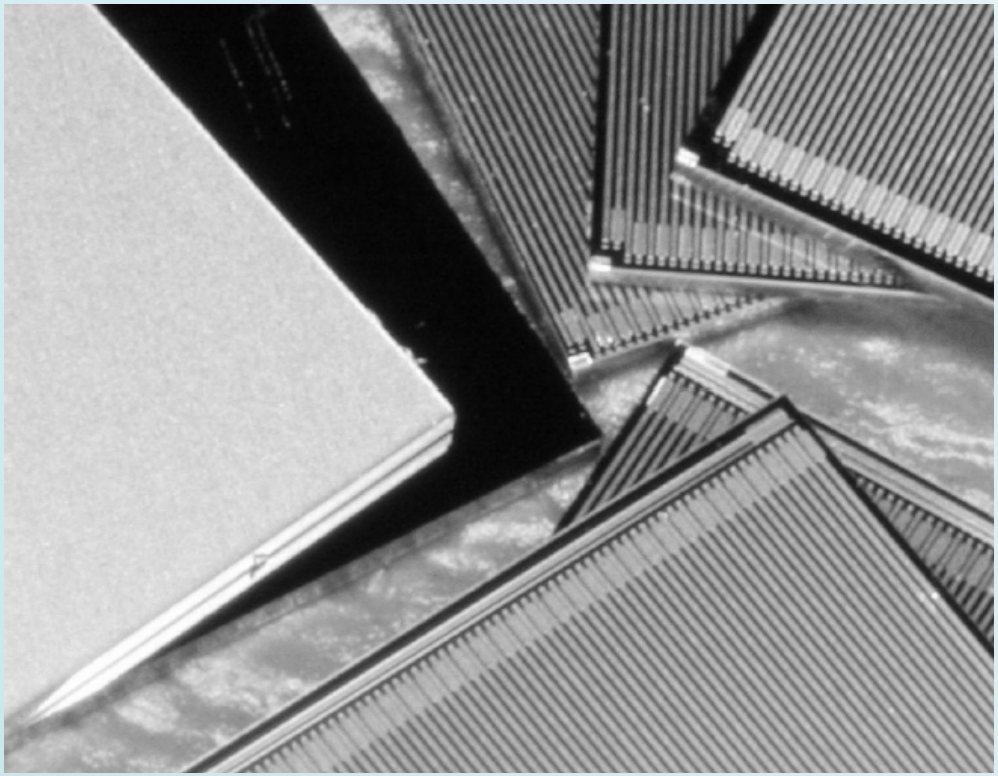
Charge Collection Efficiency (p-type)

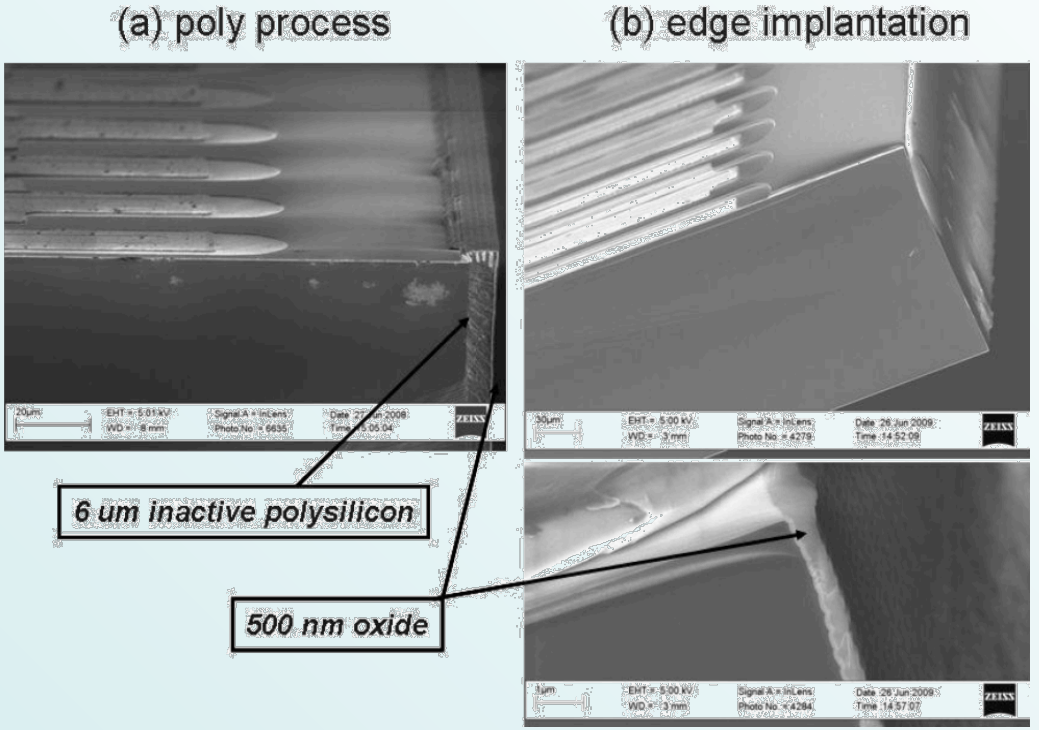
- Similar study with p-type sensor which has been laser-cut just outside 8th guard ring (no cleaving).
- D ~550 um between bias ring and the edge.



Edgeless Sensors from VTT

- Collaboration with Juha Kalliopuska
- Their main motivation is for tiling Medipix sensors. Side ion implantation for making active eges.
- Also produced strip test sensors on the same wafers.
- Initial sensors are DC-coupled, harder to work with than the usual AC-coupled ones. In process of checking IV/CV/charge collection with special hand-made biasing schemes.

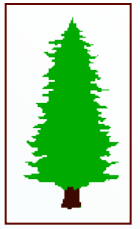




Conclusions

• Reasonable performance with slim edges was only demonstrated for n-type sensors (HPK GLAST).
• This is also the only type for which thermocycling improved the performance substantially, probably due to oxide formation.
=> Very simple process of making slim edges, compared to e.g. trench etching.
• Never got p-type sensors to work well. This can argue for inherently different properties of p-type surface than n-type surface. A need for a different post-processing of the p-type cleaved surface?
• The charge collection efficiency is preserved, within a few percent, when the slim edge distance is in the range of 200-500 um.

• Current work is specifically on trying to make resistive edges with p-type sensors (very recent, no results yet).



Data Transmission Studies

M. Norgren, R. Huang, E. Spencer, J. Nielsen, V. Fadeyev

Requirements

ATLAS upgrade will have higher data rate from more modules for both strips and pixels => need data serialization => need local (stave) data transfer.

Stave data transfer rates expected:
strips – 160 Mbps for data, 80 Mbps for clocks and commands.
pixels – less defined, strong radial dependence.

System TF bandwidth estimates

- **At 2X { 100KHz L1, 3.3μs latency, 400 int./50ns }**

[From M. Garcia-Sciveres's talk at AUW 2009 at CERN.]

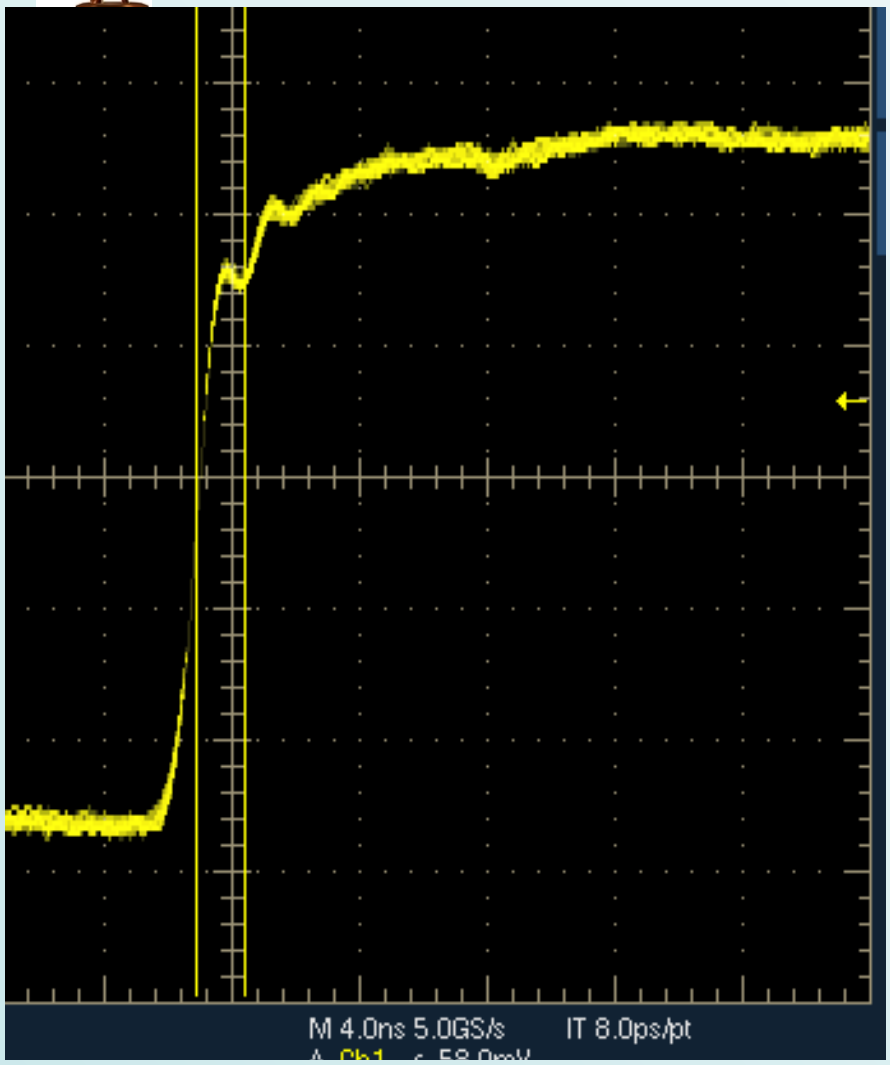
R (cm)	comp. firing per cm^2 per BX	Required BW per chip (Mb/s) (analog / binary)	Stave end data volume (Gb/s) (analog / binary)	Min. number of GBTX	Data loss x10^{-4}
3.7	60.0	749 / 454	12.0 / 7.3	3	tbd
7.0	18.4	230 / 140	5.5 / 3.4	2	tbd
16	6.6	75 / 58	**4.8** / 3.6	2	19
20	3.9	42 / 32	**2.7** / 2.1	1	10
25	1.8	19 / 14.5	**1.2** / 0.9	1	5

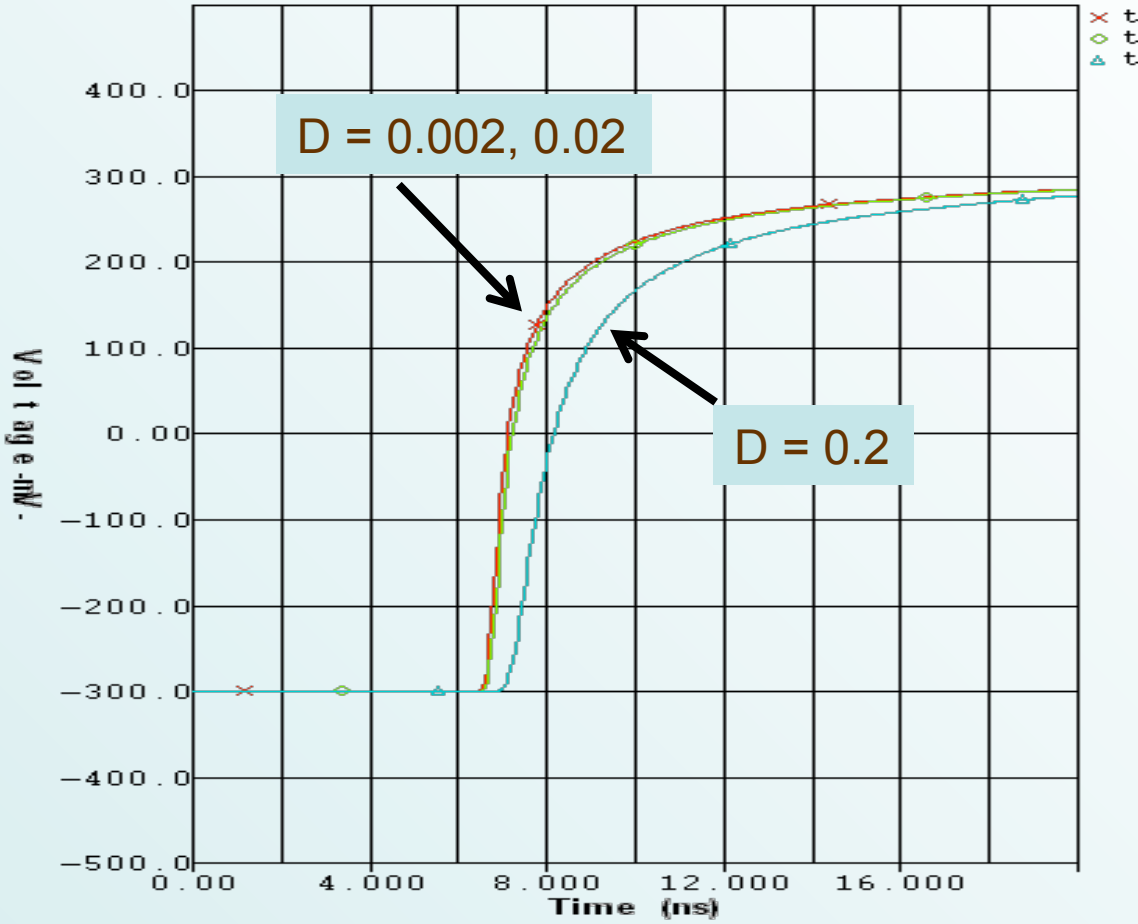
Methods

Need cables, drivers and receivers, as realistic as possible:

- Got cables from Carl as a part of stave prototype program. The latest one was made at Oxford.
- Initially standard LVDS drivers, i=3.5 mA (=> 350 mV amplitude for 100 Ohm load).
- The end-of-stave serializer technology is likely to be GBT for strips, which declared SLVS standard as its choice:
  - Made our own LVDS/SLVS chip. Designed by Joel deWitt.
  - Got some of CERN-made LVDS/SLVS chips. Initially they did not work. Got 2nd batch, about to test these.
- Test equipment:
  - High-speed oscilloscope and “eye diagrams”. Roughly speaking, tests that 0 != 1. Signal level and jitter. Usually limited number of samples.
  - Our own FPGA-based bit error rate tester (BERT), verifies signal pattern, optionally as a function of clock phase.

Simulations

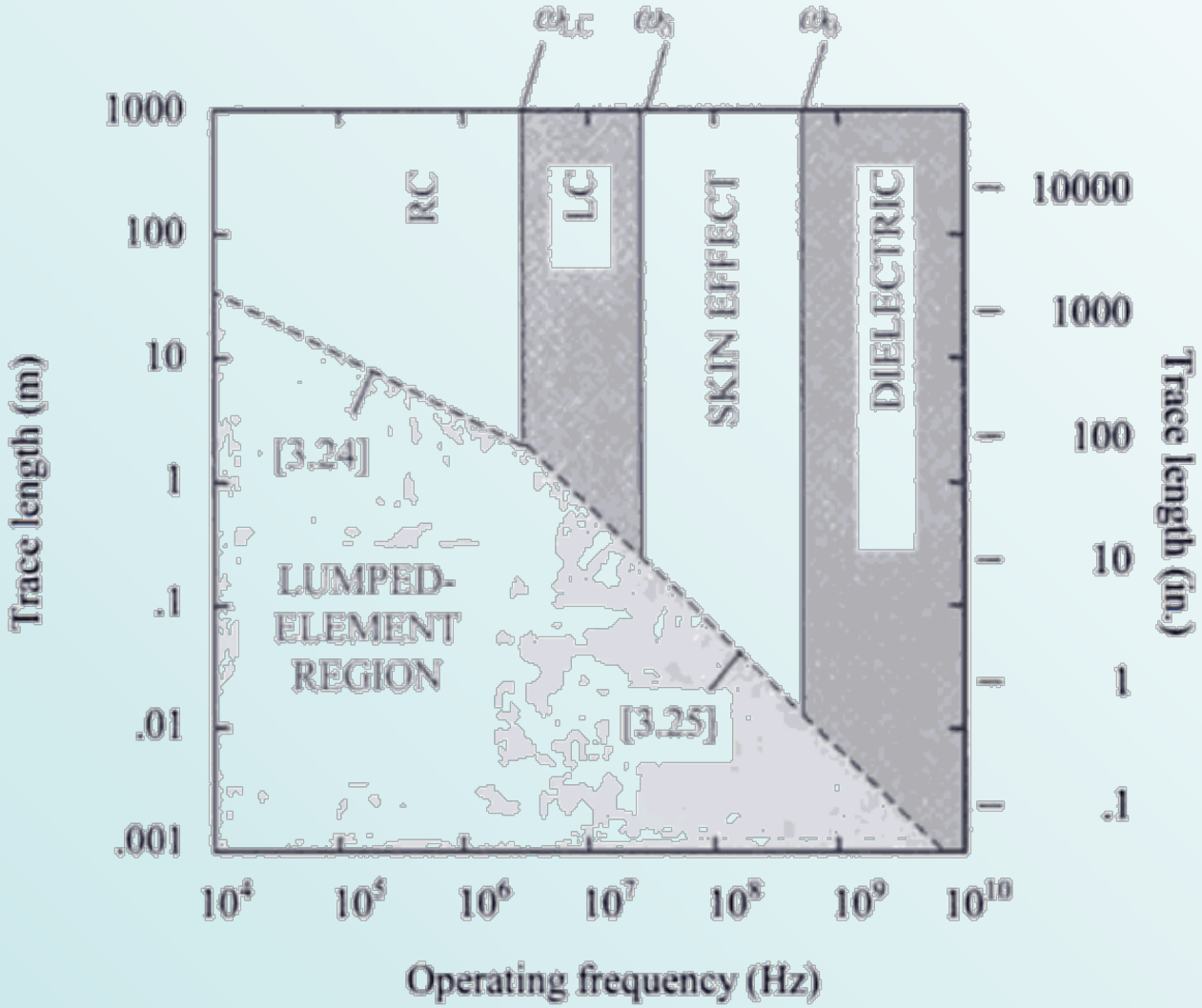




HyperLynx, one of the industry-standard packages from Mentor Graphics. 2D Field solver, works off a PCB/cable layout.

Simulated with loss tangent D = 0.002, 0.02 (standard for FR4), 0.2. Only see a significant difference in the latter (extreme) case. => Most of the “slow rise” effect due to Skin effect?

Simulations



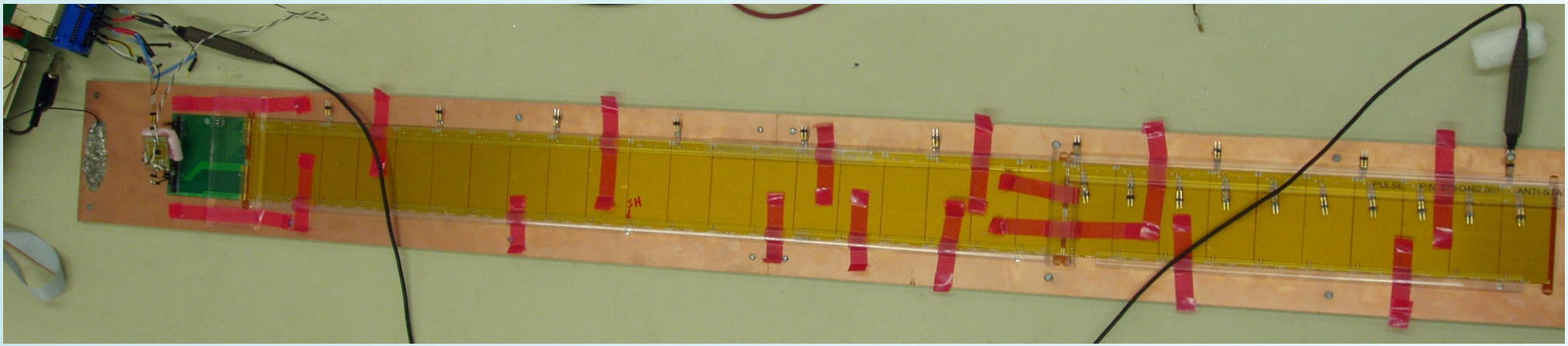
ıre 3.2—Performance regions for a 150-µm (6-mil), 50-Ω, FR-4 stripline.

From "**High-speed Signal Propagation**" by Howard W. Johnson, Martin Graham

$$Z = \sqrt{\frac{j\omega L + R}{j\omega C}}$$

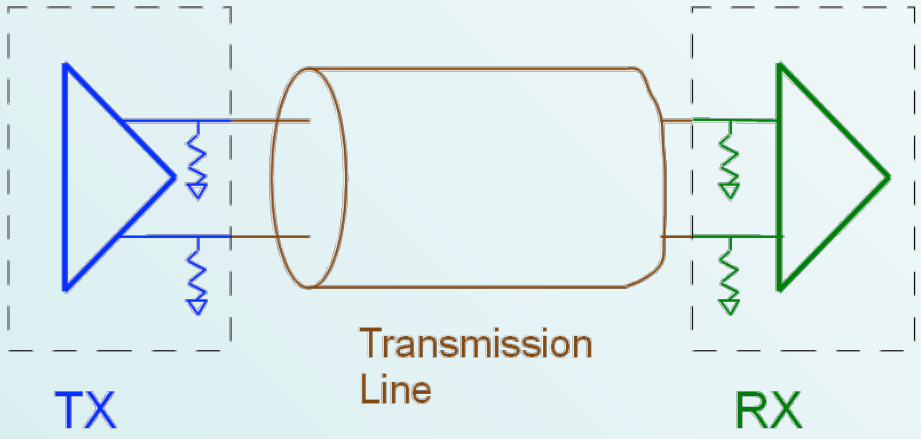
Introduction

- We are testing data transmission on long flexible cables in a stave-like environment: multi-drop clk/command broadcast to hybrids and point-to-point return lines. Want to find limits of performance of this architecture.
- Have previously shown that with LVDS signaling point-to-point links work well up to 320 Mbps, and multi-drop works up to 160 Mbps for a group of 10 loads of 2 pF.
- This was done with an old version of the stave cable:



LVDS and SLVS

- LVDS was introduced in 1994 by National Semiconductor:
  - 1.2 V common mode, 3.5 mA current across 100 Ohm termination => 350 mV differential signal.
  - Wide adoption in late 1990s for computer communications.
- SLVS was standardized in 2001 (JESD8-13).
  - Intended as high-frequency protocol scalable with lower power supply voltages of future technologies.
  - "SLVS-400": driver V. source of 0.8 V, 400 mV diff. signal, *impedance matching for both driver and receiver*.
  - Rare use in industry so far.



SLVS Implementations

- A “typical” SLVS implementation is the “SLVS-200”:
  - Common mode of 200 mV, diff. signal of 200 mV.
  - Source termination to GND and diff termination.

- Nokia scheme (NRC-TR-2006-007) (either blue or green switches are closed)

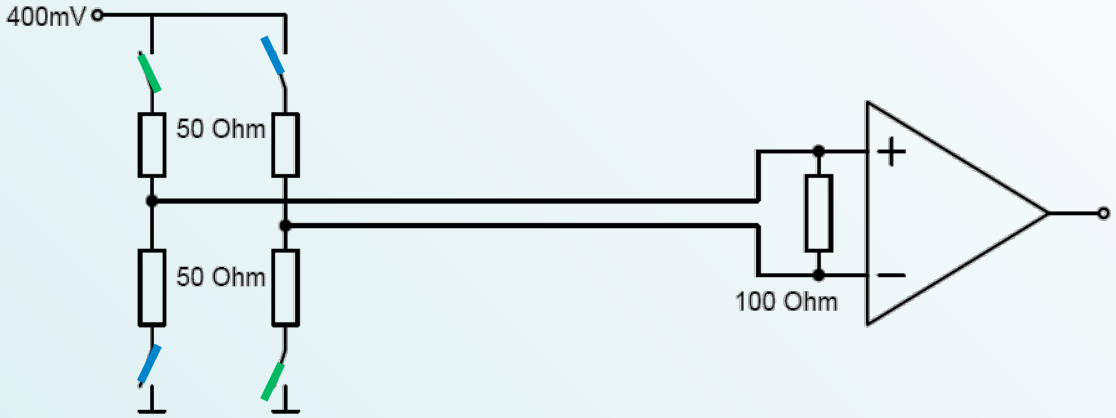
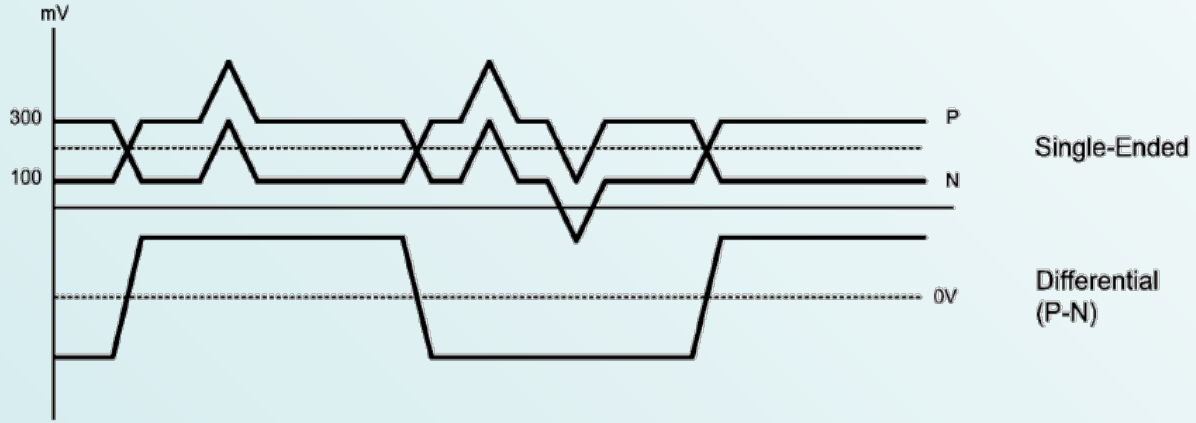


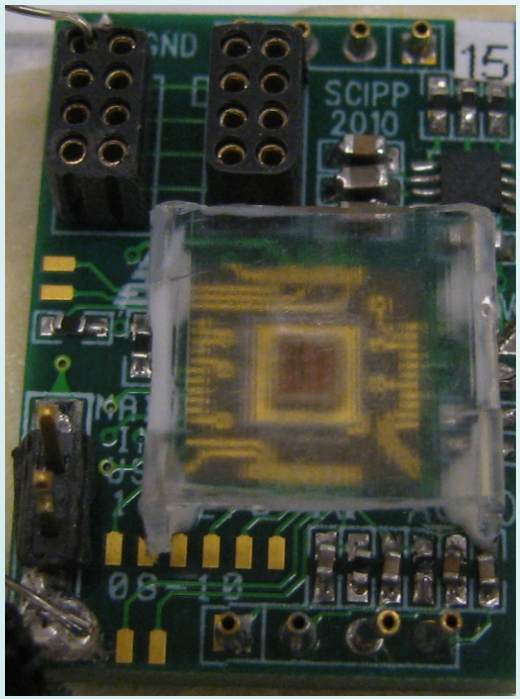
Fig. 1: The SLVS is a differential signaling method

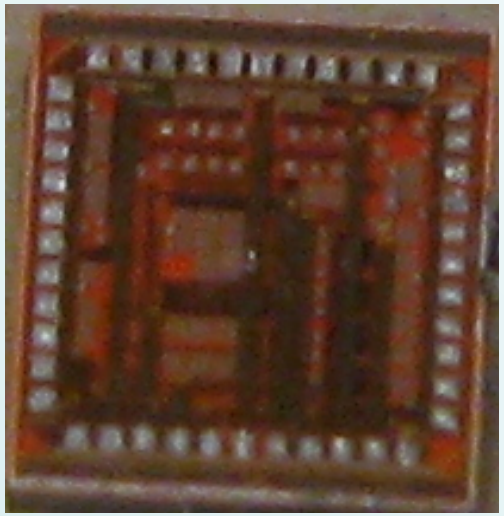
- Nat. Semi.’s LM4308 link chip (used by GBT group for tests)



AUEIO Chip

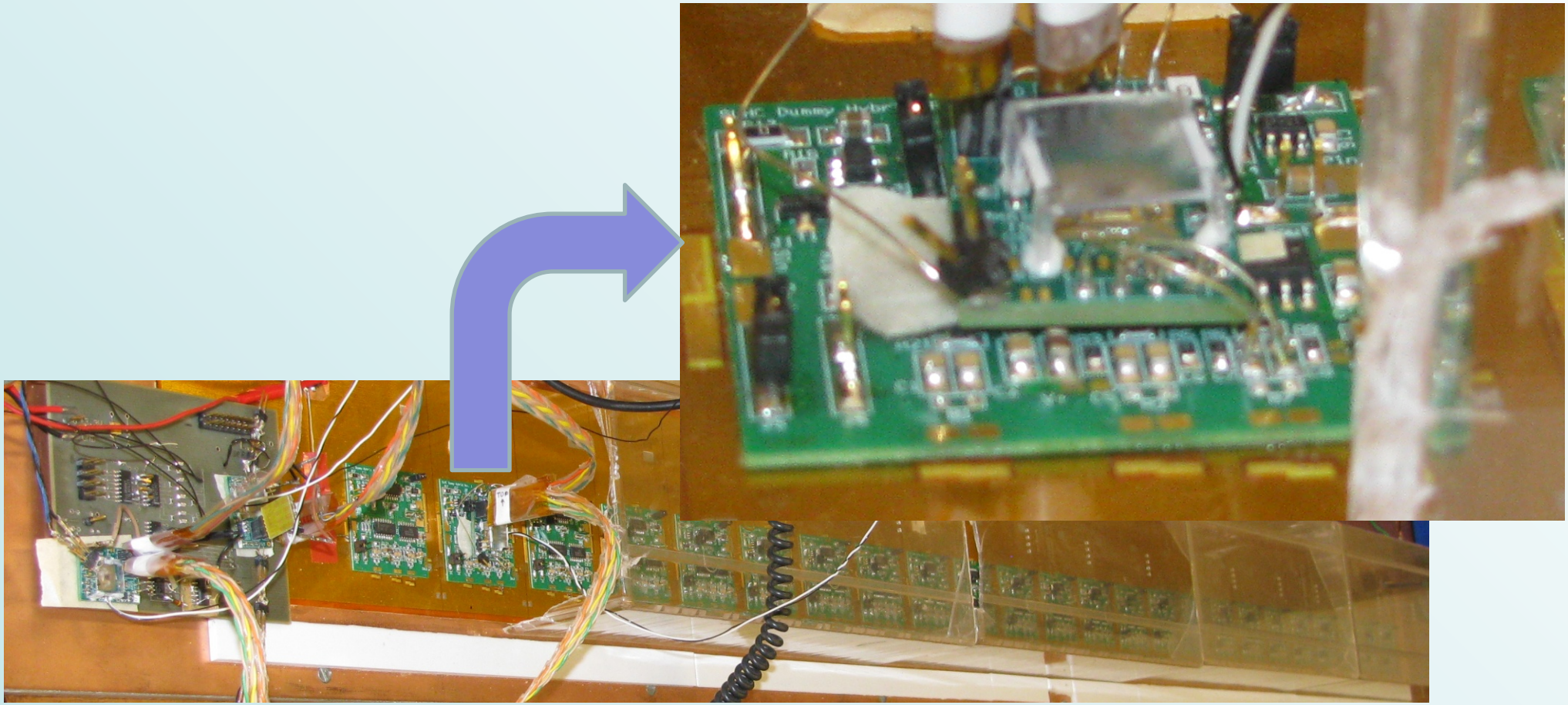
- SCIPP designer, Joel DeWitt, attempted to follow SLVS-400 spec, with scalable currents.
- Has SLVS receiver with termination to GND as well as one without, for multi-drop operations.
- Also LVDS driver/receiver with scalable currents.
- Also PLLs, noise-generating gates and some other experiments.



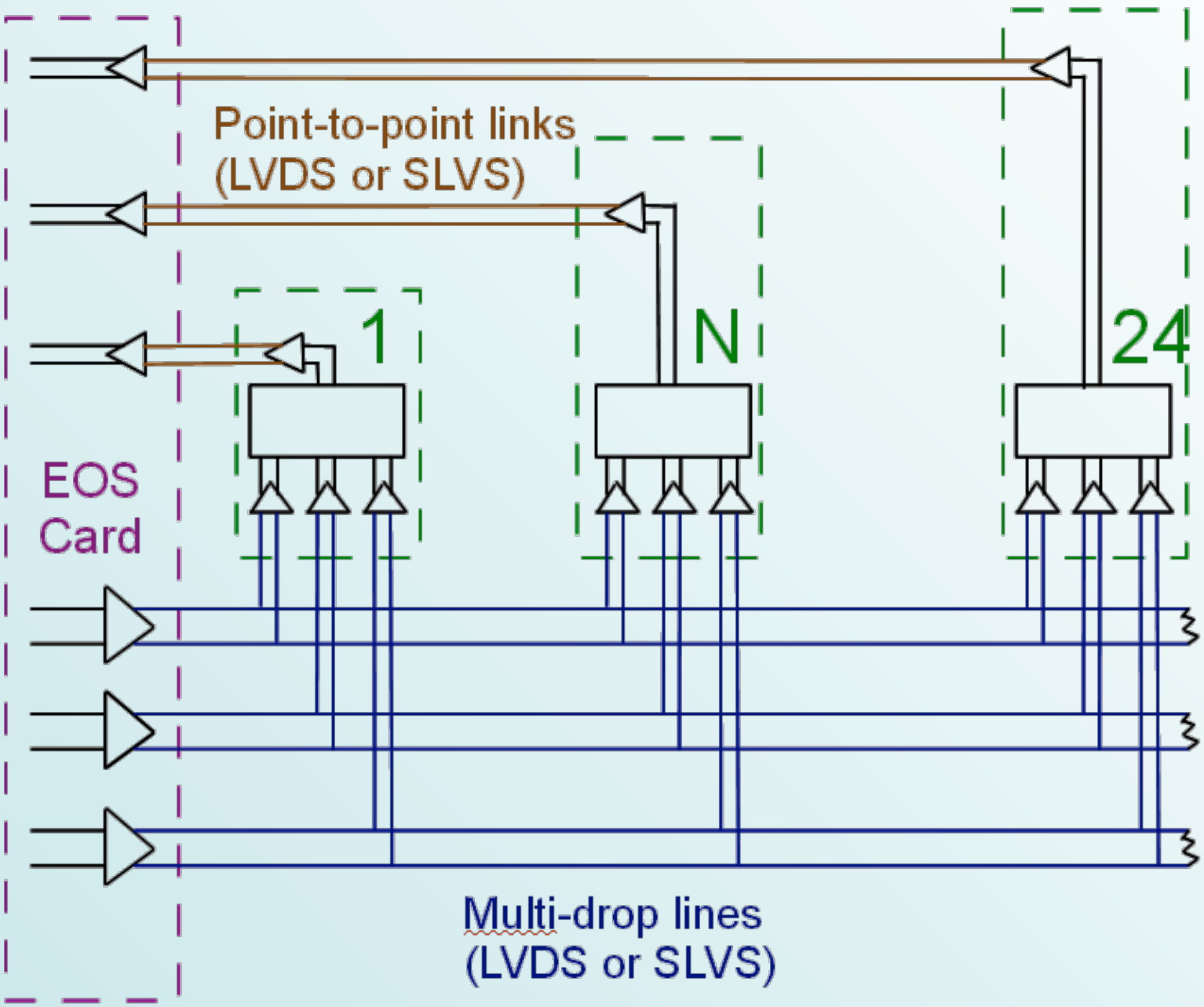


Cable Testing

- All the testing was done on Oxford cable using either provided hybrid models or SCIPP chip as a replacement.

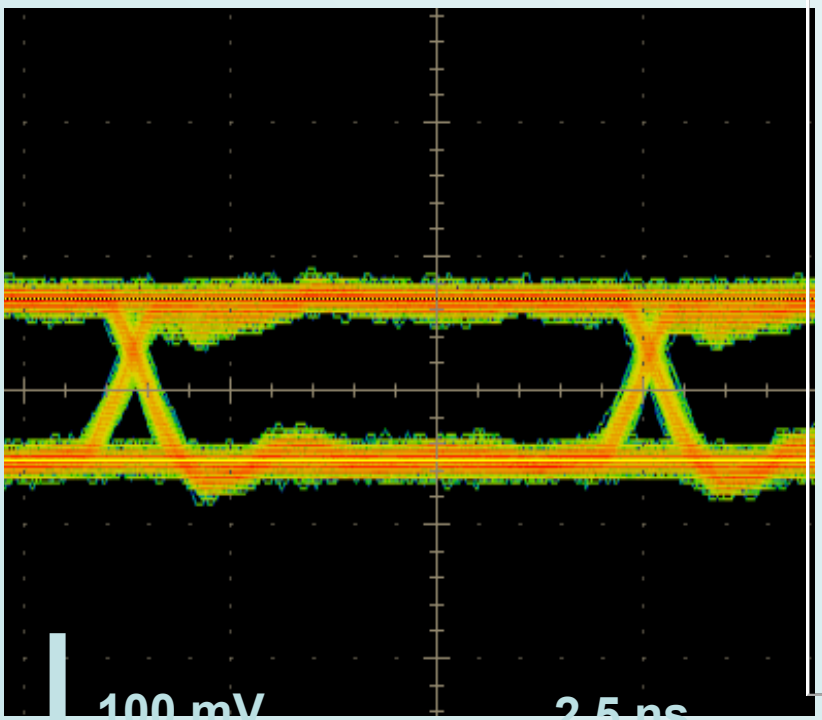


Connection Scheme

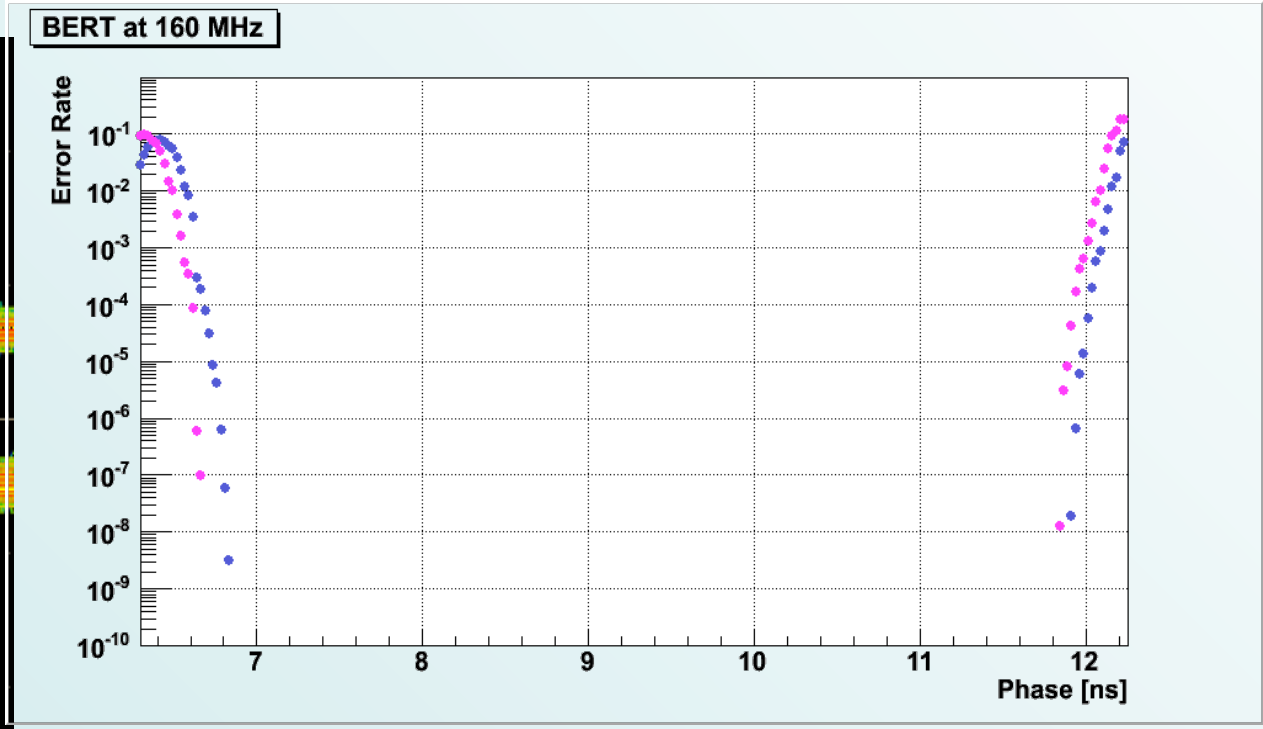


SLVS Tests

- AUEIO chip in place of hybrid # 2.
- BERT at 160 Mbps. Data broadcast on multi-drop line with a return via point-to-point link.
- Nominal performance is ok even at lowest setting of 0.85 mA.



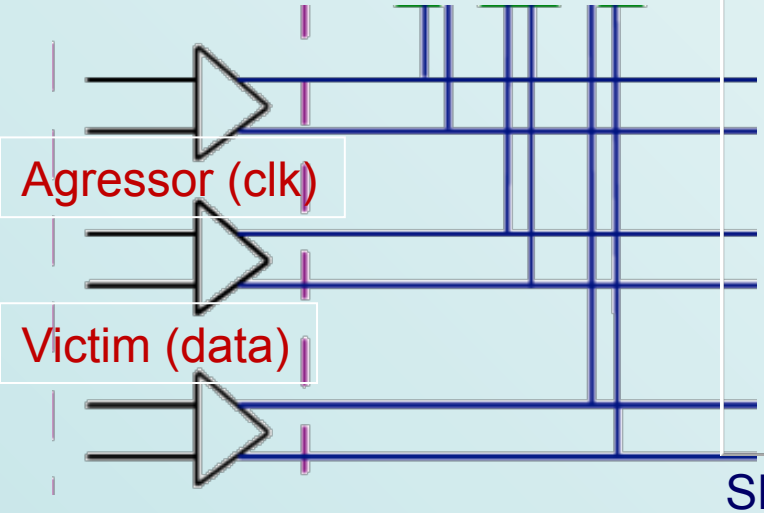
Eye diagram at i=0.85 mA

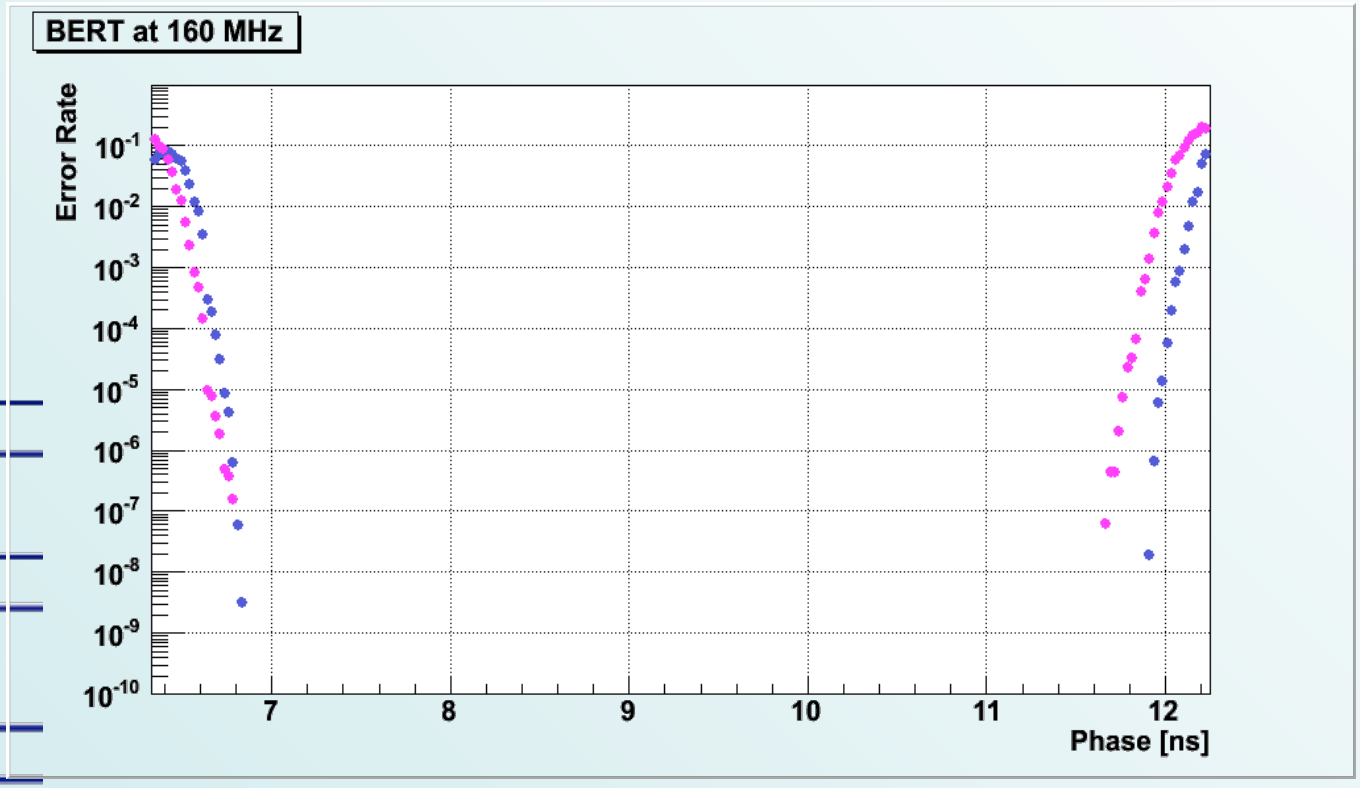


BERT comparison at I = 0.85 mA (blue) and I = 2.1 mA (red)

Cross-talk Measurements

- AUEIO chip in place of hybrid # 2.
- Stimulating a neighboring multi-drop line by a 100 MHz clock signal. Ran BERT at 160 Mbps with SLVS line at lowest setting of I = 0.85 mA.
- The effect is small, ~0.3 ns phase space closing.



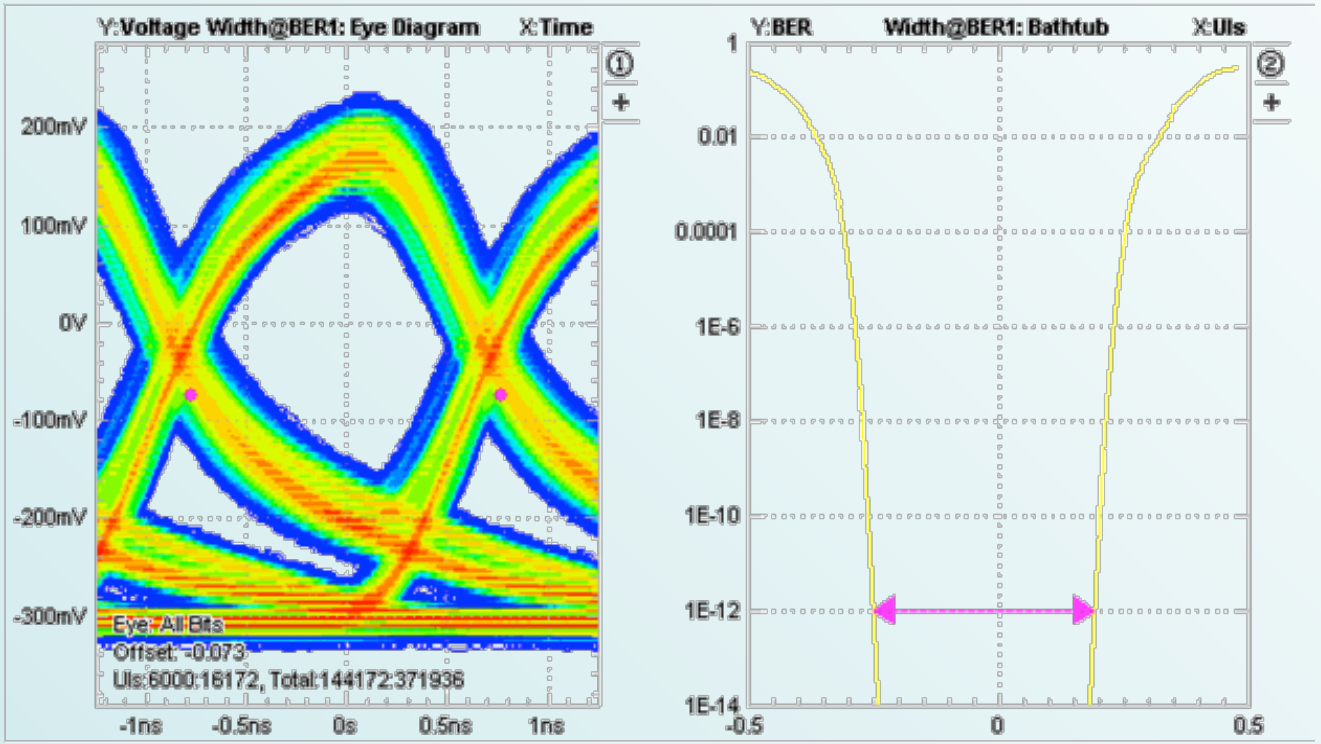


SLVS BERT comparison with (red) and without (blue) crosstalk

Fast Point-to-Point Link

- AUEIO has a built-in PLL which can driver a circular buffer with sequence of “00001000100101”.
- Run these data through 1.2 m point-to-point link at I = 4.7 mA at 640 Mbps. (BERT scheme currently in use does not work at well above 320 Mbps.)
- Estimated BERT with scope software.

Period	1545.8ps
Random Jitter	19.605ps
Determ. Jitter	647.89ps
Total Jitter @10^-12	867.15ps
Opening @10^-12	678.66ps



Conclusions

- We see promising results in quasi-realistic settings with both LVDS and SLVS signals at 160 Mbps at low amplitudes. This needs to be verified for *other hybrid locations* (in progress).
- The cross-talk influence on multi-drop signals seems to be minimal.
- See an indication that a point-to-point link can be run at 640 Mbps.
- Checks with CERN chips are about to restart. Got the necessary socket a few days ago.

An aside:

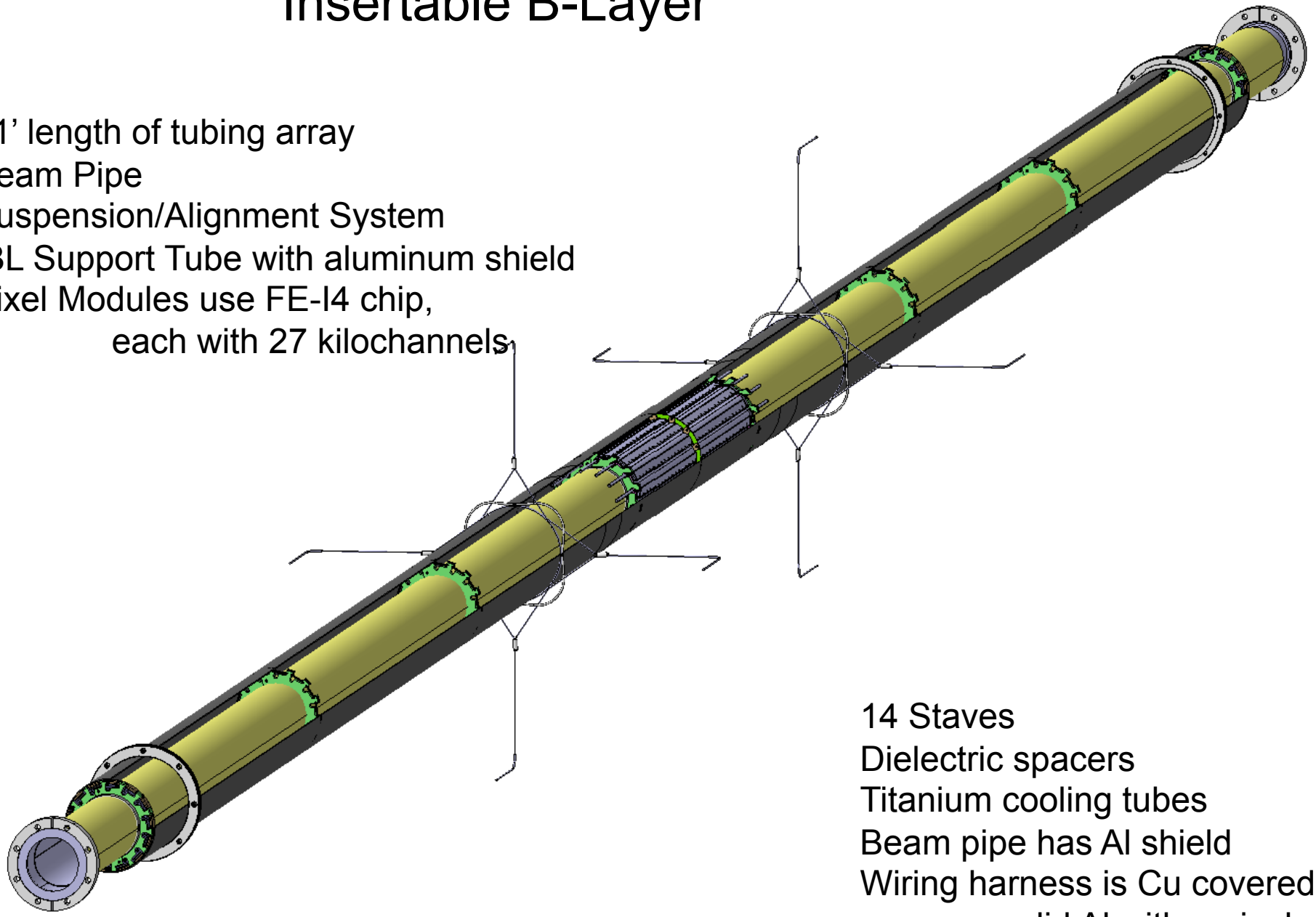
- Having low-impedance grounding scheme was crucial.
- Thin-oxide transistors, also used in AUEIO chip, are fragile, even with ESD protection built-in, and strict ESD handling protocol.

Insertable B-Layer: IBL Pixel Detector

- **Current intense development Atlas detector: could be inserted as early as 2014**
- **Packed around a downsized LHC beam pipe.**
- **Radial space IBL envelope is R40 to R31. Hardware fits into 9 mm envelope**
- **Starting recently, SCIPP provides IBL grounding and shielding co-ordination. We will also do fabrication and assembly of micro-harness cabling for the final detector services.**

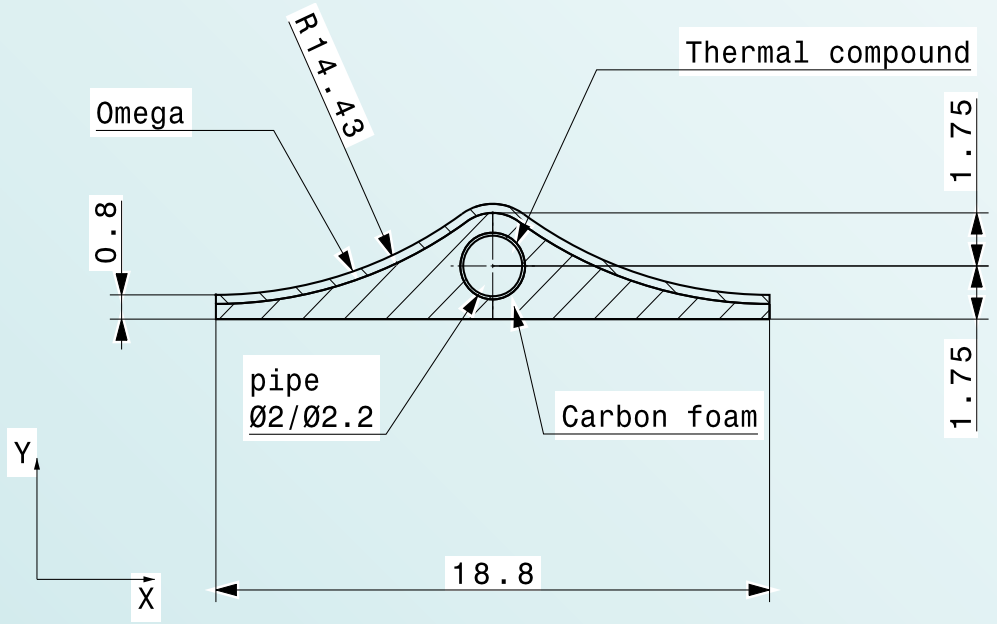
Insertable B-Layer

21’ length of tubing array
Beam Pipe
Suspension/Alignment System
IBL Support Tube with aluminum shield
Pixel Modules use FE-I4 chip,
each with 27 kilochannels

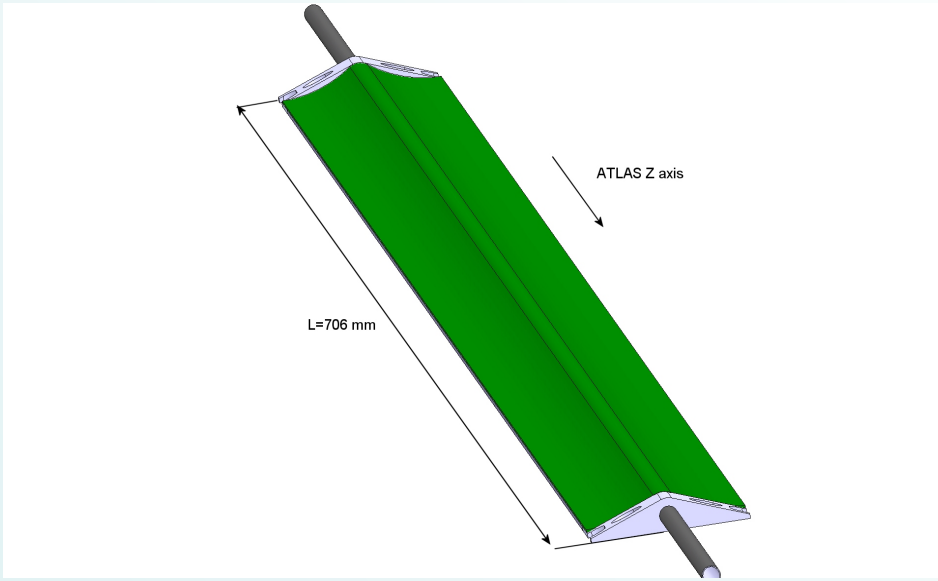


14 Staves
Dielectric spacers
Titanium cooling tubes
Beam pipe has Al shield
Wiring harness is Cu covered solid Al with no jacket or shielding

View of the IBL Stave



(a) Cross-section



(b) 3D view

Figure 67. Cross section and 3D model of the IBL stave. Dimensions are in millimeters.

Cross-section of Stave Layout

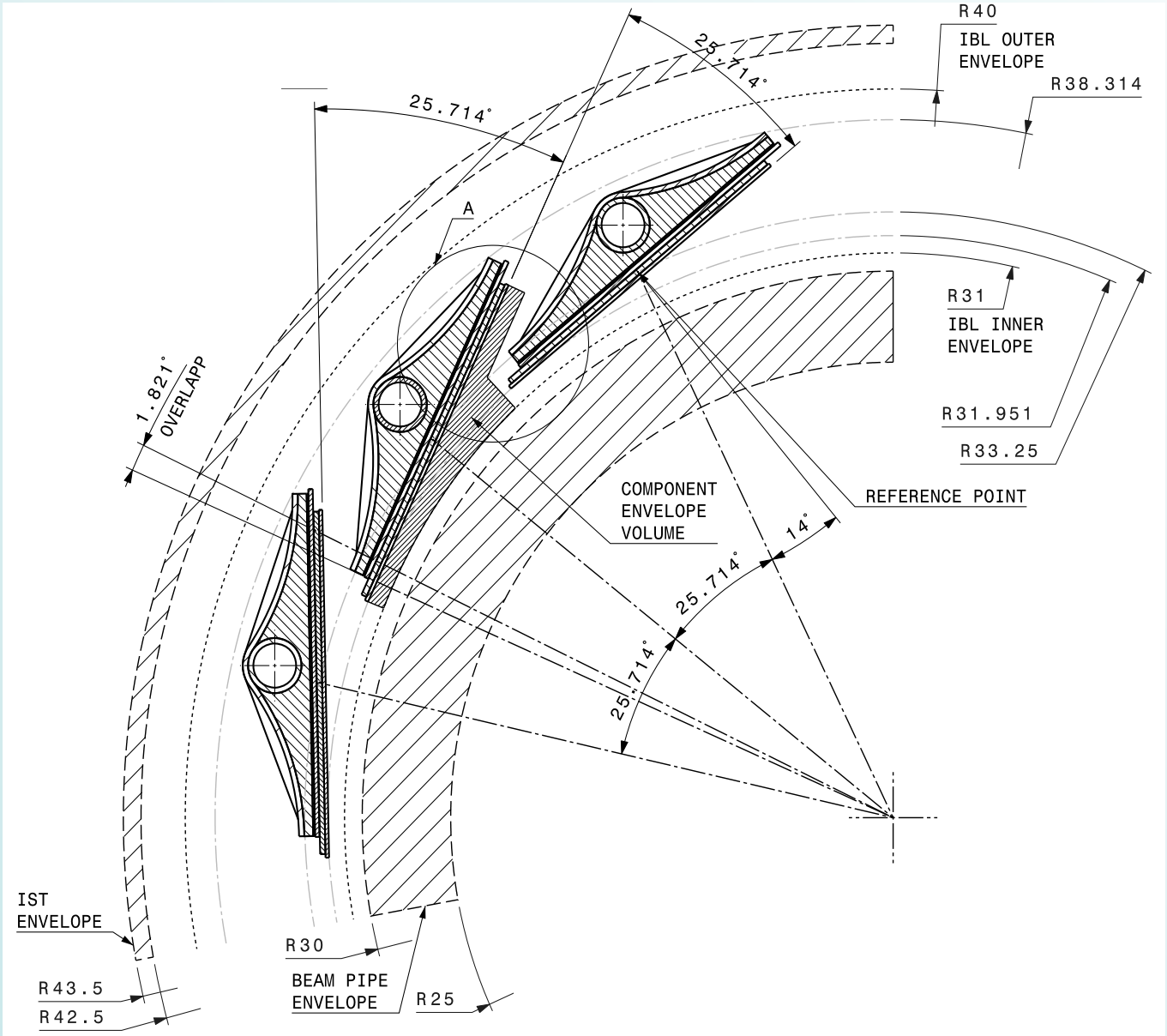
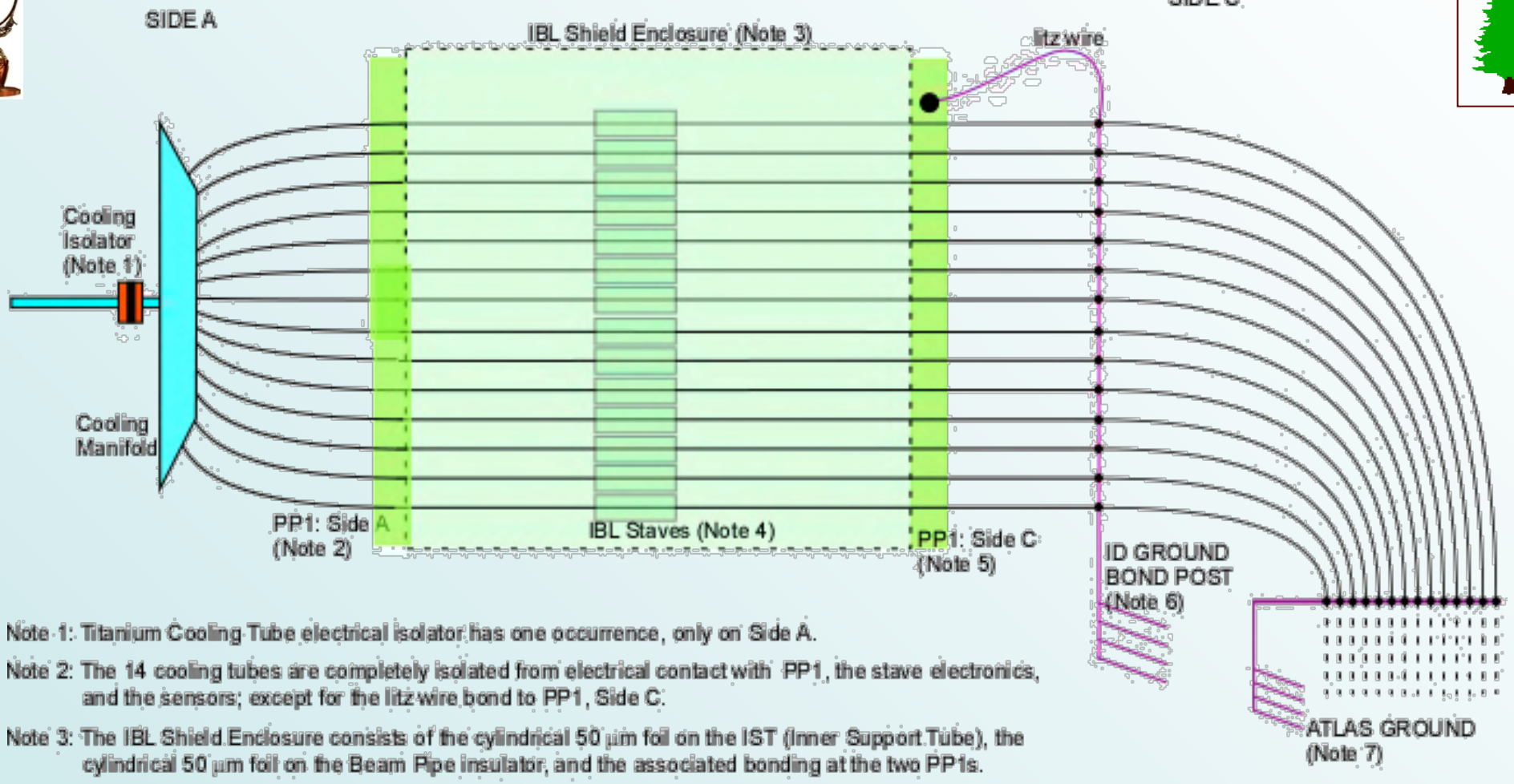


Figure1: IBL Stave Tube Electrical Shield Bonding Diagram



Note 1: Titanium Cooling Tube electrical isolator has one occurrence, only on Side A.

Note 2: The 14 cooling tubes are completely isolated from electrical contact with PP1, the stave electronics, and the sensors; except for the litz wire bond to PP1, Side C.

Note 3: The IBL Shield Enclosure consists of the cylindrical 50 μm foil on the IST (Inner Support Tube), the cylindrical 50 μm foil on the Beam Pipe insulator, and the associated bonding at the two PP1s.

Note 4: The 14 IBL staves are conductive carbon foam structures electrically bonded to the cooling tubes. The staves are electrically isolated from all the IBL electronics and sensors that they support.

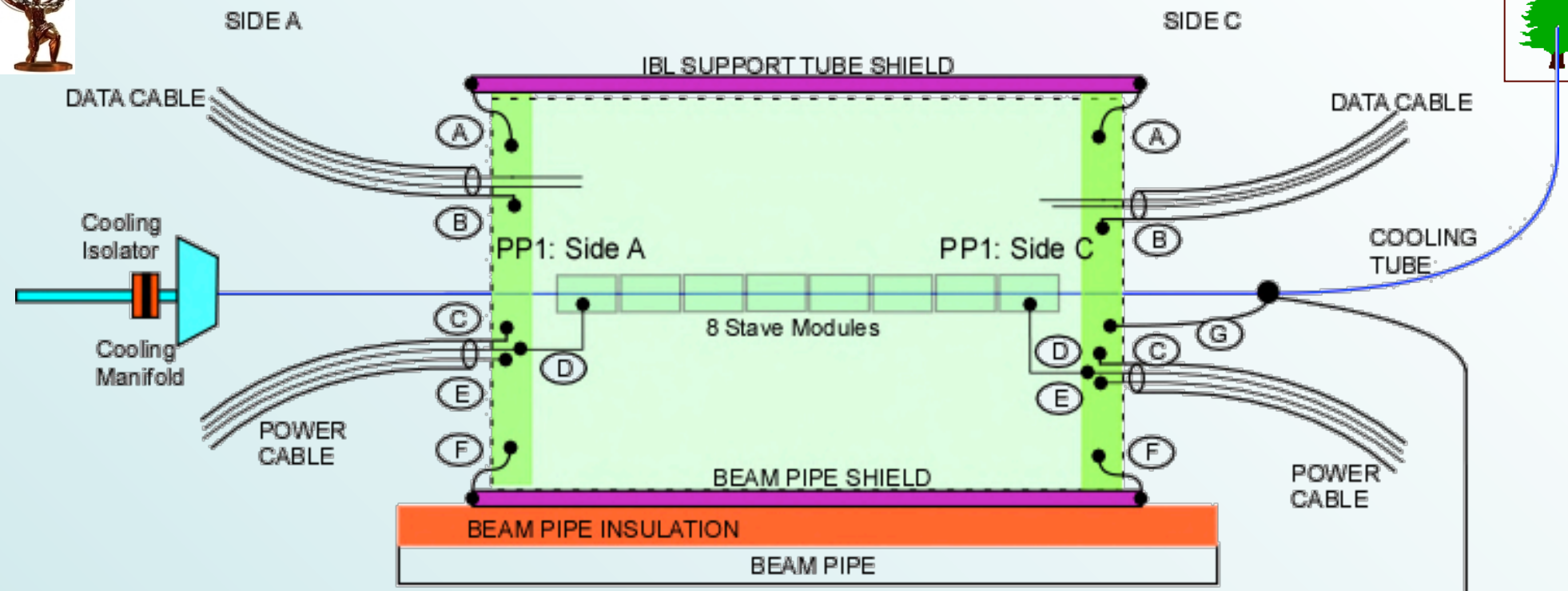
Note 5: The 14 cooling tubes bond RF (Radio Frequency) to PP1, Side C. The bonds to PP1 shield node can be 22 AWG equivalent Litz wires brazed or strapped to the tubes. The bond strap should be as short as is practical.

Note 6: To the right of PP1, C side, the tubes should be bonded together with litz wire. The common litz wire bonds to PP1. A second 6 AWG litz wire ties the cooling tubes to the Inner Detector Ground bond post that the other inner detector earthing conductors use.

Note 7: The parasitic bond to Atlas Ground that the cooling tubes make is the inevitable earthing at their refrigeration equipment. The tube array net resistance is much greater than the intentional 6 AWG copper earthing conductor tie.

Edwin Spencer
UCSC, SCIPP
December 9, 2010

Figure 2: IBL Shield Bonding Diagram



A through G detail PP1 bonds:

A. IST Shield is 50 μm Al. The PP1 bond needs to be at least three 1 cm foil straps or litz wires, at both ends of shield.
B. Data cable has foil shield with drain wire. PP1 bond is RF quality.
C. Power cable has foil shield with drain wire. PP1 cable shield bond to PP1 is RF quality.
D. Stave Module Power Return references at PP1
E. Cable HV Return bonds to Power Return at PP1. Voltage drop on Power Return to Stave Module induces a negligible drop on the HV potential.
F. Beam Pipe Shield is 50 μm Al. The PP1 bond needs to be at least three 1 cm foil straps or litz wires, at both ends.
G. The Cooling Tube bonds solely at PP1, Side C, using a litz wire or flex tape for the 14 tube group as the only path to PP1. Both Stave Flex Circuits, all electronics, and all sensors are isolated from direct electrical contact with the tube and carbon foam support structure.

H. At the cooling tube commoning point that is to the right of PP1, Side C, the single IBL earthing bond uses a litz wire to the ID Ground post that all ID detectors share.

Edwin Spencer
UCSC, SCIPP
December 9, 2010

Grounding and Shielding Interview

- Small signal current loop well defined? This is the array of conductors that the physics signal traverses to drive the charge sensing amplifier.
- Do other electric functions intersect the small signal loop? EMI needs to captured and routed around the physics signal. Digital electronics uses different metal.
- Do connectors or metal objects with EMI short across the small signal physics?
- Do unavoidable ground loops that shield EMI capture the small signal loop?
- Is the metal shield complete? Are the slots, gaps, and holes really necessary?
- Are the cables reasonably well designed? Can the cable shields get a better bond than a nasty little wire at the connector.
- Are the joints between metal more than a few fasteners? Are the joints aluminum with no plating?
- Do the shield joints between different metals have reasonable galvanic potentials?
- Is there a single point ground for the entire system?

SCT Upgrade: Research on Silicon Germanium Bipolar Technology

We designed a test chip in IBM 8WL process, with 140 Ghz npn bipolars, and did an irradiation using gamma, neutron, and proton particles.

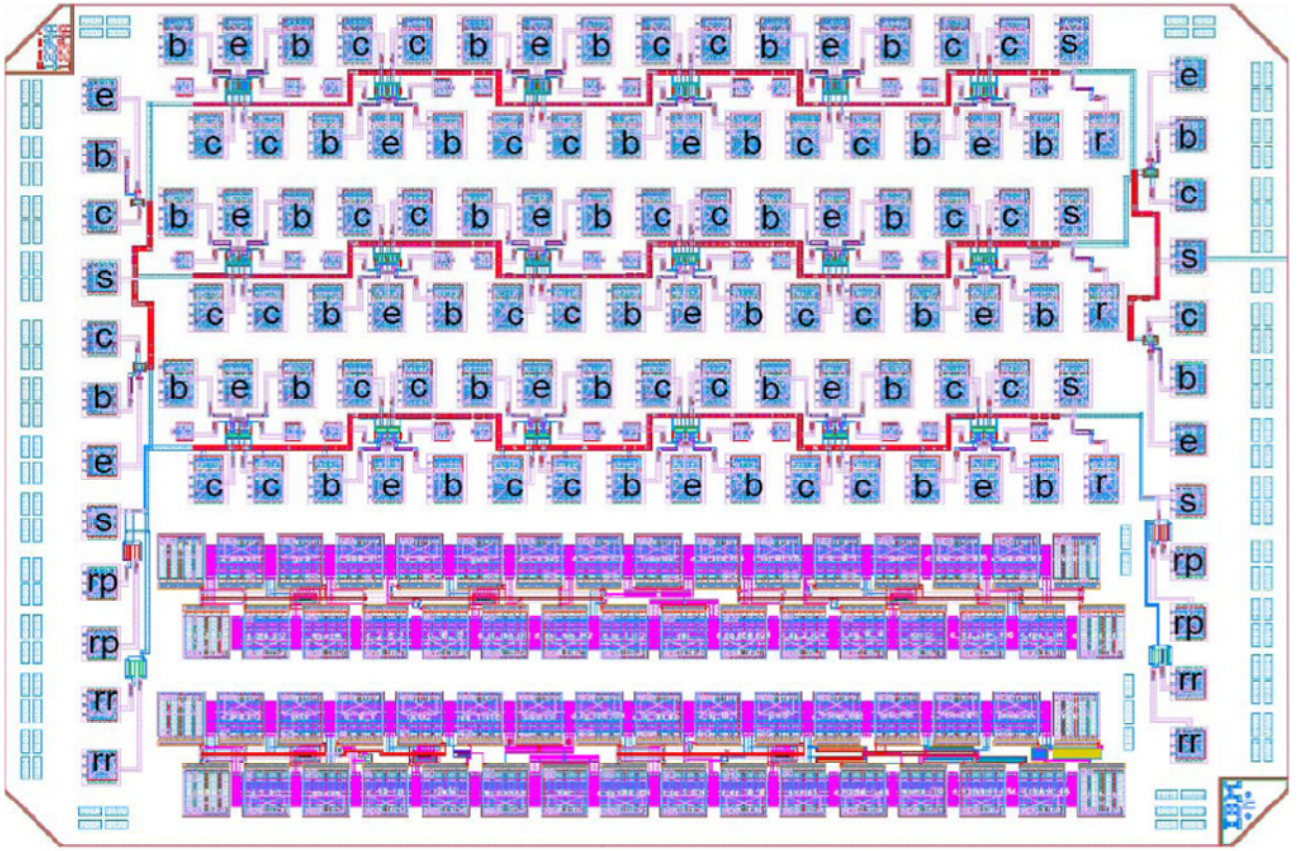


Figure 2: Layout of the SiGBiT radiation test chip. Location of the emitter (e), base (b), collector (c), and substrate (s) pads of the bipolar devices, as well as the polysilicon resistors (r, rp, rr) is indicated in the figure. The MOS test structure is located at the bottom of the test chip.

Proton Irradiation of IBM SiGe Bipolar130 nm Transistors

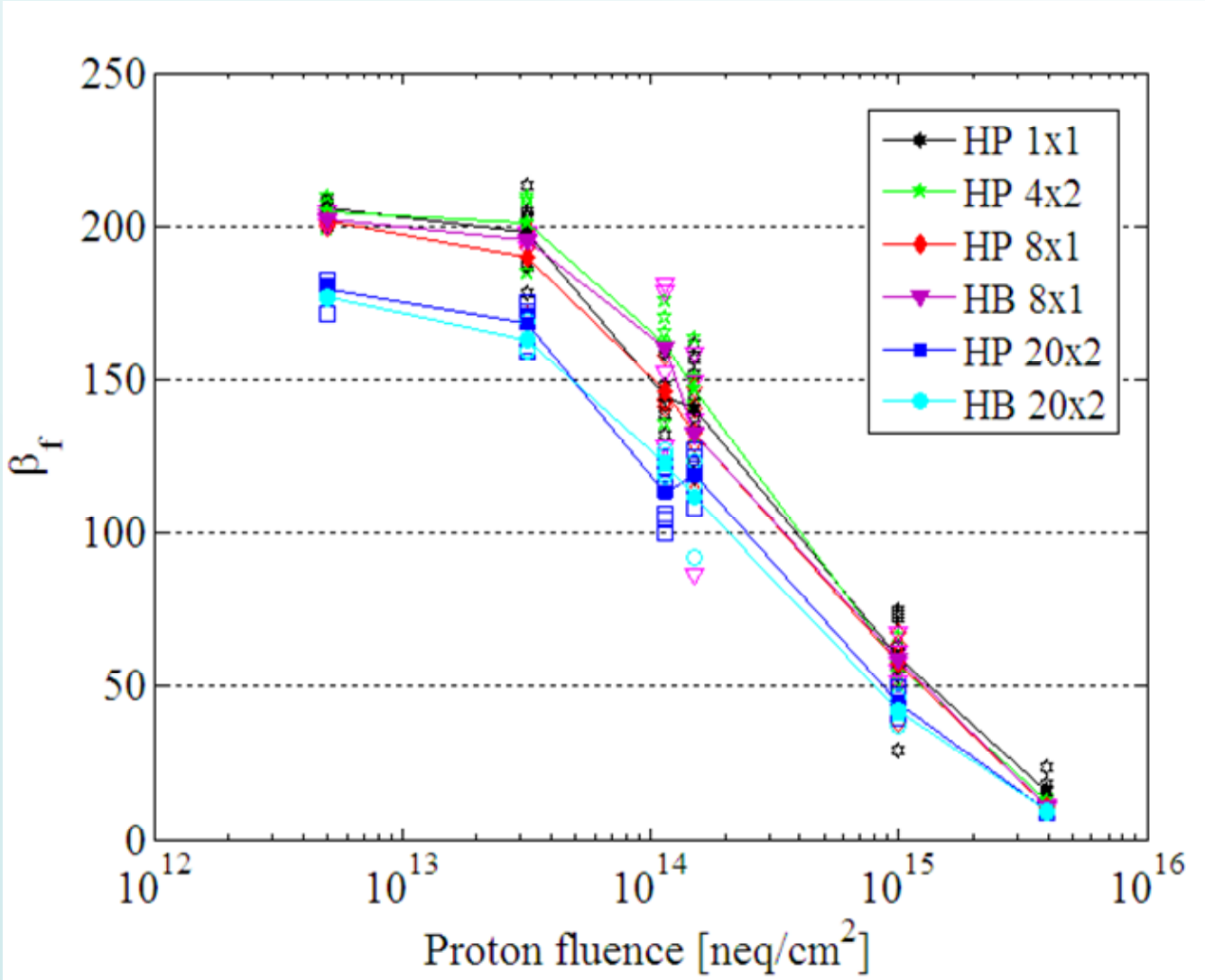
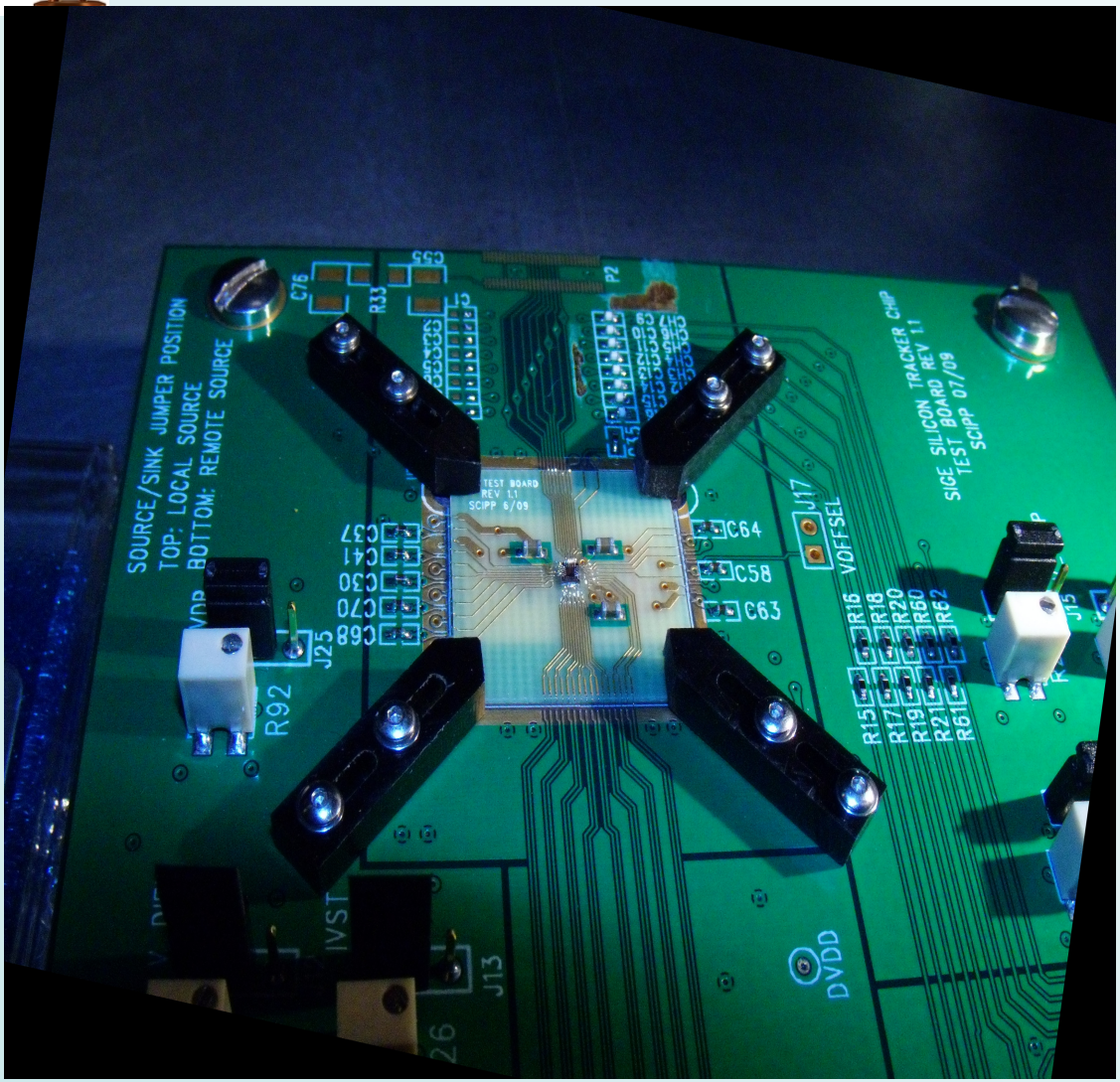


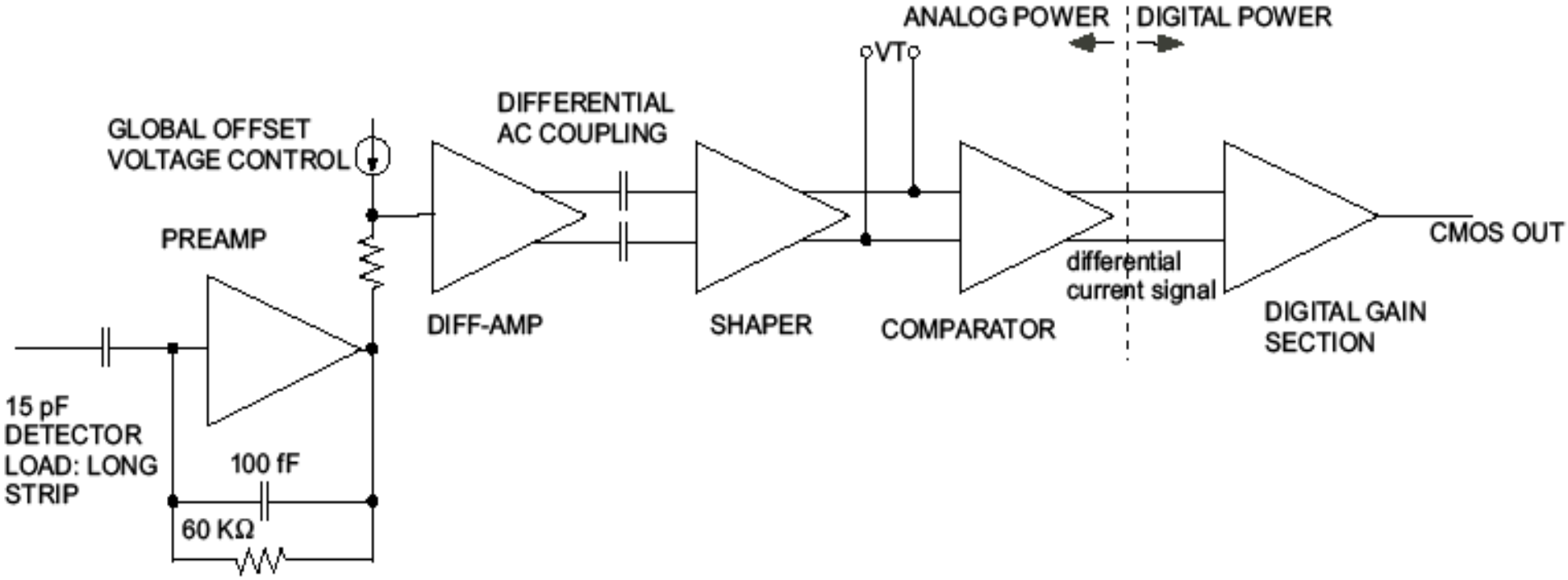
Figure 6: Common-emitter current gain (β_f) versus 800 MeV proton fluence (expressed in 1 MeV neutron equivalent fluence) for the different transistor types studied.

SiGe Front-End for SCT Upgrade



In the 180 nm BiCMOS SiGe SCIPP designed and submitted an 8 channel SCT amplifer-comparator. The goal was to minimize power consumption, while still meeting specifications of the current SCT ABCD chip.

BLOCK DIAGRAM AND POWER FOR SiGe SCT FRONT-END



102 µA +7 µA (LONG STRIP BIAS) | 30 µA | 15 µA | 10 µA (SOURCED FROM VDD) | .1 µA

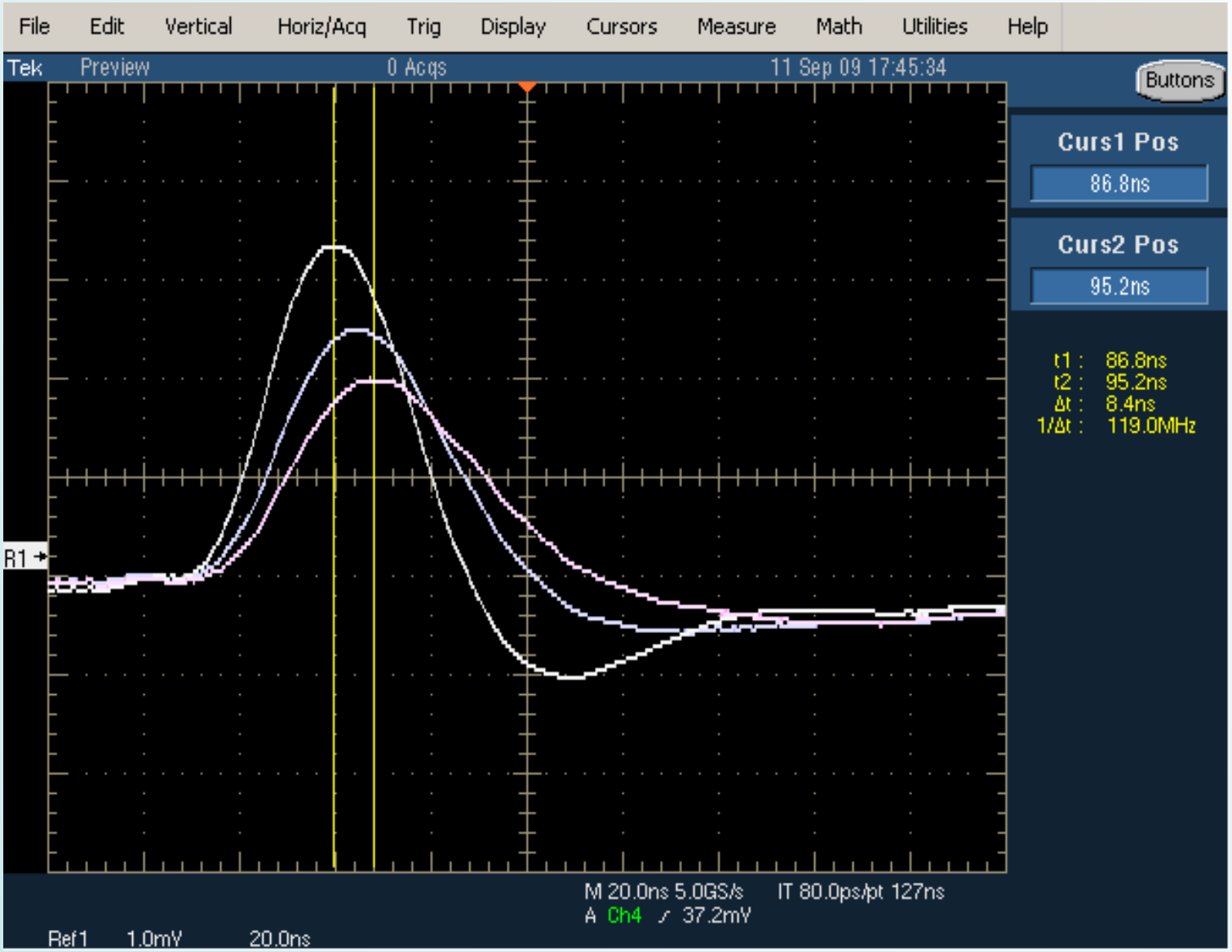
SGST biases total: 164 µA @ 15 pF (1360 e-), 126 uA @ 5.0 pF(<850 e-)

POWER @1.2 Volt RAIL: 0.197 mW/channel @ 15 pF, VT=1fC
0.151 mW/channel @ 5.0 pF, VT=0.5 fC

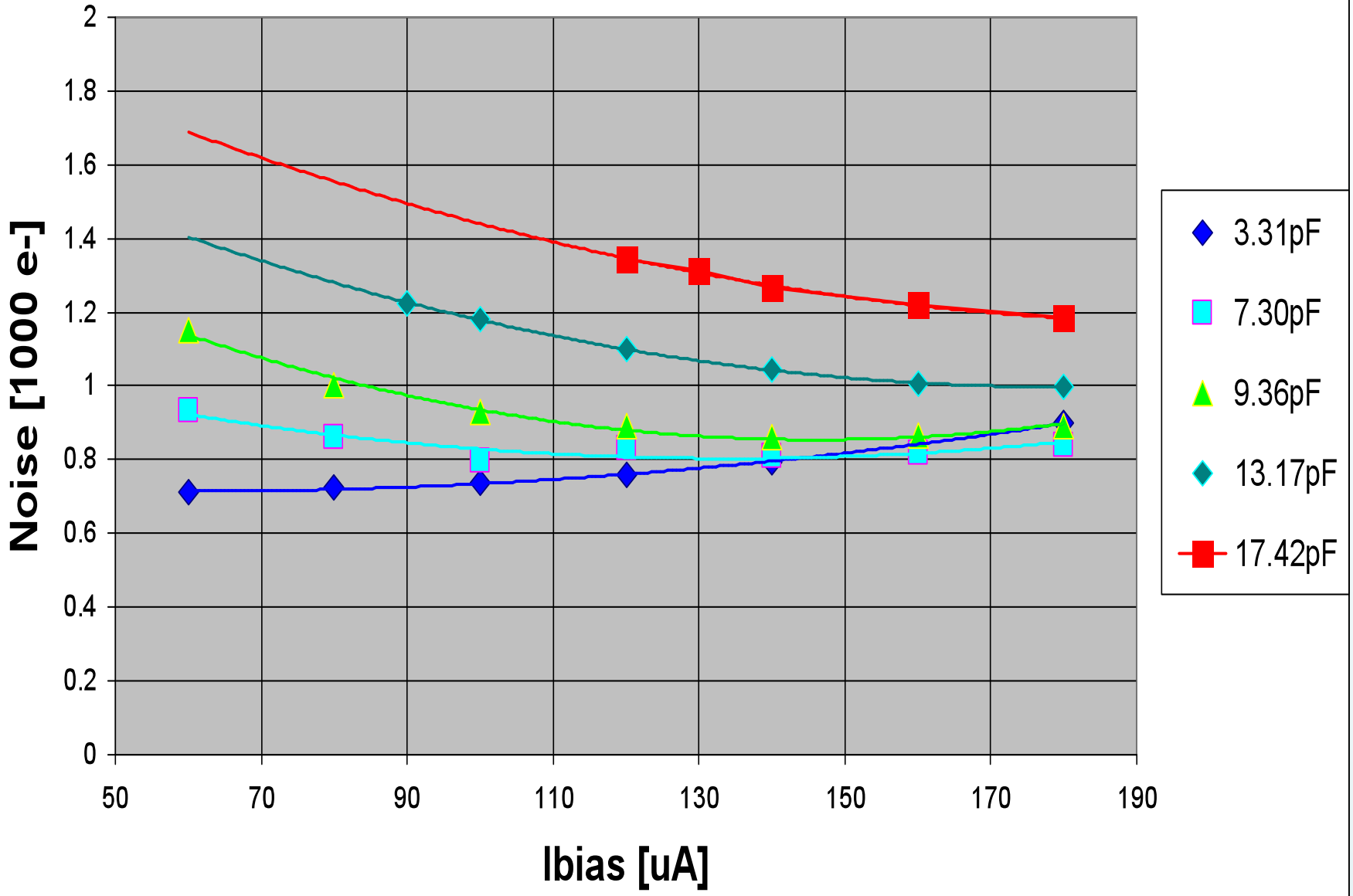
0.2 mW/channel compares with ~1 mW for current SCT front-end.

Edwin Spencer, SCIPP

Peak Shaping Time has Voltage Control

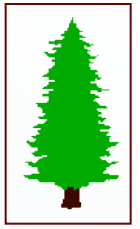


SGST Noise Referred to Input vs. Font Bias Current



Atlas SCT Upgrade Chip work for Stave09

- **Joel DeWitt of SCIPP is part of the US design team centered at U Penn doing chip development on IBM 130 nm CMOS.**
- **For the SPP, Serial Powering and Protection chip, he will convert the 2.4V logic presently employed in the SPP design to 1.2V logic utilizing IBM's standard digital library parts as a basis.**
- **For the same SPP, he will expand the command set to include instructions to allow the hybrid voltage to be trimmed remotely ± 15%.**
- **Our chip design will use the CERN licensed IBM protocols and support for 130 nm process, 8RF. One the biggest challenges will be the modifications and techniques to get SCT upgrade radiation resistance and acceptable SEU (Single Event Upset) performance.**

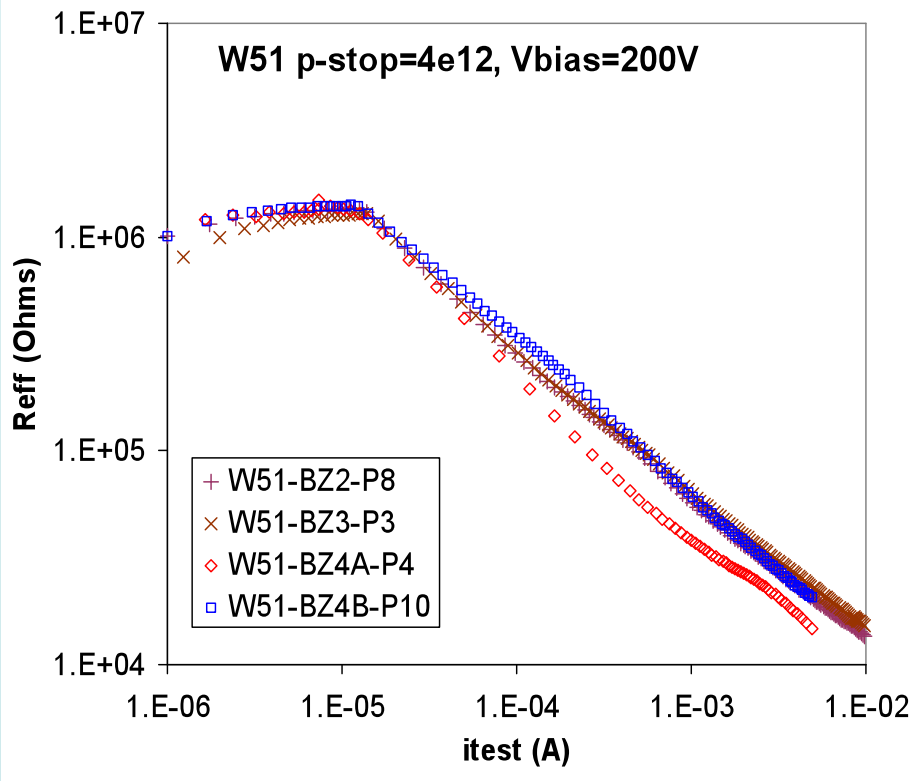


Extra Slides

DC Characteristics of PTP Structures

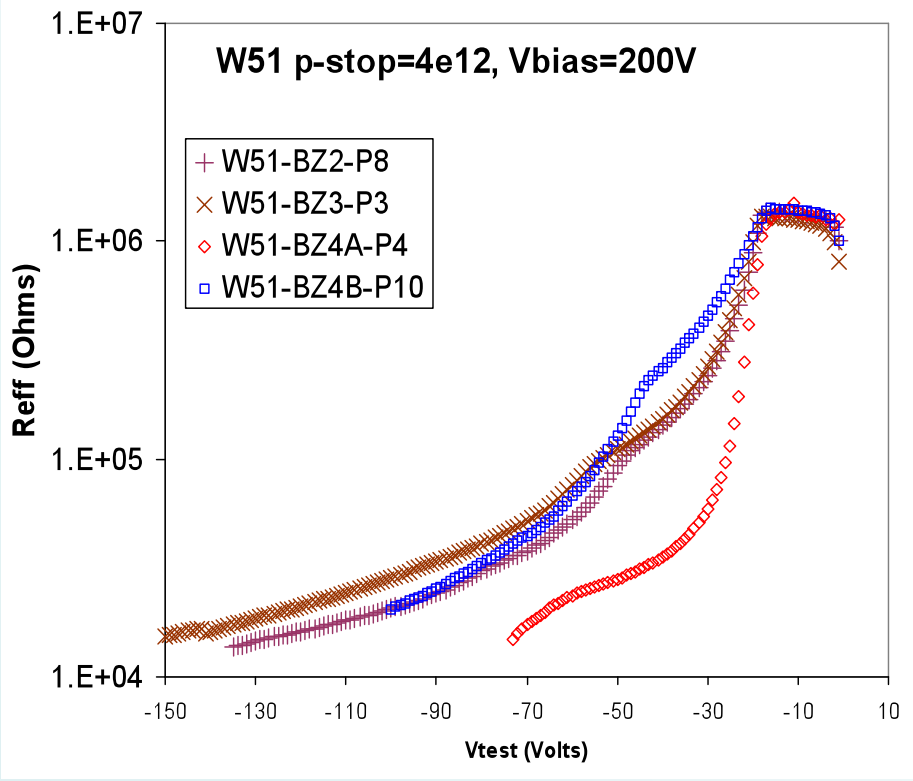
Extend the DC measurements to larger voltages and currents.

R_{eff} vs. PT current



R_{eff} = 20 kΩ reached at current of about 5-10 mA .

R_{eff} vs. V_{near}



R_{eff} = 20 kΩ reached at different voltages for different structures

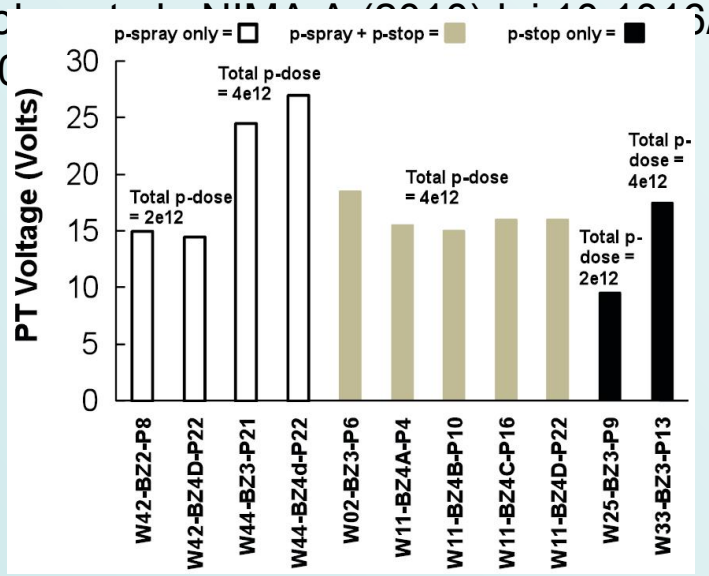
Observation #3:

Different PTP structures reach low resistance at different voltages.

PTP in Upgrade Sensors ATLAS07

- ATLAS07 N-on-P full-size sensors and "mini's"
- Test "Zones" in mini's to investigate:
  - Isolation and Interstrip parameters (C / R)
  - PTP (in Zone 4A-4D))

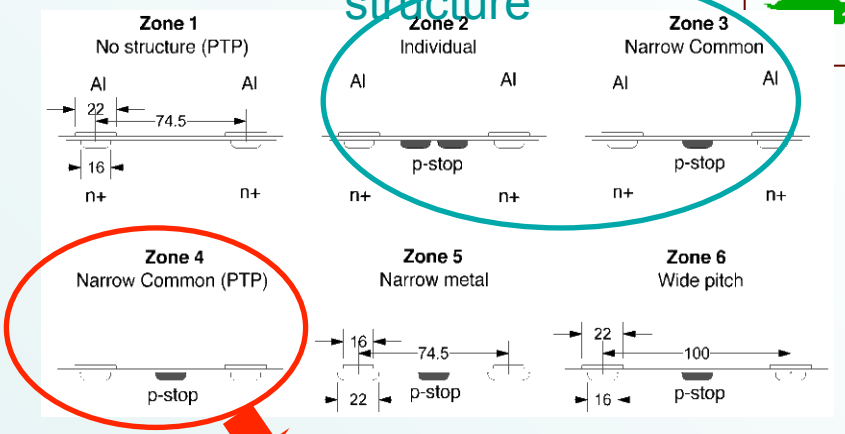
Y. Nc[illegible] NIMA A (2010) doi:10.1016/j.nima.2010.04.094



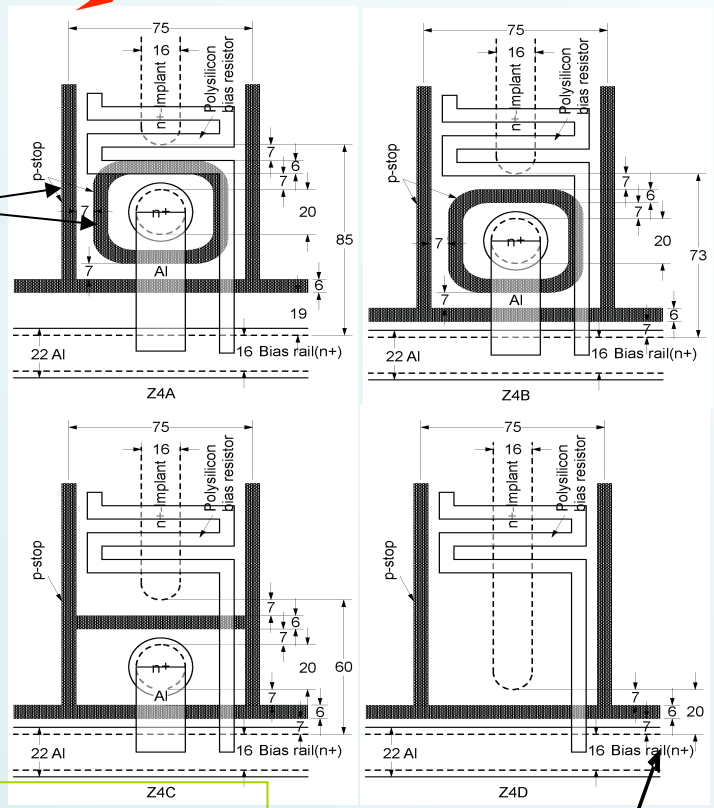
S. Lindgren, et al., NIM A (2010) doi:10.1016/j.nima.2010.04.094

- DC measurements show a surprising similarity of the PTP voltage (10-30V) across the many different structure geometries, with a dependence on total p-dose.

No PTP structure



P-stops make this complicated and delicate



Puzzle #2: The DC punch-through voltage is less sensitive to geometrical design details than expected (effect of p-stops and p-spray ?)

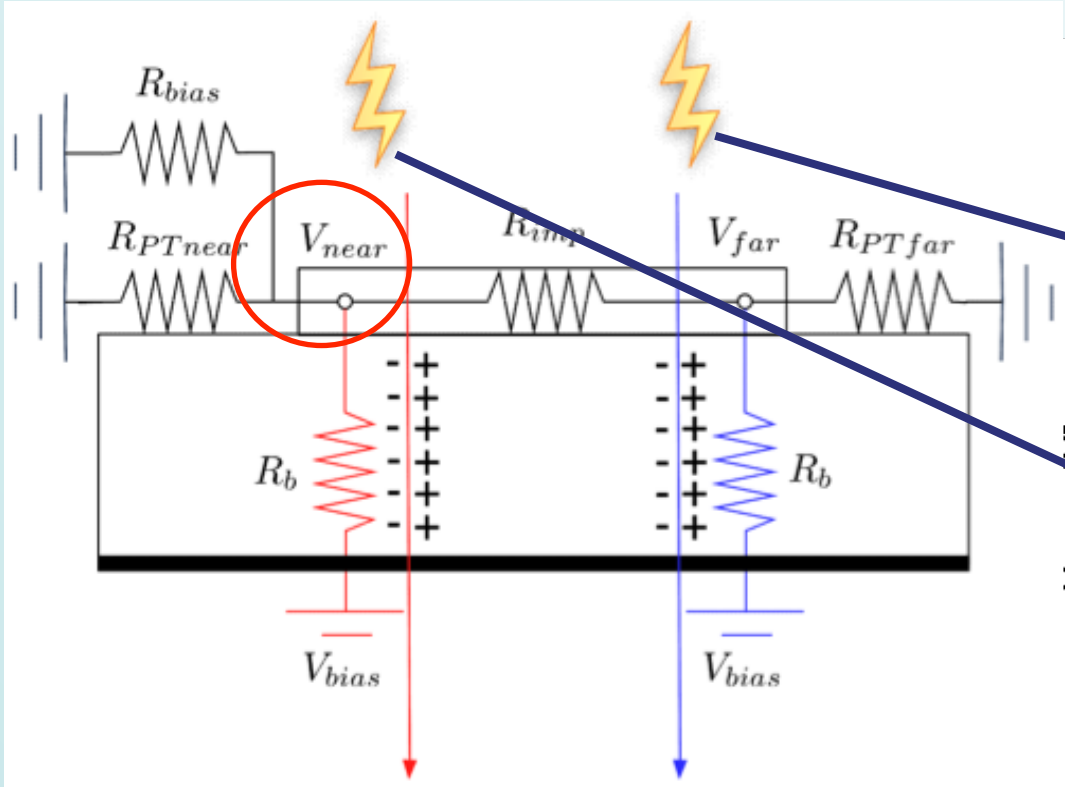
"Base line" Z3 is similar, but with 70μm distance

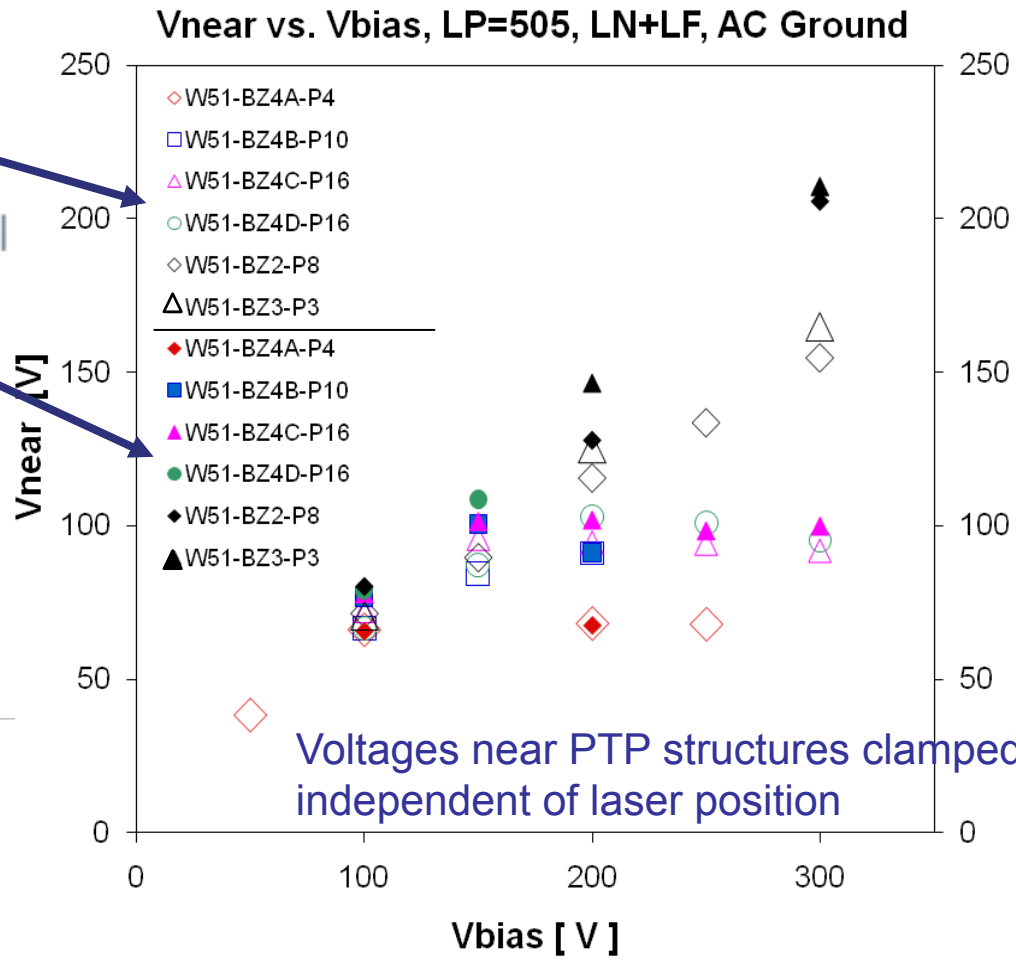
V. Fadeyev, "Punch-Through Effect..."

Propose a DC "4R" Model

- After breakdown of field inside the sensor, deal with DC resistor chain only
  - $R_{PTnear} = R_{eff}(R_{PTnear}, R_{bias})$
  - R_{PTfar} = R_{PT} on the far end of the strip, $R_{PTfar} \gg R_{PTnear}$
  - R_{imp} = Resistance of implant 15kΩ/cm
  - R_{bulk} = Bulk Resistance

To check 4R Model:
Measure both V_{near} and V_{far}
Fire laser both near and far.
Use DC value R_{PTnear}





Voltages near PTP structures clamped independent of laser position

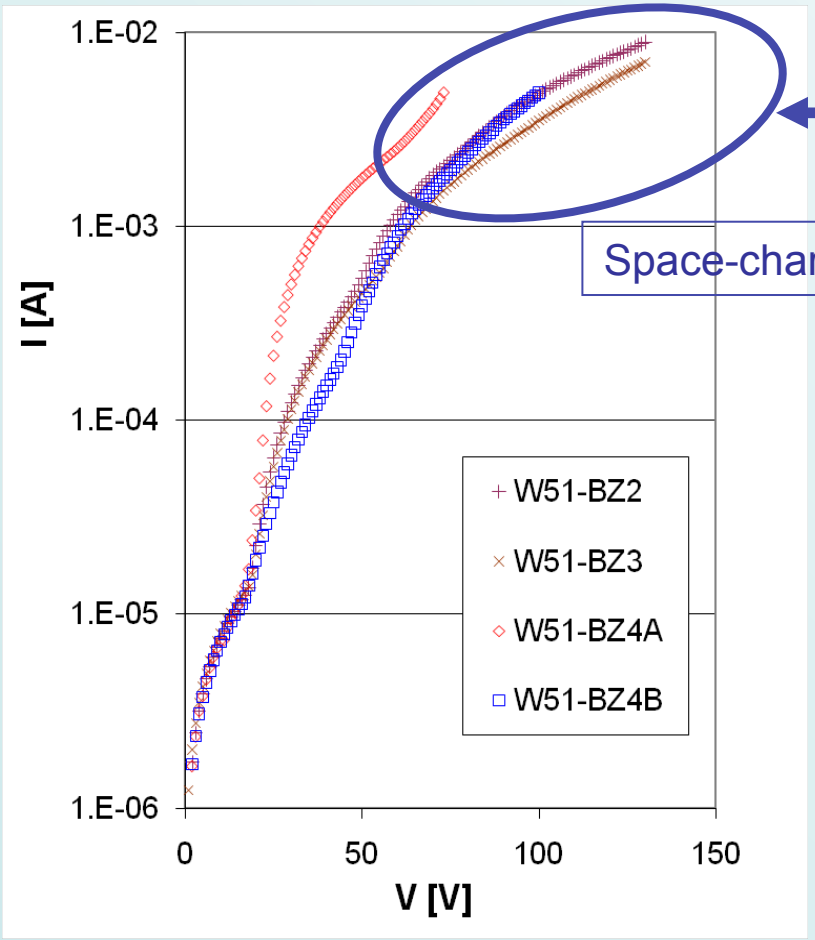
Estimate $R_b \approx$ 15-30 kΩ

Space-Charge Limitation in PTP Structures

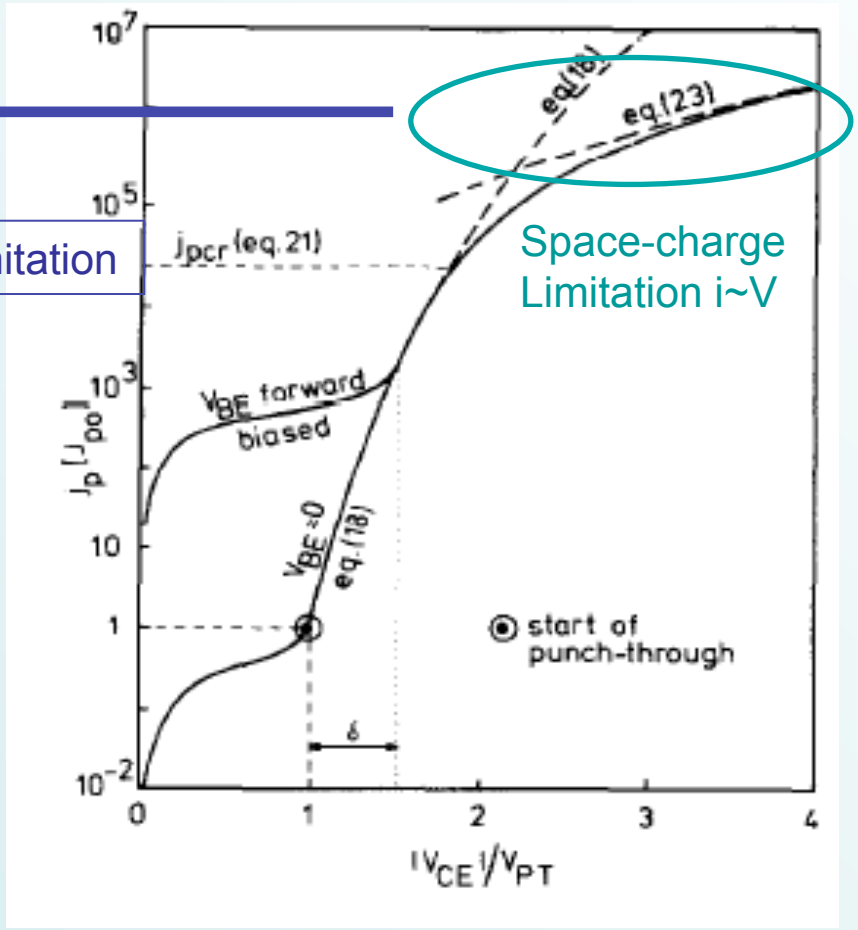
Literature:

- J.I. Chu, G. Persky, and S.M. Sze, J. Appl. Phys., Vol. 43, No.8, August 1972
- J. Lohstroh et al. Solid-State Electronics, Vol. 24, No. 9, pp. 805-814, 1981

I_{PT} vs. V_{PT}



Space-charge Limitation



Space-charge Limitation i~V

I –V curve indicates space-charge limited region at high voltages, when $R_{min} = L^2 / (2 \varepsilon v_s A)$ [for a planar sandwich geometry]. A fundamental limit of the PTP technique?

N-on-n sensors

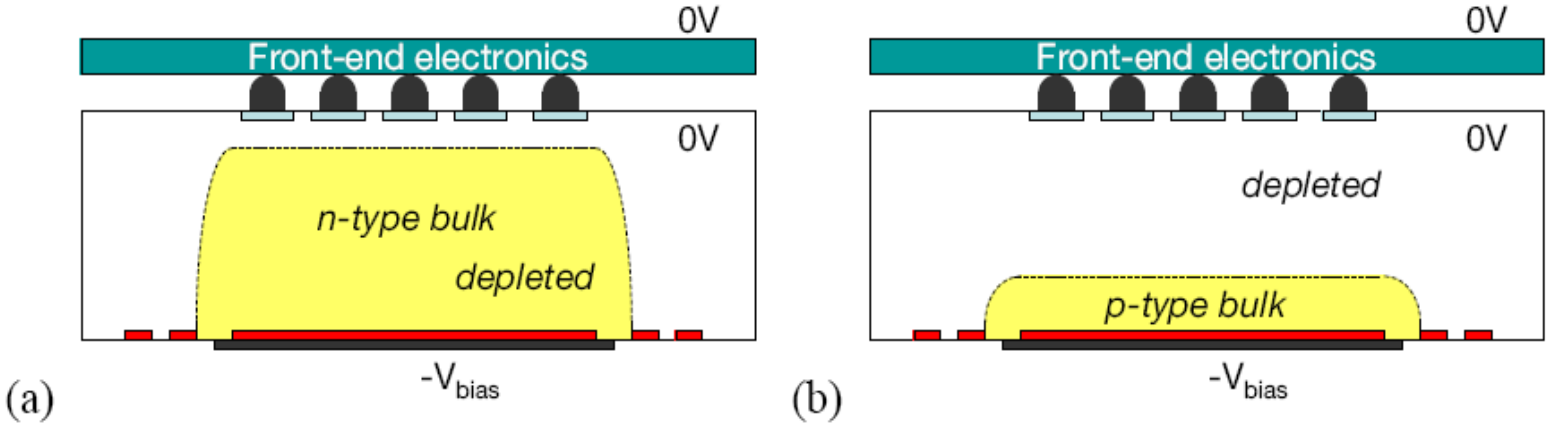
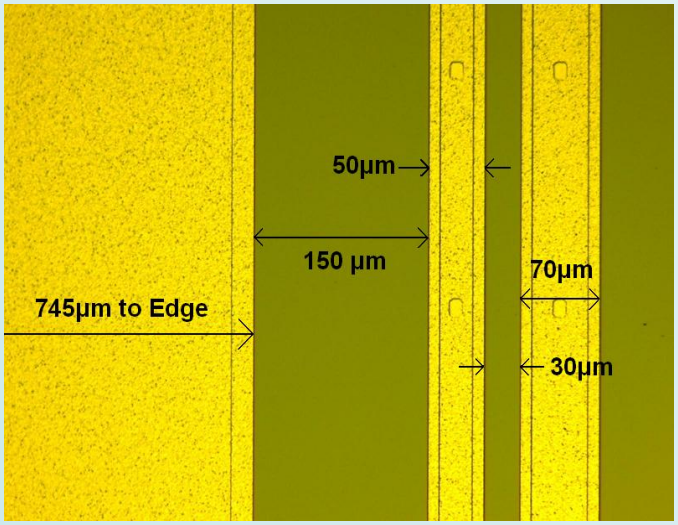


Figure 15. Comparison of depletion zones in n^+-in-n pixel sensors before (a) and after (b) type inversion. Before type inversion the electrical field grows from the backside and reaches the pixel implants (full depletion). After type inversion the depletion zone grows from the pixel side and allows operation even if the bulk is not fully depleted.

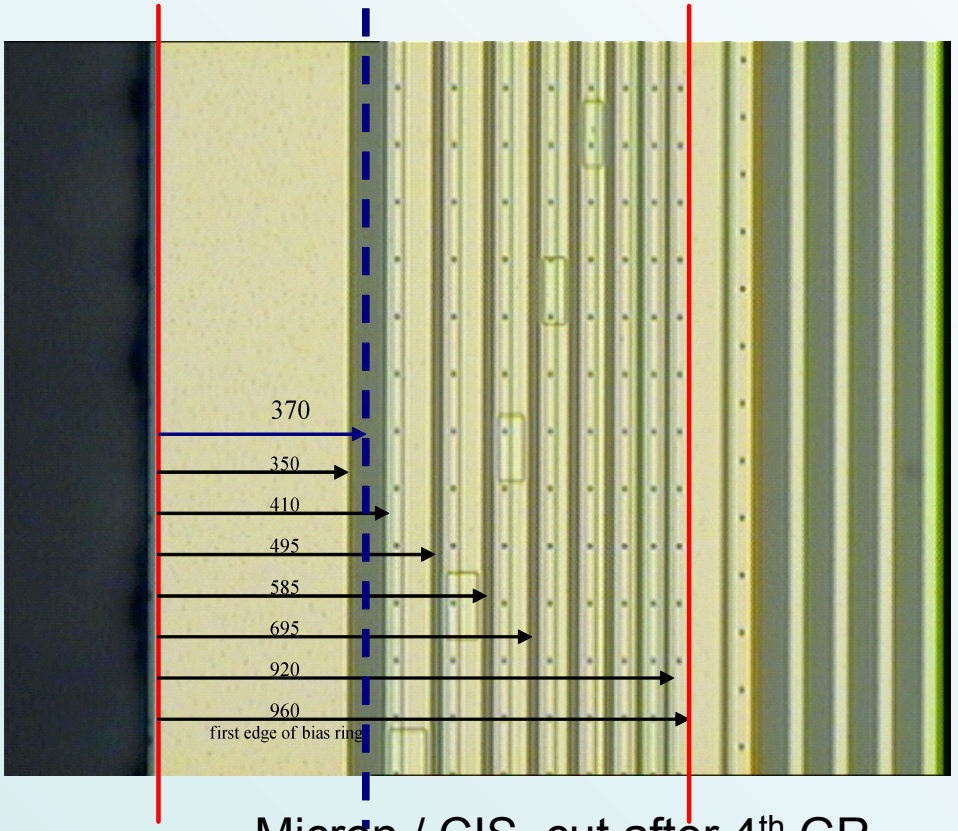
[From G. Aad et al., "ATLAS pixel detector electronics and sensors", JINST P07007]

Sensor Layouts

- Two types of (strip) sensors were used in this study:
- HPK with 1 GR
- CIS and Micron with 8 GR



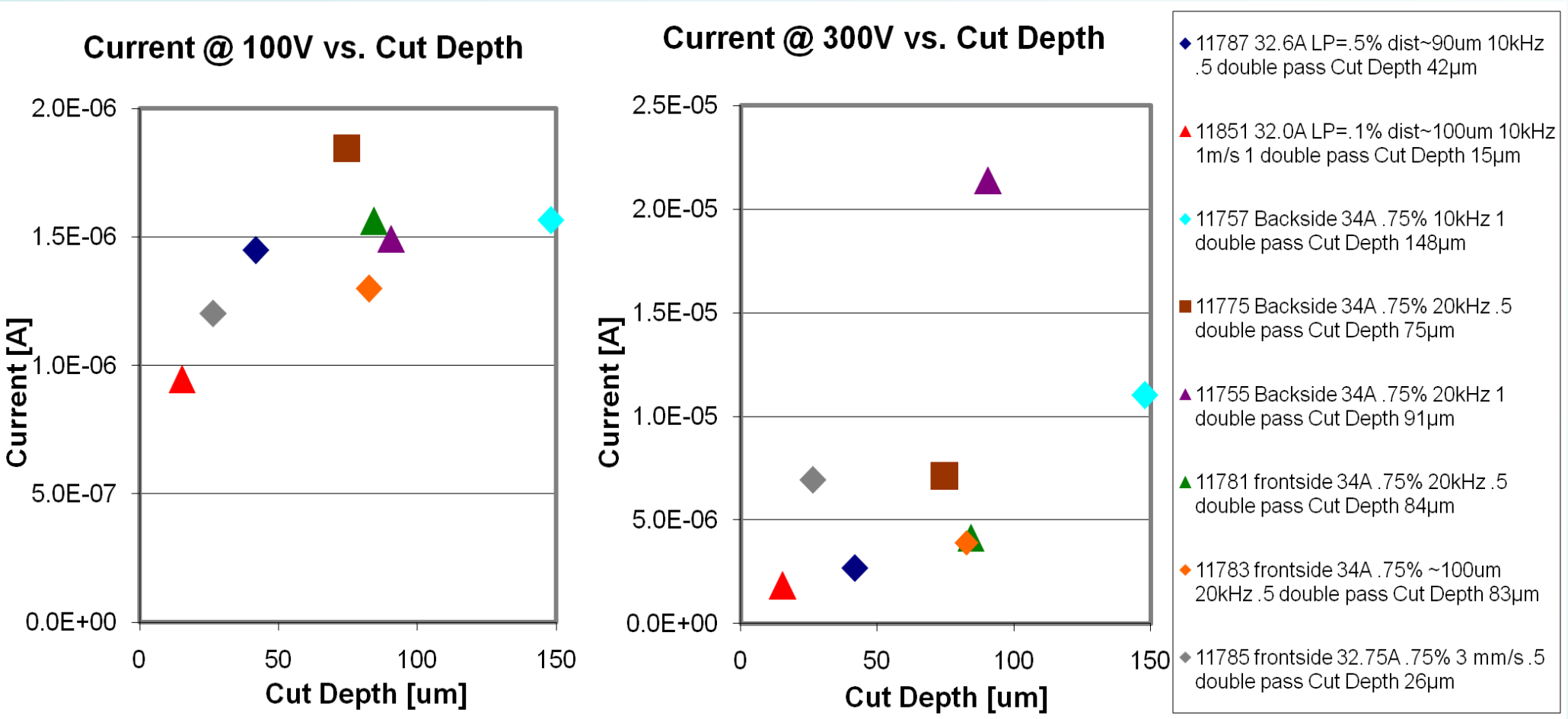
HPK, cut in the middle of unimplanted zone



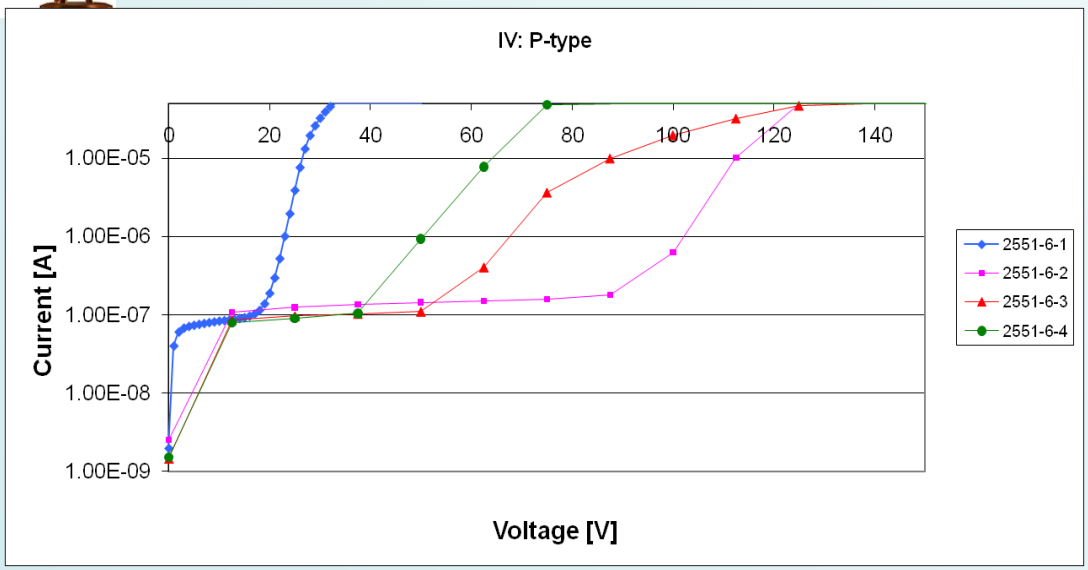
Micron / CIS, cut after 4th GR

Scribe Depth Dependence

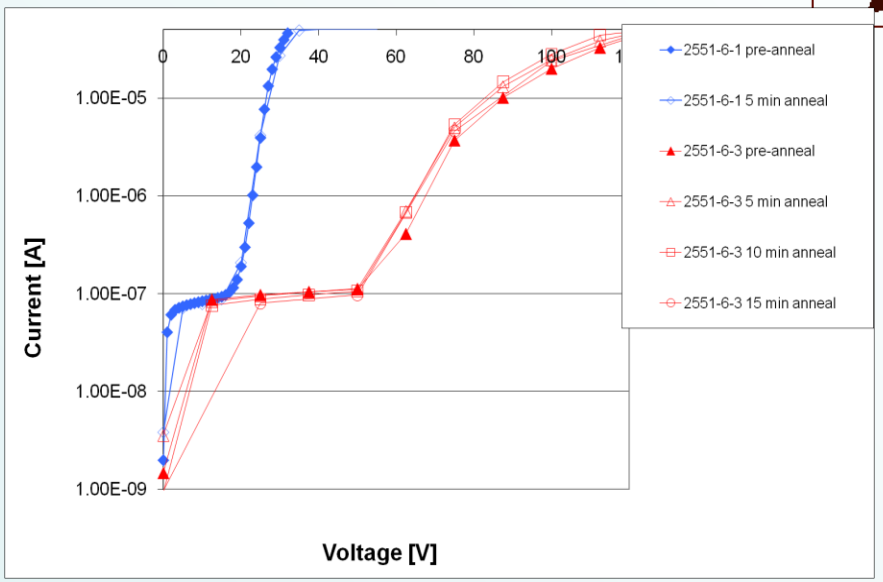
- Lower laser power might be just a proxy for shallower scribe depth.
- Minimal reliable cleavage with d = 26 um.



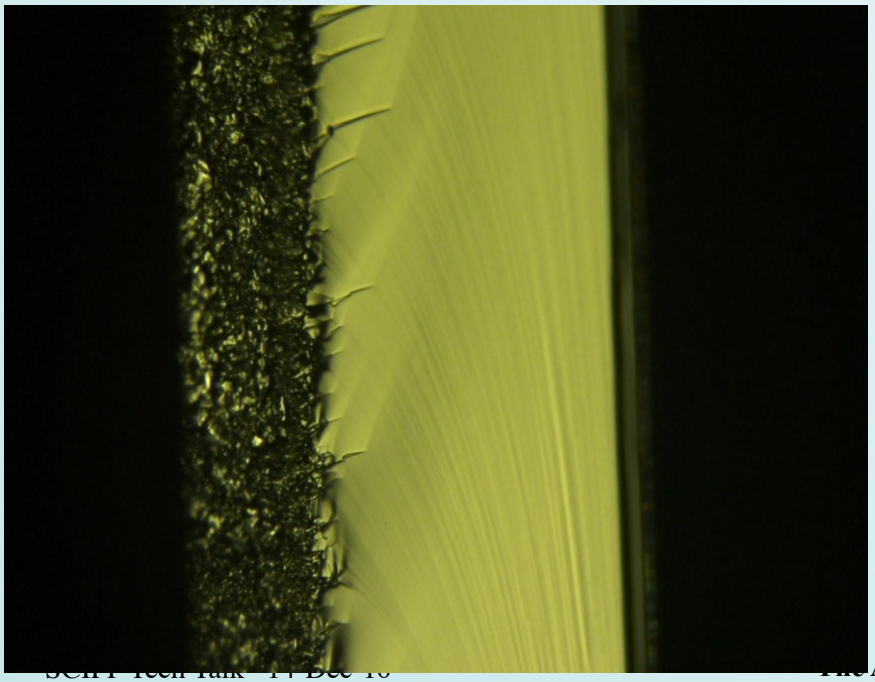
Micron (p-type) sensors



Breakdown at 20-120 V.



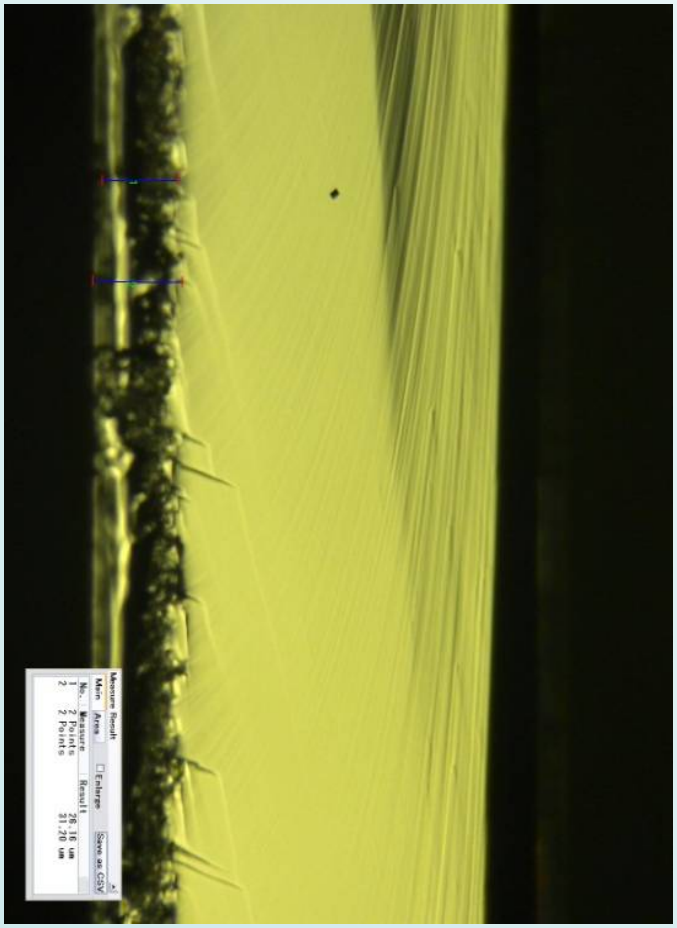
No improvement with annealing.

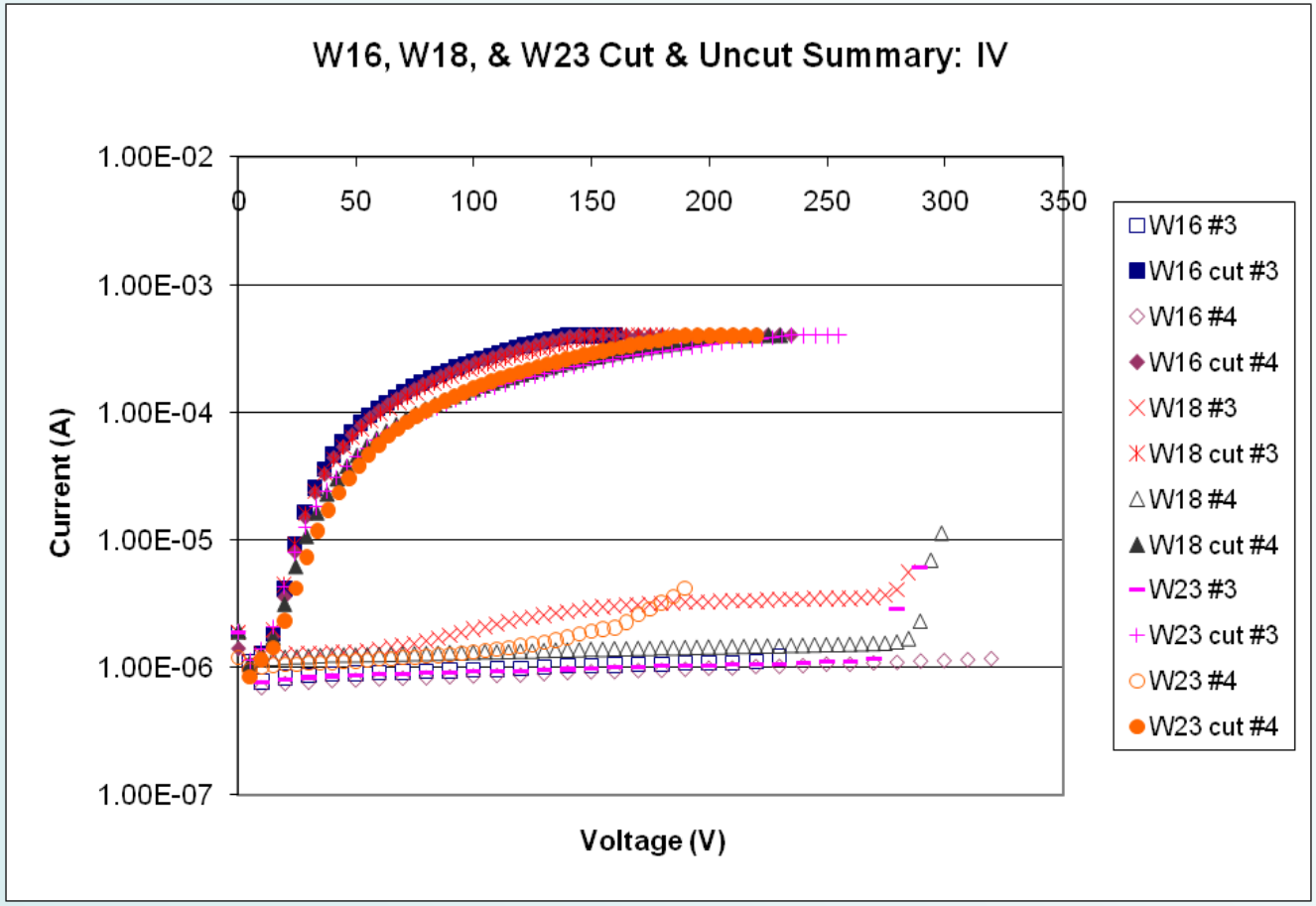


- Relatively early breakdown, 20-100 V.
- Similar visual cut quality.
- No improvement with thermocycling.

"streaks" even for visually best sensor (#2 in the plots)

CIS sensors (p-type)

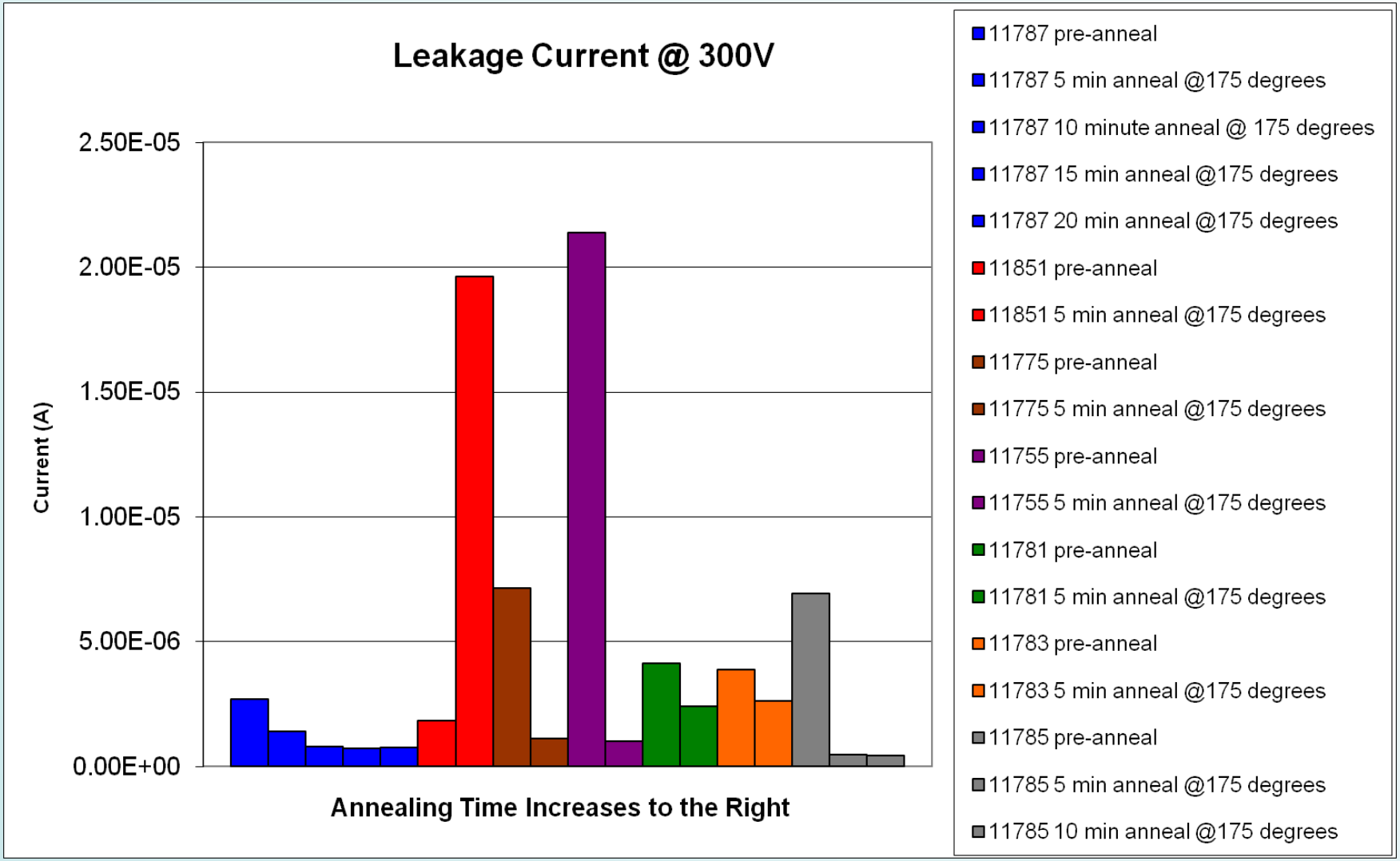




- Some of the sensors showed a relatively early breakdown voltages of 200/300 V before the procedure
- Processed sensors show a uniform early breakdown at ~20 V

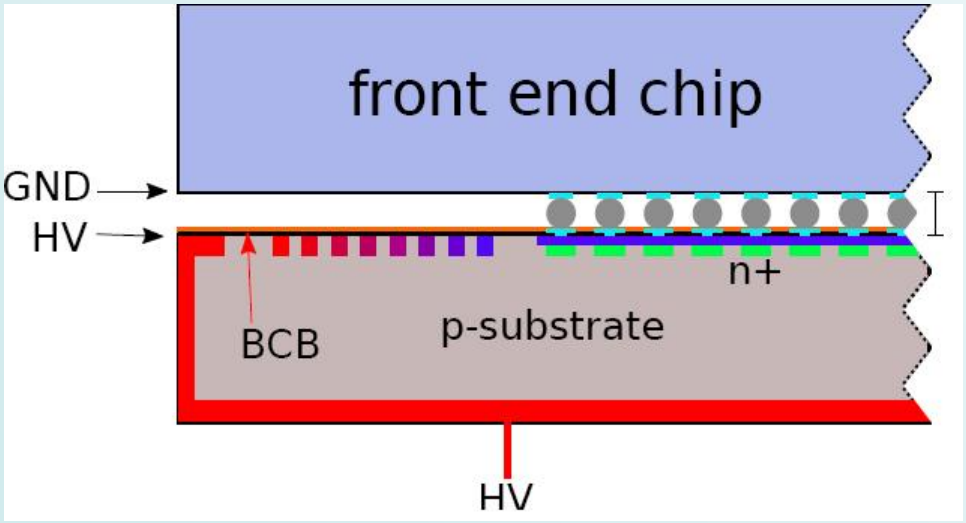
Post-cleaving Treatments (n-type)

- The improvements in leakage current are likely due to oxide formation in the cleavage plane resulting in a “inactive” surface (E. Yablonovitch *et al*, Phys. Rev. Lett., Vol. 57, p. 249 (1986).)



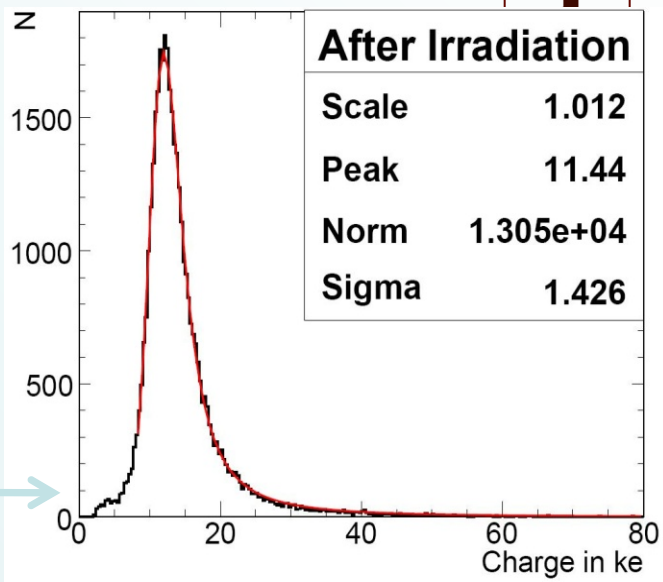
N-on-p Sensors

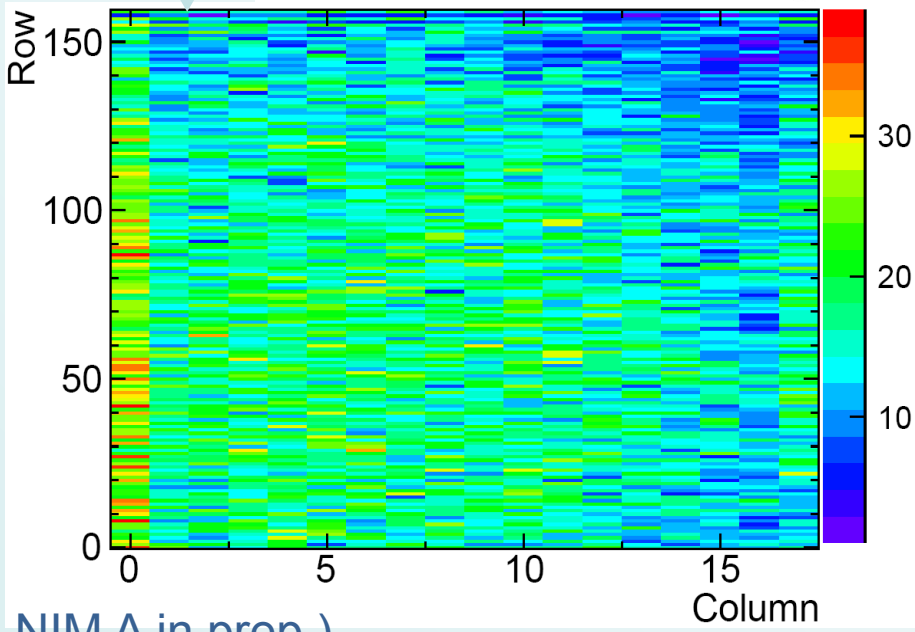
- Attractive due to cost (single-side processing)
- Unique challenge: HV from the back side in close proximity to the FE.



Solution: Cover the sensor with a thin layer of BCB (BenzoCycloButene).

After proton irradiation to $1x10^{15}$neq/cm^2 , at 550 V.



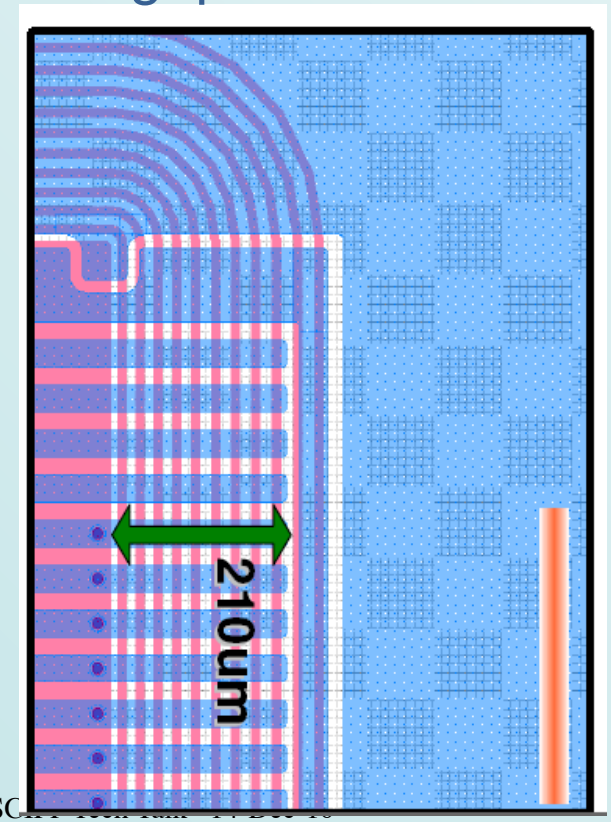


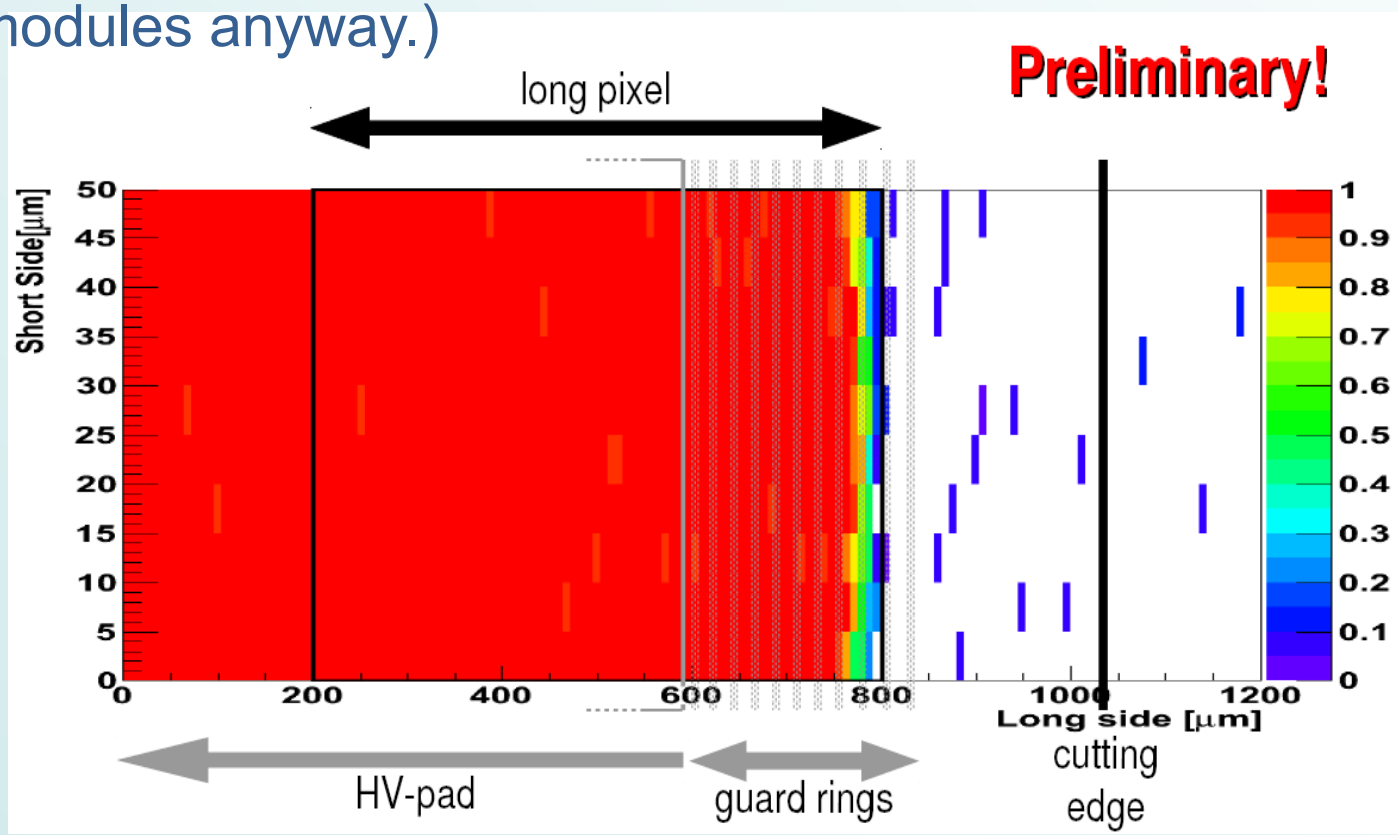
Tested up to 700 V (Munich) ->
No sparks seen!
Further tests after irradiation.

Proceedings to RESMDD 2010 (P. Weigell *et al*, NIM A in prep.).
Further details on BCB: Anna Macchiolo (PPS – Hamburg).

Slim Edges

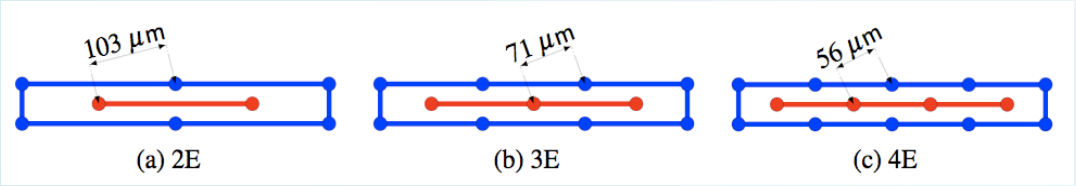
- N-on-n design to limit the amount of inactive periphery:
  - Reduced number of Guard Rings (GR) on the back side
  - GR location is shifted under the outer pixels.
  - Saw cut location only 200 um from the pixels.
- Observe no loss of efficiency until ~170 um from the HV pad.
- Expect to limit inefficient edge to 200-250 um. (There is a ~100 um gap between the modules anyway.)

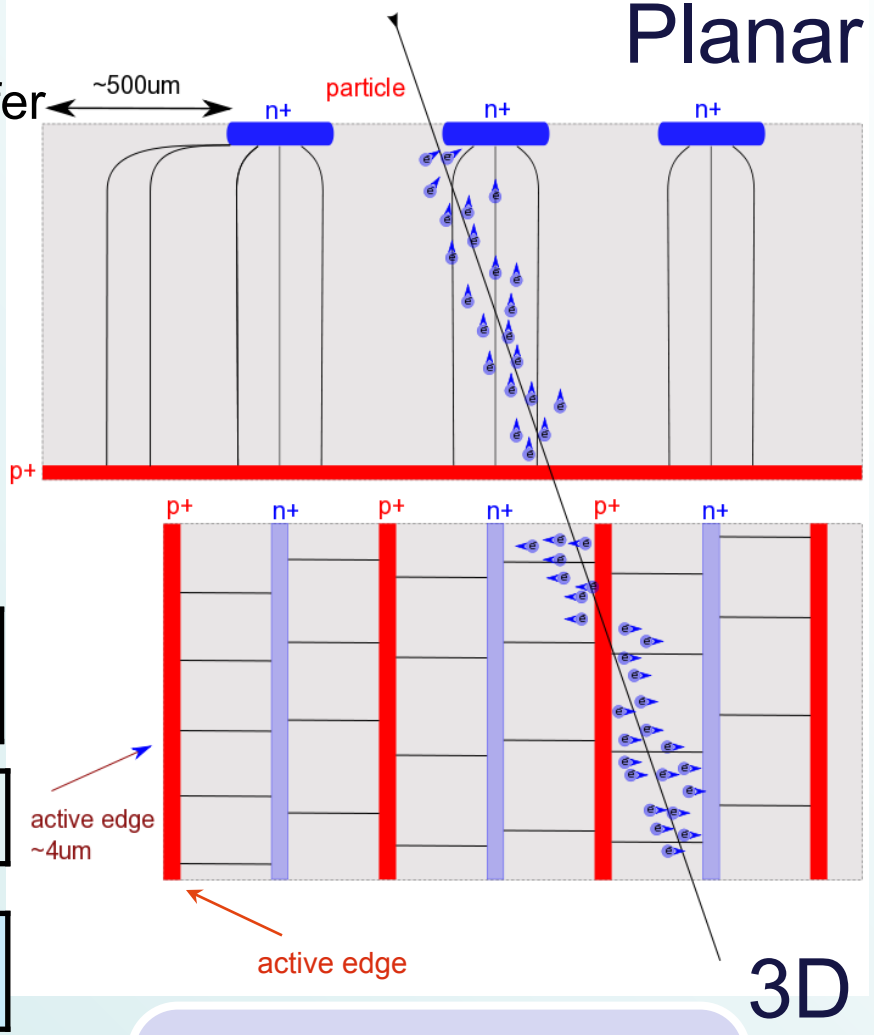




3D Sensors Principle

- Proposed by Sherwood Parker et al.: NIM A 395 (1997) 328
- Very advanced technology
  - Electrodes (both types) processed inside the wafer bulk - perpendicular to surface
  - Different cell configuration: 2E, 3E or 4E





Advantages:

3D Features:

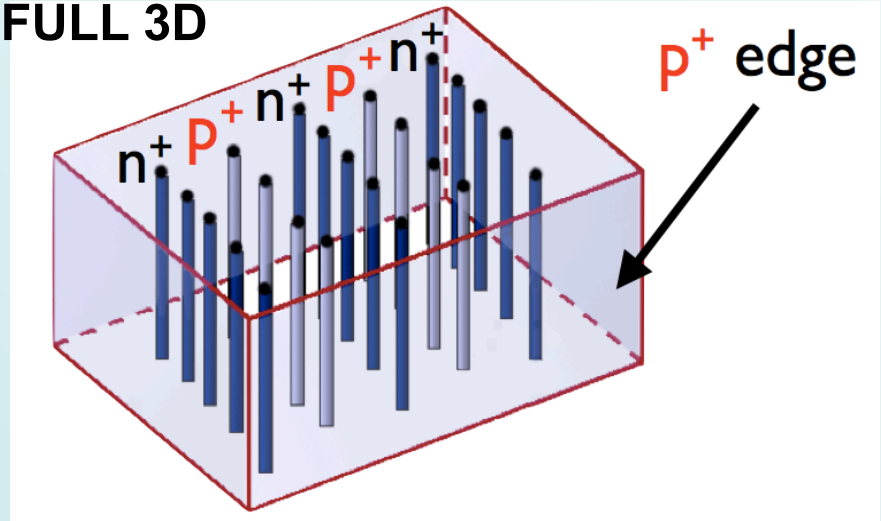
3D Features:	Advantages:
high electric field	high efficiency / radiation hard
short collection path	lower depletion voltage
sensor edge is an electrode	faster charge collection
	active edge ~4μm

This and the following 3D slides are from Andrea Micelli's talk at Pixel 2010.

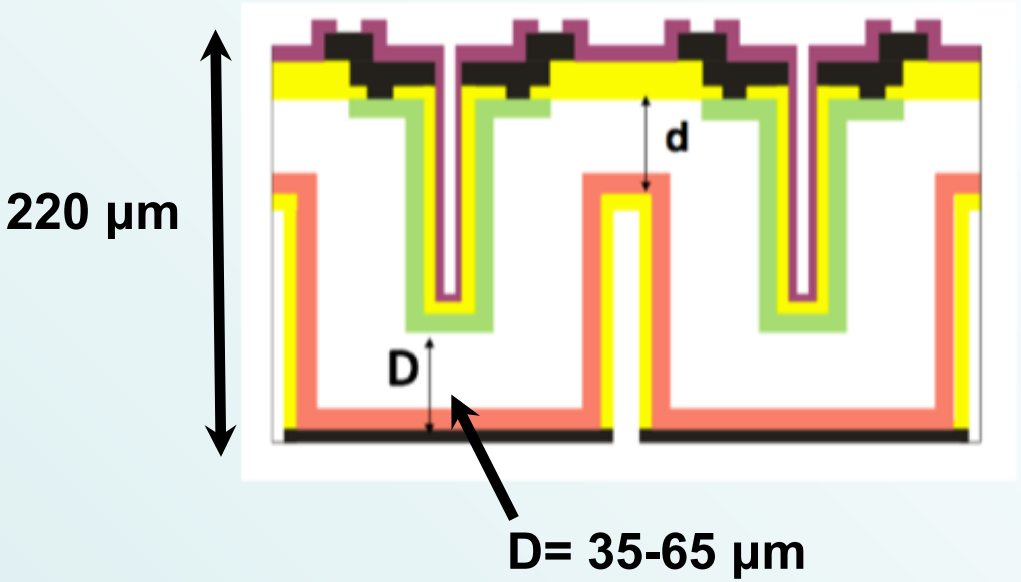
3D Sensors Designs

- Two designs under study - similar behavior and performance

FULL 3D



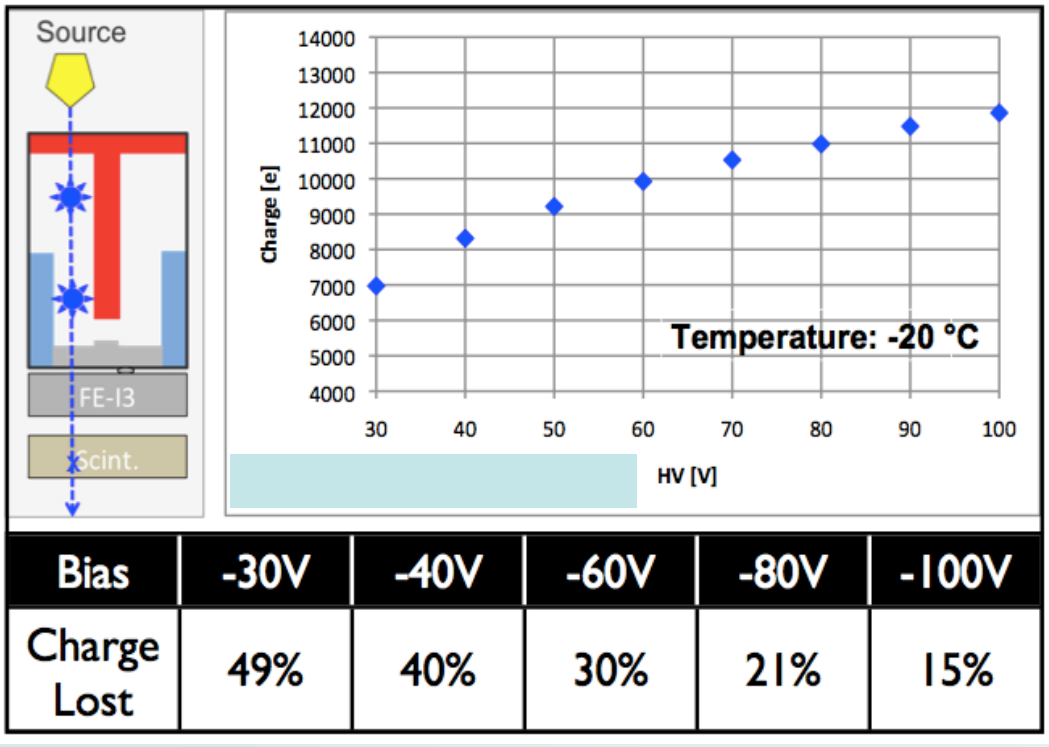
Modified 3D sensors



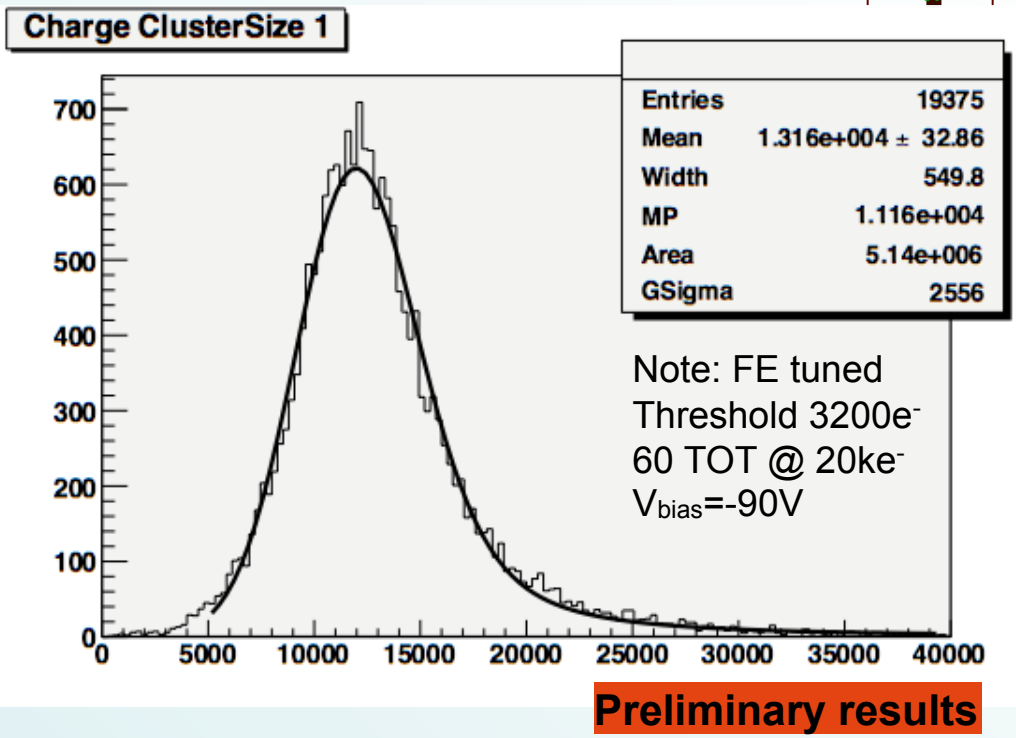
- agreed on "baseline" sensor produced by Stanford/SINTEF (5th gen.) to-be-produced by FBK and CNM
- same dimensions and read-out:
  - 160×18 pixels, each 50×400 µm²
  - bump-bonded to ATLAS FE chip
    - ➡ time-over-threshold (ToT) signal
    - ➡ 60 ToT @ 20 ke⁻, threshold = 3200 e⁻

- partially overlapping electrodes
- simplified wafer handling
- double-sided double-type columns
- produced by FBK and CNM

Lab Measurements



Bias	-30V	-40V	-60V	-80V	-100V
Charge Lost	49%	40%	30%	21%	15%



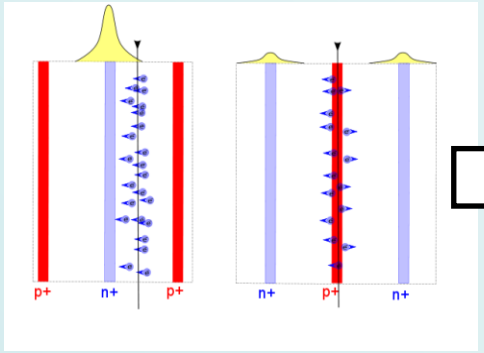
3D-FBK-3E proton-irradiated to 1×10^{15} $n_{eq}cm^{-2}$ (thickness 200μm)

- radiation damage: run with bias voltage -80 V
  - ~ 20% signal loss
    - ➡ in agreement with lab tests made with β source Sr^{90}
  - sensor was not fully depleted
- overall efficiency still high (~99%)

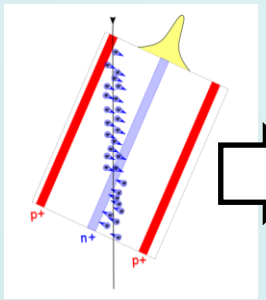
Test Beam Studies: Tracking Efficiency

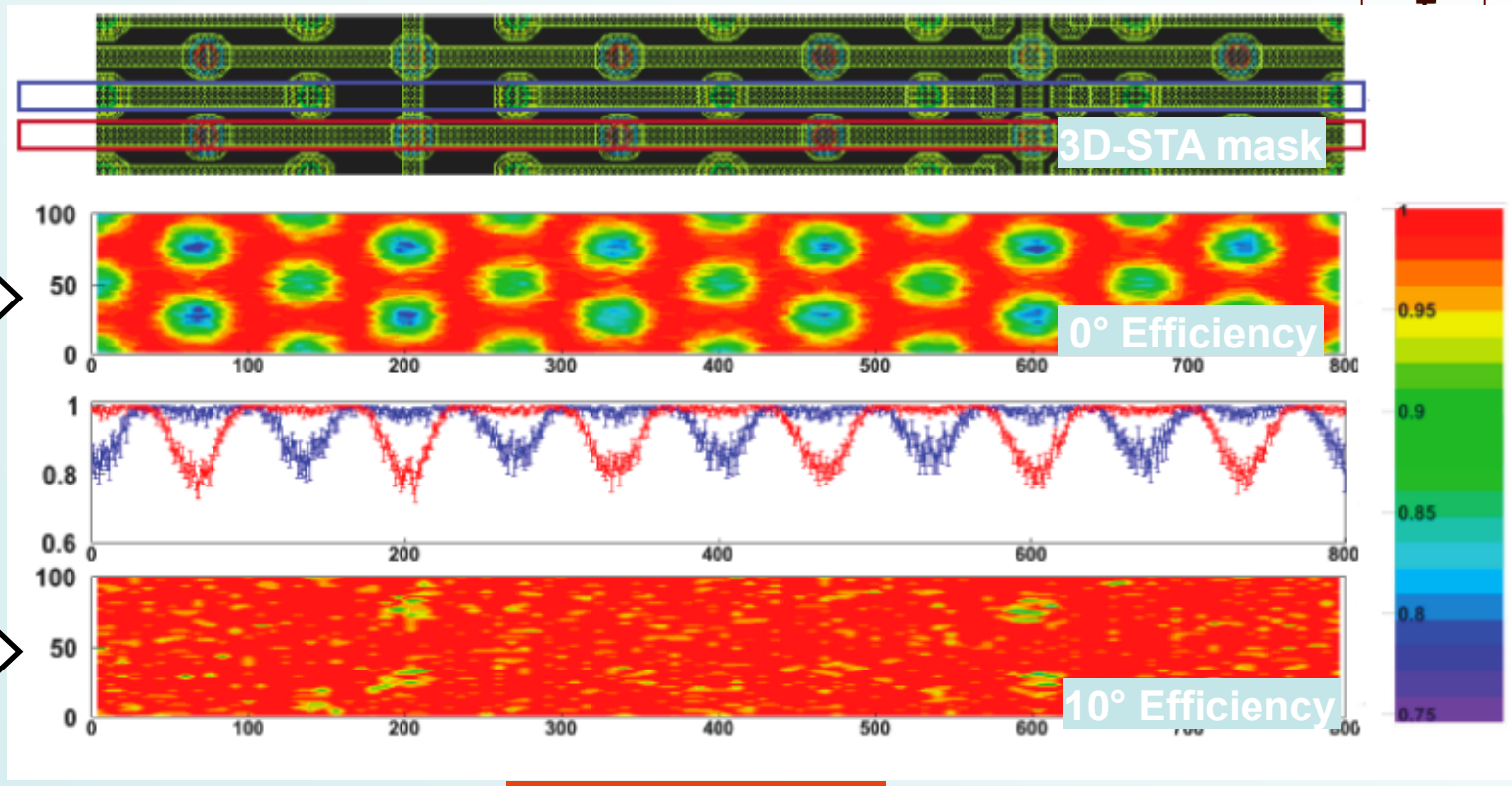
STA eff.

∠0° => av. eff. 95.6%



∠10° => av. eff. 99.9%



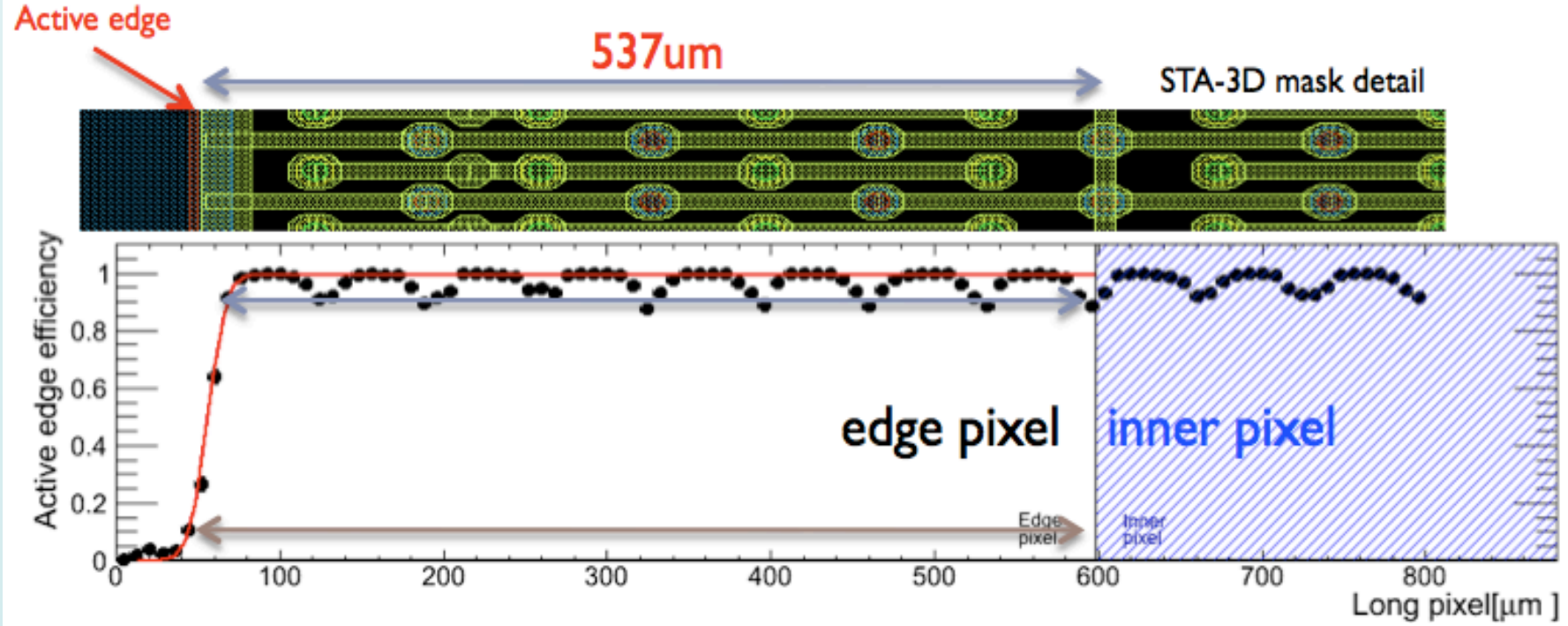


Preliminary results

3D sensors:

- lower efficiency for 0° (not 'uniform' color for the plot)
  - a lot of charge/signal loss for tracks
    - ➡ charge below the threshold
- tilt angle has large impact
  - hit efficiency becomes more uniform when the tracks are inclined

Active Edge



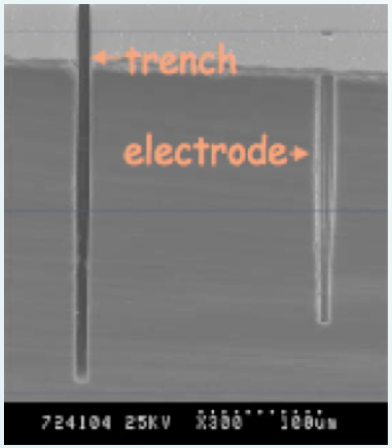
P. Hansson, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.06.321

- Traditional Si sensors have large dead region at edges (~1mm)

- ATLAS IBL has no overlap in z coordinate (along the beam)

- 3D sensors with active edge:
  - etched trench around sensor edge, doped similar to electrodes
  - minimize dead area between modules (IBL)

➡ sensors is still active up to 6 µm from edge



SLVS Advantages

- Regardless of the data transmission, SLVS has other advantages:
  - Thin-oxide transistors are expected to be more rad. hard than thick-oxide transistors at 130 nm.
  - SLVS could be made entirely from thin-oxide transistors.
  - This also means that only 1.2 V power supply is used, with benefits for power consumption and system simplicity.

CERN-made SLVS buffer

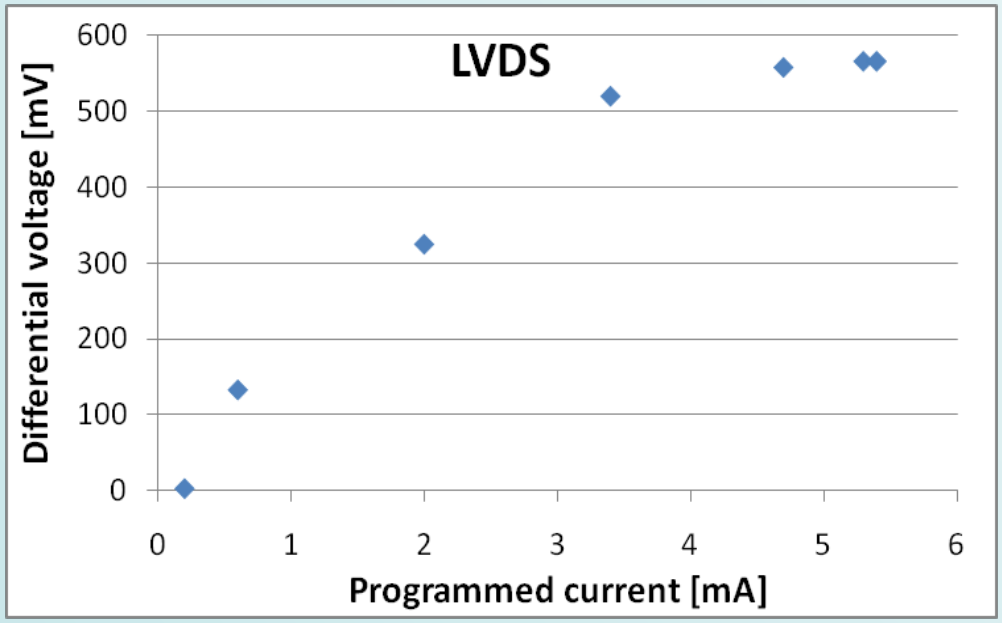
- Implementation similar to SLVS-200, but without source termination to GND.
- Scalable source current between 0.5 mA and 2.0 mA.
- TWEPP'09: S. Bonacini, K. Kloukinas, and P. Moreira,"e-link: A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication"

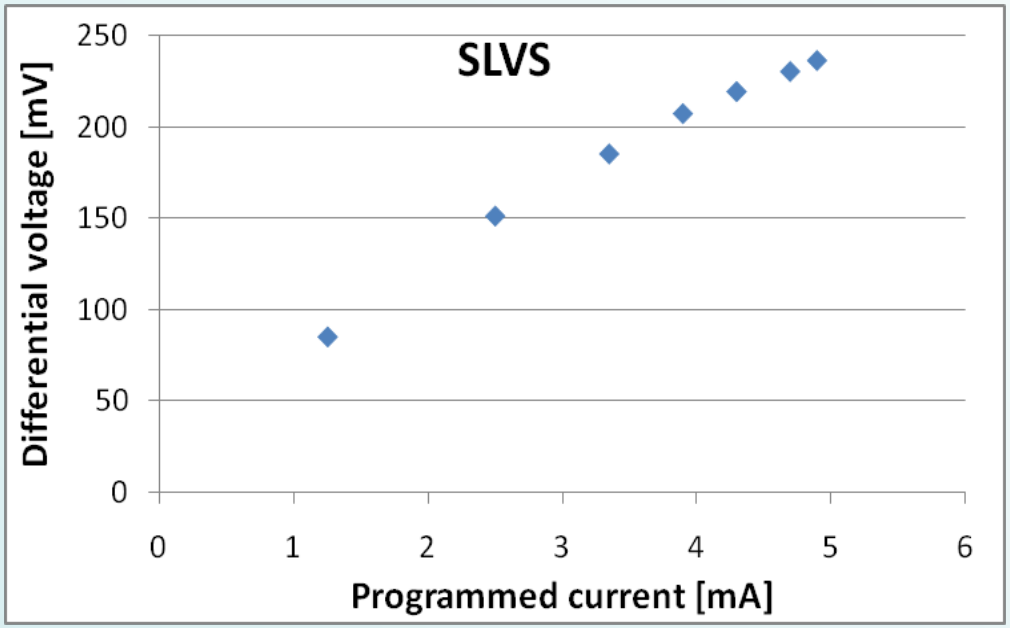
- We received 2 chips from Sandro.
- Arggggh! They did not work. Were tested before shipment.

- Thin-oxide transistors at 130 nm are known to be extremely sensitive.

AUEIO Chip Performance

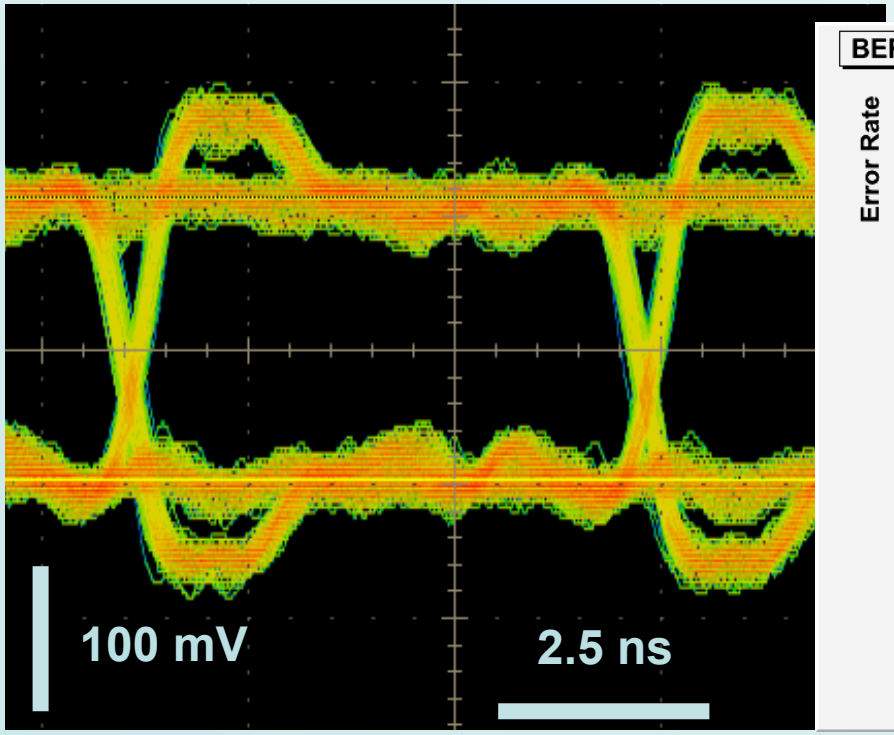
- LVDS diff. output between 130 and 570 mV.
- SLVS diff. output voltage between 85 and 240 mV (across 100 Ohm differential termination).
- Rise time of 170 ps for SLVS signals and 270 ps for LVDS
- Could drive 880 MHz clock through the output.



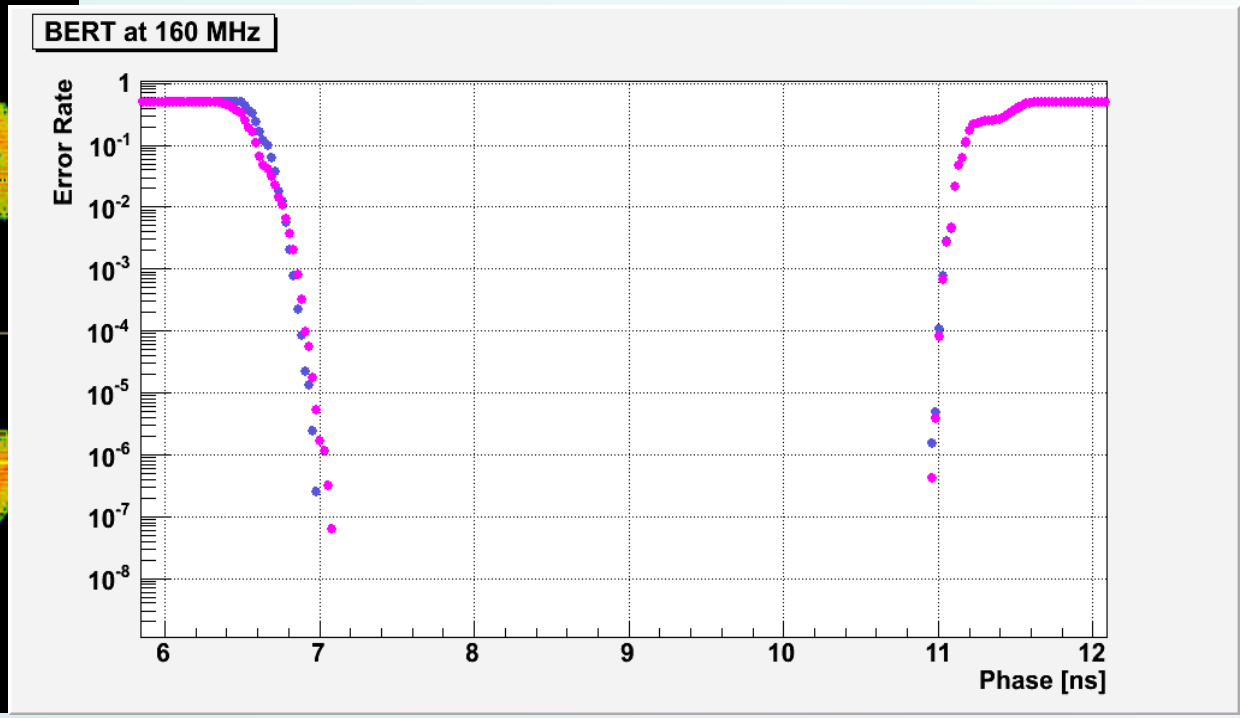


LVDS Tests

- AUEIO chip in place of hybrid # 2.
- BERT at 160 Mbps. Data broadcast on multi-drop line with a return via point-to-point link.
- Nominal performance is ok even at lowest setting of 1.5 mA.



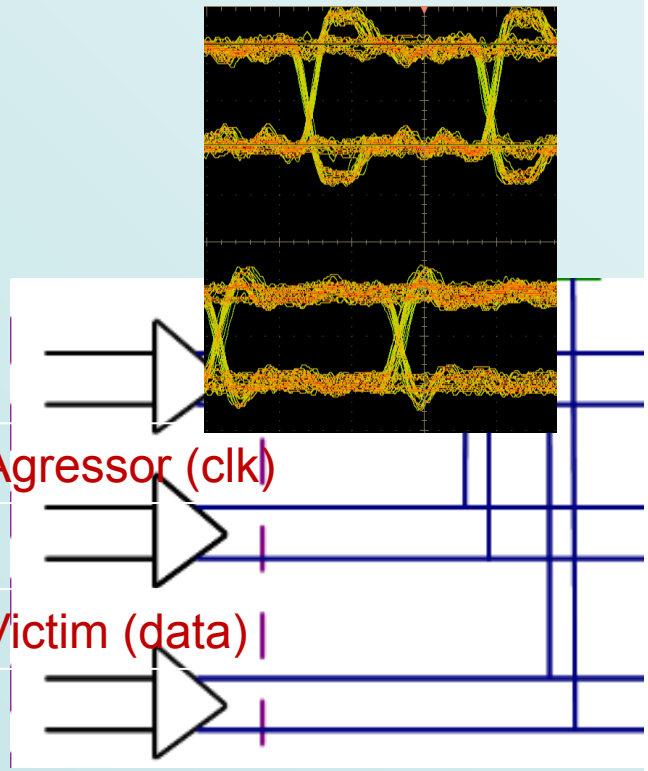
Eye diagram at i=1.5 mA

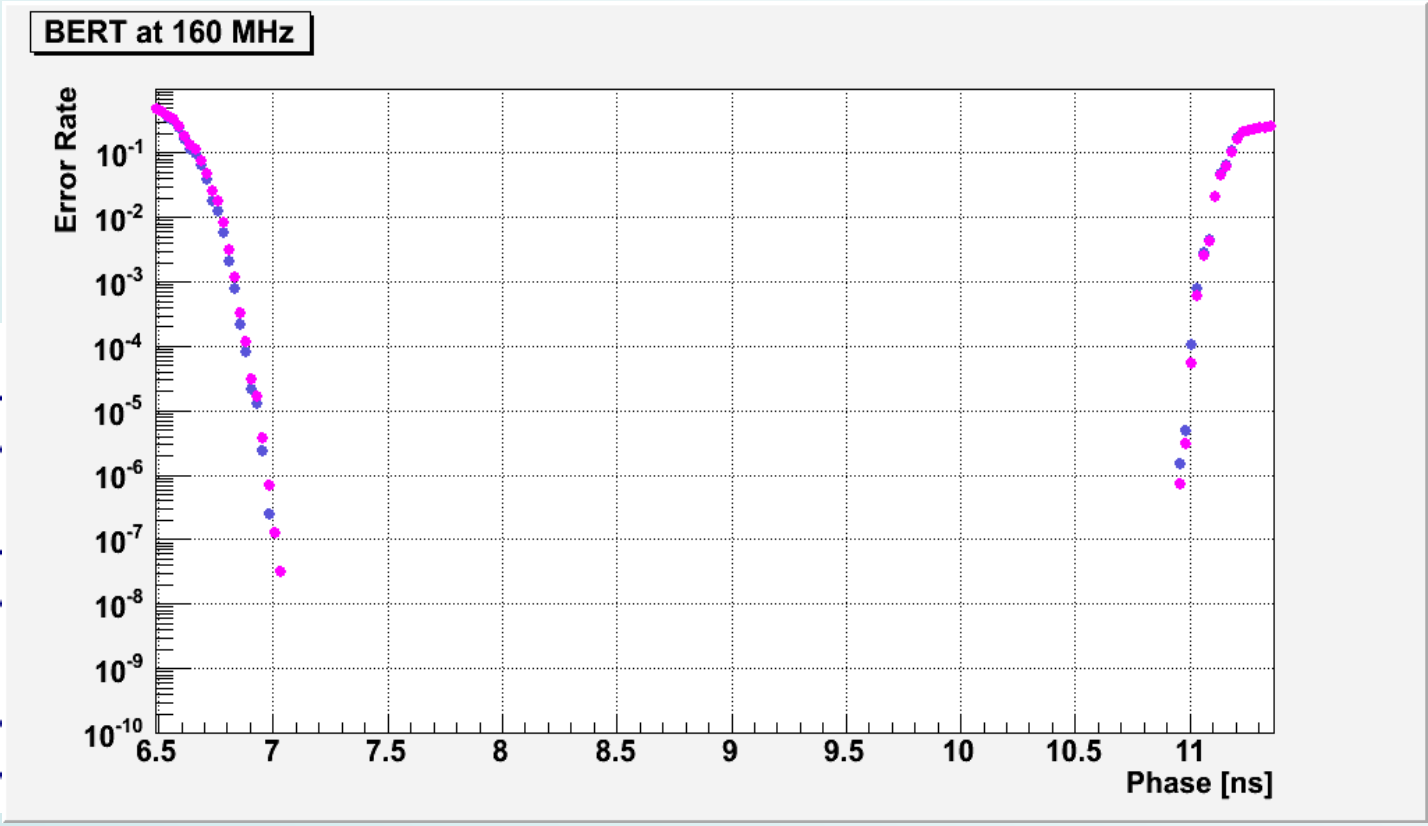


BERT comparison at I = 1.5 mA (blue) and I = 3.1 mA (red)

Cross-talk Measurements

- AUEIO chip in place of hybrid # 2.
- Stimulating a neighboring multi-drop line by a phase-shifted data. Ran BERT at 160 Mbps with LVDS line at lowest setting of I = 1.5 mA.
- No effect.





SLVS BERT comparison with (red) and without (blue) crosstalk