

Thoughts on Data and TTC Transmission for the Upgraded ATLAS Inner Detector

Alex Grillo

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These are some thoughts about how we might modify the architecture of the transmission system for data (going out of the detector) and TTC (clocks, commands, configurations going into the detector) for the upgraded ATLAS Inner Detector (ID). The perspective is mostly from that of the SCT experience but I think most concepts would apply to both pixels and strips for the upgrade. The details (e.g. level of multiplexing) may be different for each, but it might also be different for the mid-radii strips and the outer radii strips. These ideas are based upon keeping the concepts which are worthwhile from the present scheme, improving (hopefully) some of the concepts which have proved to be problematic and taking advantage of the advance of technology within the constraints of the upgrade program.

Some ideas have been expanded and some revised since the 11-Sep-05 draft. I have also had useful discussions with Tony Weidberg of Oxford and with him and others at the meeting organized by Francis Anghinolfi during ATLAS ID Week of Sep-05 concerning the “SCT Upgrade: ABCD Next”. Some issues raised in these discussions have been included. More feedback is most welcome as this is intended to be a discussion note.

1. Robustness

We began the development of the present ATLAS-SCT transmission architecture with a few general guidelines which we thought would enhance the robustness of the system against common failure modes. These included:

- a. Avoid shared parallel write busses where one failed IC tends to take out the whole bus, i.e. use serial data paths.
- b. Provide redundant data transmission paths onto and off of the detector.
- c. With the whole tracking detector segmented into smaller units (i.e. a detector module) and with this unit containing its own isolated power and reference potential, employ optical transmission for all high speed communication between the detector unit and the off detector electronics. This not only might save some services volume (fibre vs. wire) but it minimizes interference between different detector units thereby making scale up to a large system based upon test results of a small subset more viable. It also does not increase power over electrical readout.
- d. Provide a mechanism whereby a failed IC will not kill a much larger unit of the detector, i.e. a full module. Thus some way for the serial data stream to bypass a dead chip should be employed.

- e. In order to minimize electrical noise, all electrical communication between ICs or between the detector units must be via low amplitude fully differential signals. Something roughly matching the LVDS standard was adopted.

2. Transmission data rates and multiplexing

The natural clock frequency of the readout ICs is the beam crossing frequency or perhaps x2 the beam crossing frequency. The SCT now transmits data at 40 MHz (1xf) and the Pixels at 80 MHz (2xf). The beam crossing frequency could become 67 MHz or 80 MHz (100 MHz has also been mentioned but I think that is unlikely) in the upgraded detector. Optical transmission technology now typically runs at data rates of several hundred MHz to a few GHz. Provided that such data rates are achievable with radiation hardened hardware, we should try to make use of these higher data rates to reduce the number of fibres required, however, we should try to maintain some level of redundancy.

Operating the fibres at ~GHz speeds implies some multiplexing of serial data streams running at 10s of MHz into one stream running at 100s to 1,000s of MHz. This can be accomplished by an additional multiplexing IC with n inputs and 1 output. A schematic of this is shown in Figure 1. The serial data streams between the ICs and the multiplexer can remain LVDS. It should be possible to design a quasi LVDS transmitter for each readout IC and a receiver for the multiplexer such that a dead or noisy readout IC stream can be masked out at the receiver end and not kill the operation of the multiplexer for the other n-1 data streams. The multiplexer can be designed to always cycle through all of its input channels inserting a "0" in the time slot for each channel which is masked off, or it can be designed to skip over the masked off inputs. I prefer the first alternative even though it may transmit extra 0s because it doesn't confuse the entire data stream if the mask register should suffer a bit-flip error. A method needs to be designed to synchronize the transmitting multiplexers and receiving (off detector) de-multiplexers. I think this can be accomplished by a command to the multiplexer which resets its channel pointer and produces a recognizable output pattern (e.g. a long string of 0s followed by a complex alternating pattern) which the receiver can use to synchronize.

The specific number of readout chains multiplexed into one optical link and the number of readout ICs in each chain will depend upon the final detector layout chosen and may be different for different radii of the detector. The required data rate for each chain and for each optical link will depend upon those choices and may actually constrain those choices. Therefore, it would be useful to determine what are safe operating limits for both data rates. If, for example, 160 Mbits/s operation for each chain is achievable, that may afford more flexibility in the detector layout.

3. Bypass of failed ICs

The present SCT readout allows for any single IC to be “bypassed” if it should fail. This is done by switching the output data stream from the “normal” output pads to the “bypass” output pads, and likewise for the receiving pads, on the ICs on either side of the failed IC. While the normal output pads are routed on the hybrid to the adjacent IC, the bypass pads are routed around the adjacent IC to the next IC in the chain. This has worked reasonably well but has created the following difficulties:

- a. The layout of the hybrid circuit has added complexity with the addition of four extra traces (2 for differential data and 2 for differential token passing) for each IC and these additional traces are longer than the “normal” data/token traces as they slip under one IC in order to connect two non-adjacent ICs. The differences in capacitive load of the normal and bypass traces required slightly different designs for the two drivers/receivers in order to keep power to a minimum.
- b. The connections to bypass an IC at the edge of the hybrid required very long traces. These long traces required a much more powerful differential driver (i.e. more power consumed) and these signals became the function limiting the operational speed of the IC.
- c. Some of the redundant paths so complicated the topology of the hybrid layout that one was not implemented precluding the bypassing of one IC.

A simpler bypassing scheme, which was employed by the BaBar silicon readout, would be to define two different directions for the data stream (e.g. to the right and to the left of each IC). Normally, half of the ICs send data to the right and half to the left. If an IC should fail, the data flow direction of some ICs are changed such that all to the left of the dead IC send data to the left and all to the right of the dead IC send data to the right. This is illustrated in Figure 2, where one IC in the third chain is marked as “dead” and the data flow arrows are modified accordingly. This does not decrease the number of drivers and receivers, nor the number of traces, however, to first order all traces simply connect adjacent ICs with no circuitous paths. However, if a given serial chain includes ICs on two sides of a detector module or on different physical hybrid segments, there will still be some long lines that the drivers/receives must accommodate.

Thinking further about this issue of a long connection to the next IC on the backside of a module or a different physical hybrid, we could redefine the datalink output of the present ABCD IC. The IC now has three data outputs: dataout to the adjacent IC, dataoutBP to bypass the adjacent IC and datalink to the optical driver. The datalink output is only used when an IC is a Master and it must then be connected to the optical driver and not another IC in the chain. If we generalize this third output such that any of the three outputs can be used to

connect to the next IC in the chain or the multiplexer, this third higher-powered output can then be used whenever the connection is going to be a long run.

Combining the concept of right vs. left data flow with the generalized third output for longer runs, there would be three independent controls: one to switch directions between right and left, one to use the higher-powered output (the old datalink output) instead of the normal right or left output and a third to specify a Master IC. Only two of the three outputs would be connected to other ICs or the multiplexer. If the Master operations (e.g. initiating the token and placing header information at the beginning of the serial data stream) are moved to the multiplexer (labeled ComCon in Figures 1 and 2) the third control will not be needed.

With this scheme, the normal output drivers can be designed for minimum power to only drive a signal to the immediately adjacent IC. The third output can be designed to use more power to drive a long line but it will only be powered when needed. This should minimize power and avoid the issue of the bypass drivers of each IC having to drive varying line lengths depending upon topology. The high powered driver will only be powered when needed and only on the few ICs with a long connection.

One last point is that fully intact readout chains could be initially configured to only drive data in one direction. The split data flow (i.e. part of the chain sending data to the right and part to the left) need only be activated when one IC in the chain is dead. This doesn't change the bandwidth requirement since the redundancy of optical links requires sufficient bandwidth for all chains to send data in only one direction if necessary. This would reduce the power consumption of most chains but probably would not reduce the overall services for power and cooling capacity unless that capacity is established on a statistical basis of expected IC failure rate.

4. Configuration read-back

The present SCT readout IC, the ABCD, does not allow for read-back of its configuration registers. Tests for single event upset in a particle beam have indicated that we should not have a problem if we periodically reload the registers. The higher fluences of the upgraded ATLAS and the smaller geometries of the IC structures could create a worse problem. The worst aspect of not having register read-back is that we cannot tell in situ what the real error rate is. The re-load rate then must be set to the worst case estimate.

Since there will be an even more severe limit on services for the upgraded ID, it will not be practical to add a second output stream for this read-back data. The configuration data read back will have to share the same output stream as the detector hit data.

The readout IC for the upgraded ATLAS should provide for read-back of configuration registers. The protocol developed for the SCT readout provided for such configuration data to be read back but it was decided not to implement this because it required extra circuitry. This part of the protocol should be re-examined to see if it can be improved and then it should be implemented in the new IC design. Perhaps the much smaller geometries of the IC ($0.25\text{ }\mu\text{m}$ or $0.13\text{ }\mu\text{m}$ instead of the present $0.8\text{ }\mu\text{m}$) will keep the overall size of this extra logic to a manageable amount.

5. Command protocol

The command protocol was developed to allow triggers, short commands and long configuration commands to use the same input stream. The primary identifying sequence of three bits was chosen in order to allow consecutive triggers to appear with only a gap of two beam crossing periods. This used to be a requirement of the ATLAS trigger. This was later relaxed to a longer gap so that the Pixel IC, which reached final design after the ABCD, could make use of a longer bit stream making it more immune to bit flips in the command sequence.

It is even more important that the upgraded ID electronics minimize fibres so it will still be a requirement to use a single input stream for triggers and commands. It would be advantageous to enhance the encoding of the primary identifying sequence as the Pixel protocol has done. Assuming that the same 4 period gap between consecutive triggers is maintained, something like the Pixel protocol could be used. The alternative would be to run the input data stream at twice the beam crossing frequency to afford more bits to the sequence. This latter change would also have the advantage of shortening the time to load configuration registers, which may have to be done more frequently than presently planned. Tony Weidberg has pointed out that that increasing the bandwidth of the TTC signals will increase the probability that a single event upset (SEU) will cause multiple bit errors thus decreasing the reliability of the commands. This would have to be studied further before any change is made to the TTC bandwidth. Indeed, it will probably be necessary to study this issue with whatever new technology is used for the on detector circuitry as the smaller geometries now available in IC technologies may be more susceptible to SEU induced multi-bit errors.

6. Encoding of Clock and Command Signals

For the same reason to save fibre count as in the present SCT, the clock and command signals can be encoded on the same optical signal and decoded by the receiving IC. There would be advantages to incorporating the clock and command decoding function and the output data multiplexing function into the same IC, which I have labeled as “ComCon” (for Communication Controller) in Figures 1 and 2. Special commands to synchronize the multiplexer and to set the multiplexing mask would be decoded and executed within the same IC. It may also be useful for this IC to initiate the token passing to the readout ICs and to

supply the header information for each serial data stream. This would move the Master functionality to this IC instead of having it duplicated in each readout IC. If the token passing is initiated in the “ComCon” IC, a token passing signal from the “ComCon” IC would have to be added to each serial data line (DLxA and DLxB lines in the diagrams). Such extra lines are not shown in the figures.

If command decoding and execution will be incorporated in the “ComCon” IC and complete redundancy of data fibres and TTC fibres is to be maintained, clock and command lines will have to run between the two “ComCon” ICs for a particular detector unit. This would be necessary to allow commands sent down one TTC fibre to be executed in the “ComCon” IC connected to the other TTC fibre. These extra lines are also included in Figures 1 and 2.

We should look into not only combining the clock and command signals into one optical signal but to actually multiplexing several command streams together, probably the same number of command streams as we multiplex data streams. This could be important in order to keep the time required to configure the larger number of ICs serviced by the same group of data and clock/command fibres to a manageable level.

The concern mentioned above, raised by Tony Weidberg with regard to increased SEU problems with higher TTC bandwidth, must be understood as well as the expected rate of register re-write, also necessitated by SEUs, so that dependable TTC transmission can be achieved along with adequate performance. The SEU problems with command transmission could be mitigated with appropriate error correction encoding as long as the clock can be adequately extracted; however, this adds a new level of complexity.

Figure 1 shows separate clock and command drivers for each readout chain and then those signals bussed in parallel to all ICs in each chain. It will be important to have separate drivers for each chain in order to provide better isolation of failed chains. Depending upon the final topology of the detector unit, it may also be necessary to provide phase adjustments between the different chains to compensate for different transmission lengths. Whether this phase adjustment is done at the driver or the receiver end, it will be easier to manage if each chain has separate clock and command drivers and if all the ICs in a single chain are physically close together.

These separate clock and command drivers for each chain necessitates a large number of drivers in the “ComCon” IC as well as a large number of differential transmission lines. It has been pointed out that the electrical versions of the clock and command signals could be transmitted using the same biphasic mark encoding used for the optical TTC transmission. This would halve the number of clock/command drivers in the “ComCon” IC and the number of clock/command transmission lines. Assuming that the circuitry to implement this encoding and decoding (or for some other equally suitable coding scheme) is small, this could

save IC area, IC interconnect complexity and power. Such a simplification is shown in Figure 3.

7. Redundancy of Clock and Command Signals

I think we should continue the scheme to provide a redundant clock/command fibre for each detector unit for the obvious reasons. The present SCT scheme has only one fibre per detector module but has a provision for the optical signals of an adjacent module to be used if the primary one fails. This scheme saved one fibre per module (an overall savings of 25% in fibre count) and was primarily implemented to provide a method for synchronizing the clocks (equivalent to beam crossing signals) of adjacent modules. Since the redundant clock and command is passed to each adjacent module in a long chain, many modules can in principle be timed in a bootstrap fashion.

This scheme, however, has some unfortunate side-effects. Since the clock and command signals being passed to the adjacent module are electrical not optical, these signals provide an electrical tie between two modules which degrades the isolating advantage of using optical transmission. The connection of these electrical signals between modules also complicated the mechanics of the cable and fibre harness for each module since these four signals (differential clock and differential command) had to be tied to the adjacent module and the topology of that connection was not identical for all modules.

It would be much simpler if we can keep the clock/command fibres and the data fibres unique to each detector unit. Since the data fibres will multiplex a much larger number of detector channels, keeping two clock/command fibres paired with two data fibres should not increase the absolute fibre count very much. We should analyze the usefulness of the shared fibre scheme when the present SCT is commissioned in the next 18 months to see how useful that scheme is and determine if some other scheme like using cosmic ray tracks can be developed for synchronization.

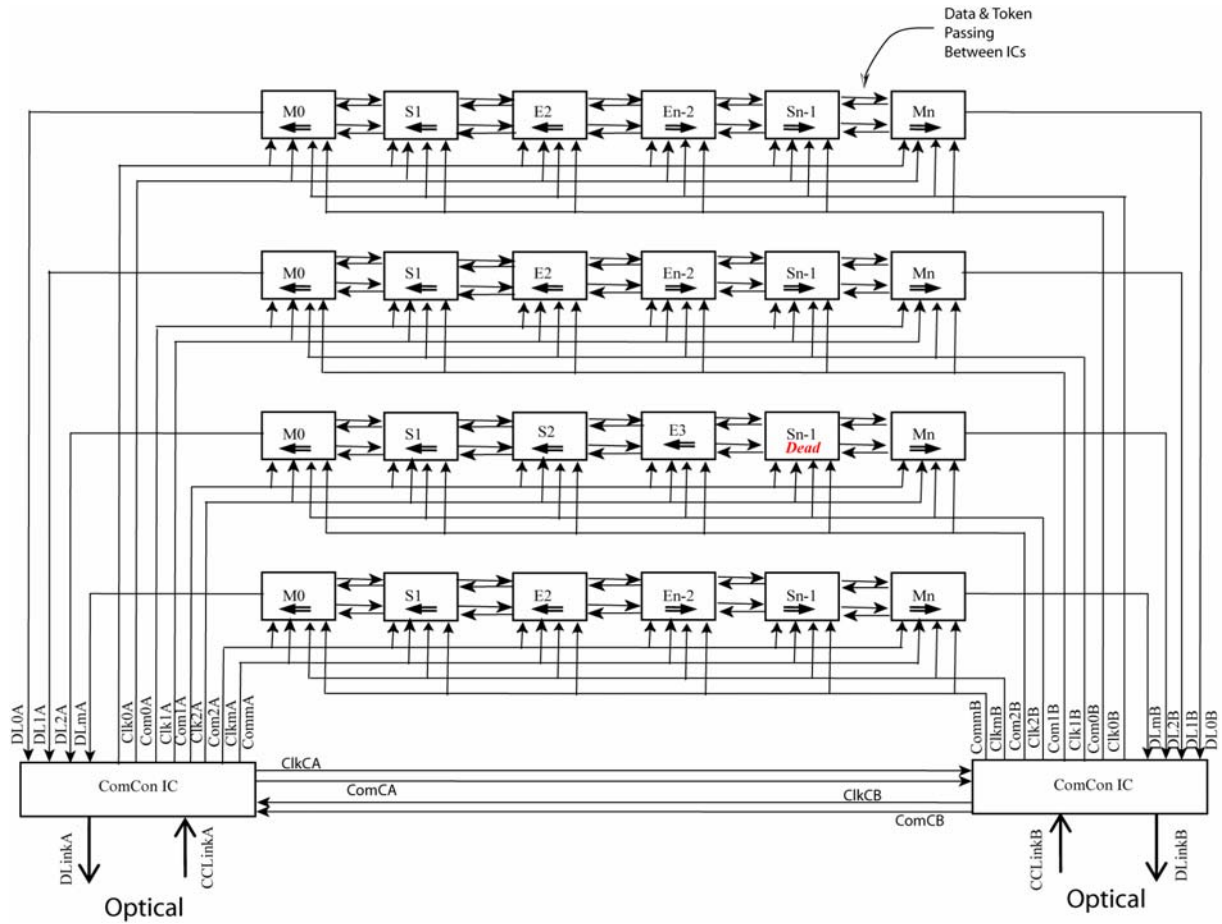


Figure 2: Same Hypothetical Arrangement but with One Dead IC in Third Chain. Data Flow Direction Changed to Skip Dead IC.

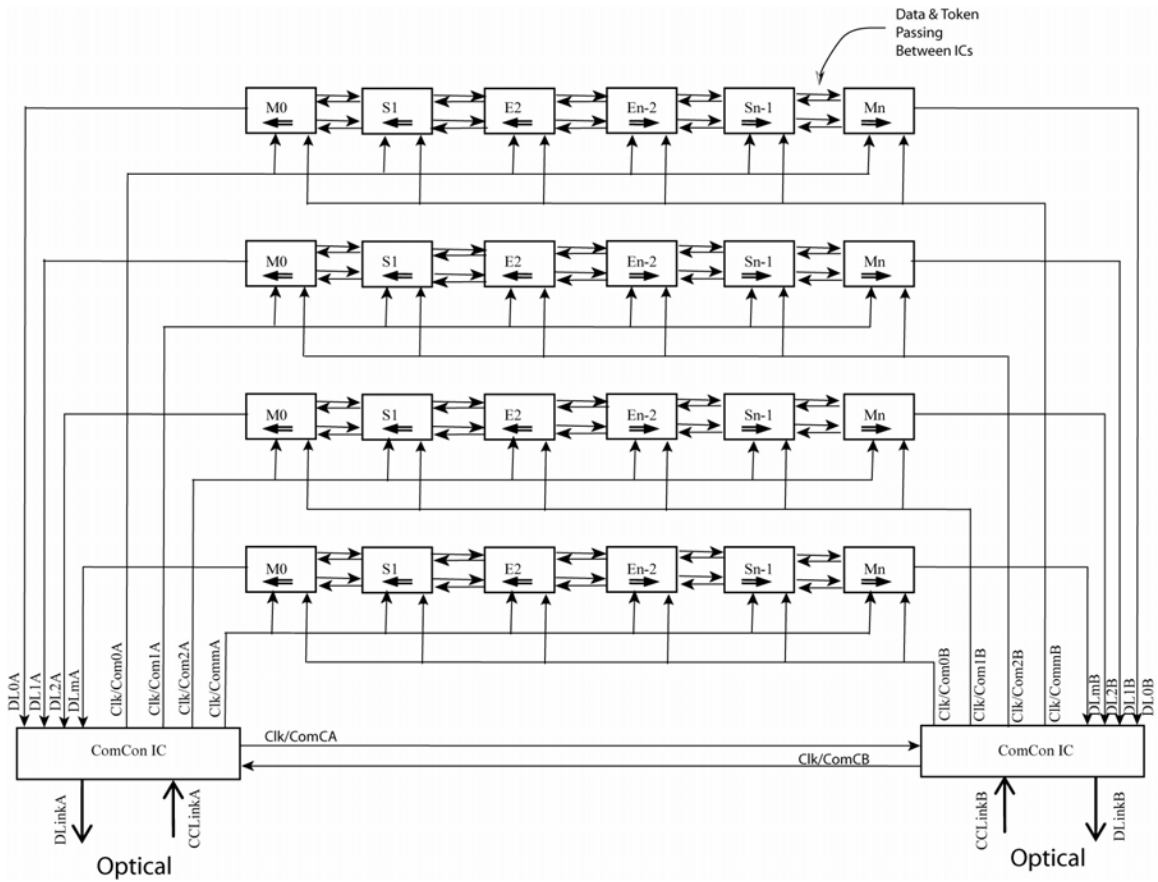


Figure 3: The Separate Clock and Command Lines Driving Each Chain Have Been Replaced by an Encoded Clock/Command Line Saving Drivers but Requiring Each IC to Decode the Clock and Command Signals.