Upgrade Work at Nevis

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IN THE CITY OF NEW YORK

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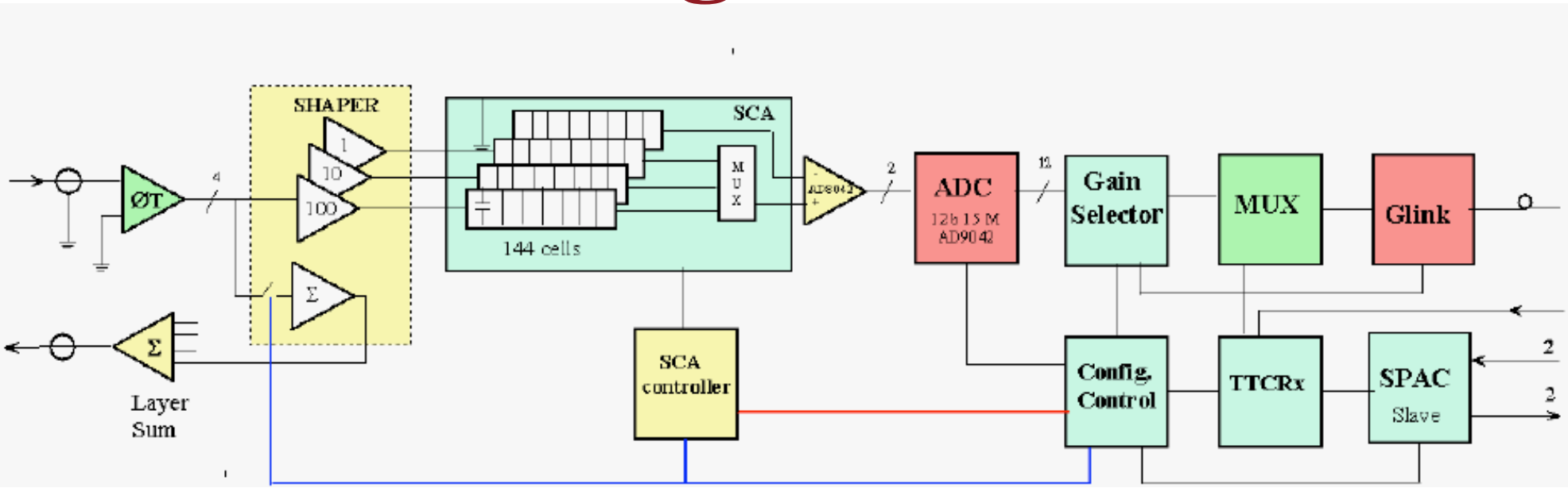
- Initial plan (June 2005)
  - What we have done
  - What we decided not to do, and
  - What we decided to do instead
- Revised plan (~today)
  - Current work
  - Future evolution

Initial Plan

- Focus on architecture for FEB2 first
  - Design for dataflow (FY06) ✓
  - Implementation in COTS components (ADC, FPGAs, transmitter & receiver) (FY06 & FY07) ✓
  - Develop surrounding test infrastructure (DAQ, signal injection, analysis) (FY06 & FY07) ✓
  - Extensive testing of dataflow (FY07) (underway)
  - Radiation testing (FY06 & FY07) X
  - Development of MUX in 0.13 μm CMOS (FY07) X
  - MUX preproduction (FY08?) X

Dataflow Design Considerations



- Rebuild FEB1?
  - Complex, 11 ASICs
  - Analog pipeline implies communication to FEB
  - Single transmitter = single point of failure
  - Single clock for readout, transmitter, etc.

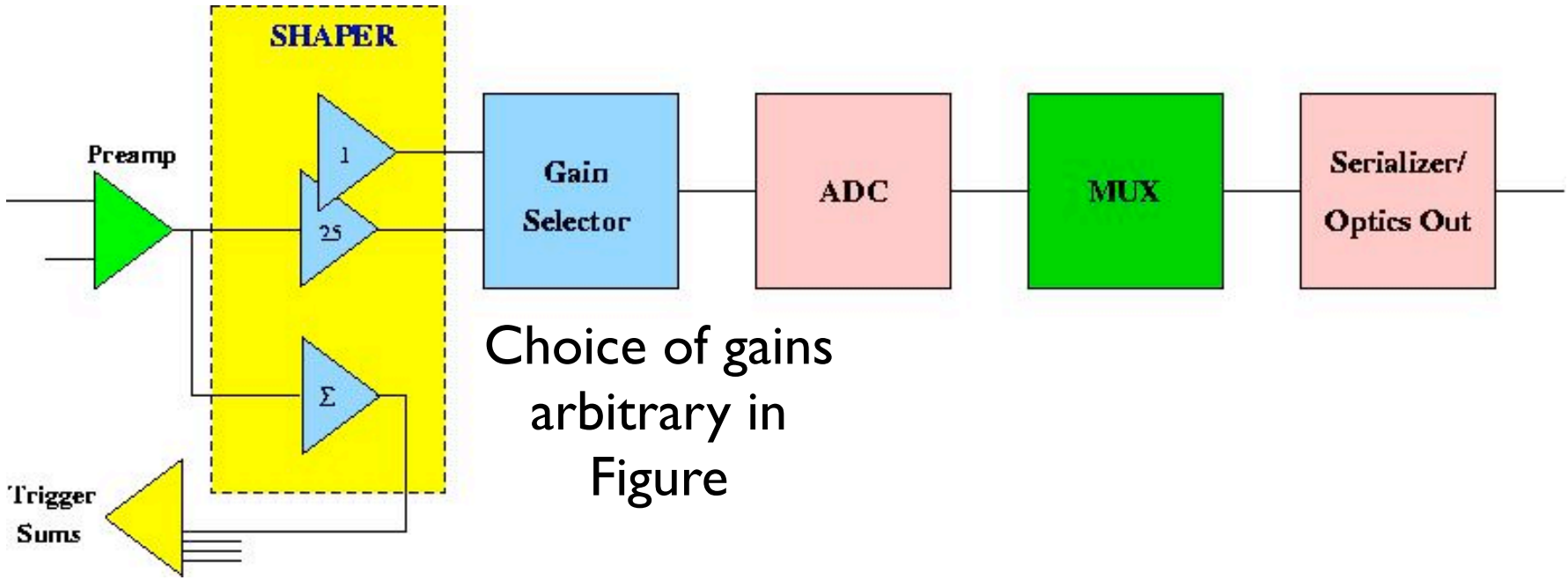
Rebuild?

- Still need to redesign ASICs in current technology
  - Large effort
- Current technologies have lower voltages, more leakage
  - Makes large dynamic range potentially more challenging
- BUT:
  - Significant architectural changes probably means rebuilding RODS as well
- Do we need better L1 trigger selectivity for EM objects? (Probably yes)

Design Considerations

- Digital vs analog pipeline:
  - Analog pipeline difficult given dynamic range (16 bits) and noise requirements
    - Harder with lower voltages and larger leakage currents
  - Digital means digitizing at bunch crossing rate, within ~800 mW/channel total power budget
  - Digital pipeline could be on or off detector
    - On: triply redundant pipeline chip, should be ok (still ASIC)
    - Off: large datavolume to transfer, *but*: no L1 accept down to FEB, potential for decoupled trigger upgrade

"Baseline" FEB2 Architecture



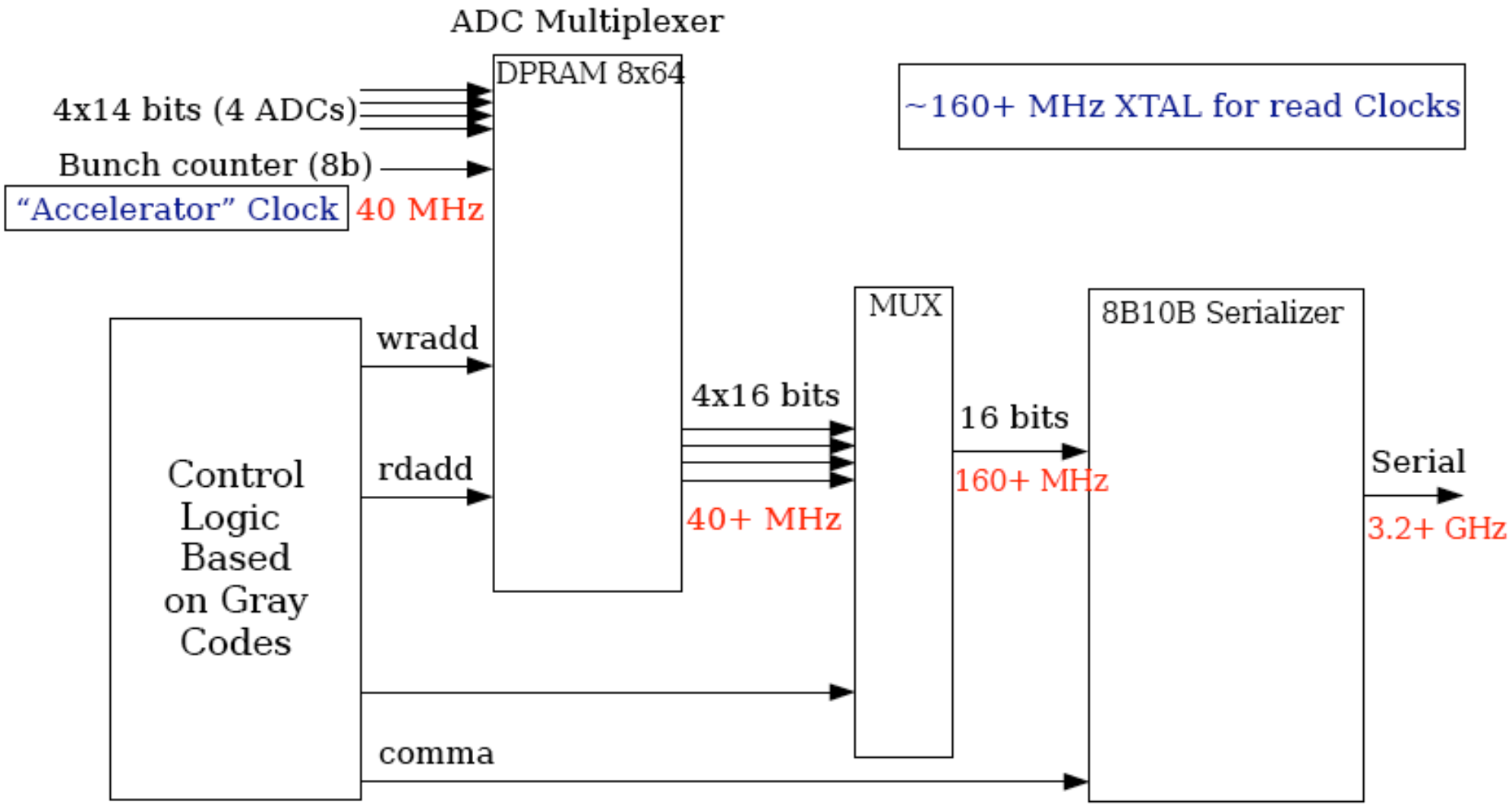
Choice of gains arbitrary in Figure

- Digitize at full bunch crossing rate
- Provide analog sums for decoupled trigger upgrade
- ~100 Gbps without zero suppression
- "Fallback" has digital pipeline on detector

Digital Logic

- Important part of testing infrastructure
  - All data flows through there!
- Good starting point to focus ideas
  - Understand data rate constraints at multiple points
  - “Easy” to implement in FPGA for initial studies
- Where we started

Initial Design

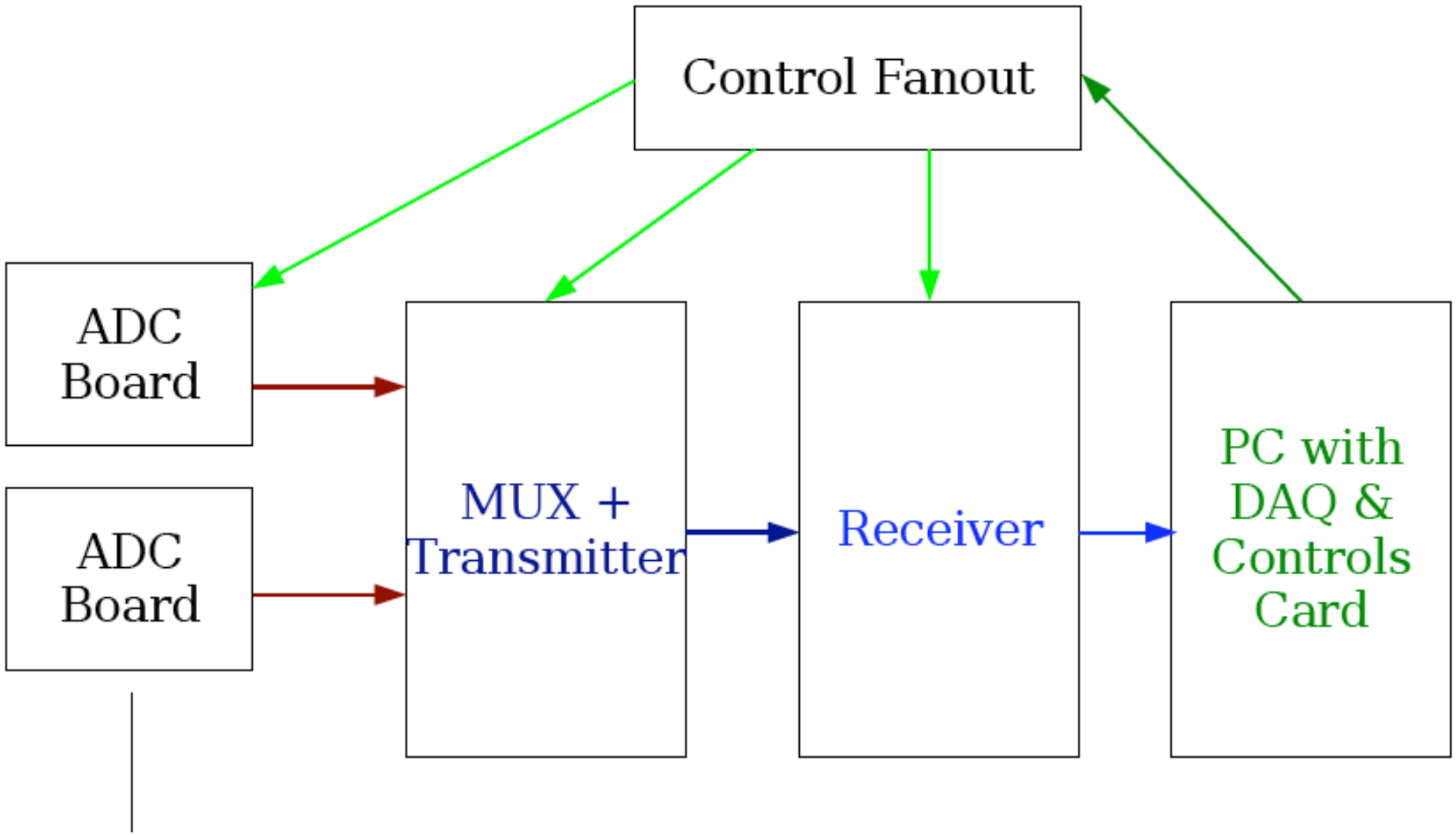


Features

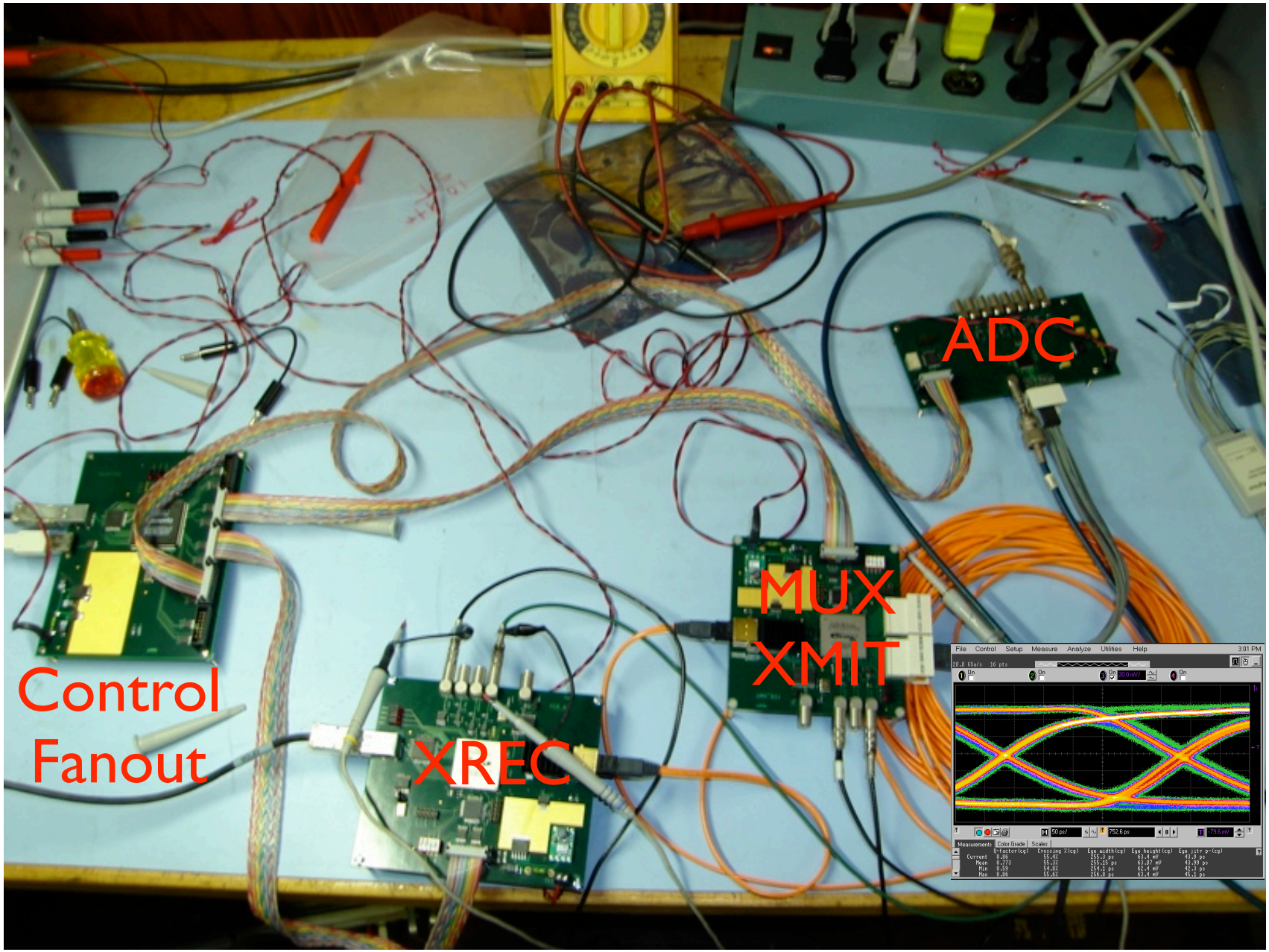
- Two independent clocks
  - ADCs clocked to accelerator, fill “ADC multiplexer” at that rate
    - Clock needs to be brought down to the board
  - MUX, serializer (all high speed components) use clock derived from crystal
    - Much better jitter control
    - Choose frequency to be (4+ε) x accelerator clock, allowing regular insertion of control words
- Gray code to manage multiplexer addresses
  - Minimize effect of upsets

- Data spends very little time in ADC multiplexer (< 8 bunch crossings)
  - minimize upsets
- Triple redundant MUX
- IBM 8B10B encoding at serializer level
  - Standard in many high speed applications, part of libraries
  - Low complexity (5B6B + 3B4B)
  - Sufficient transition density for clock recovery, DC balanced
  - Error detection + control characters
- Also considering a “scrambling” model

Testing Infrastructure

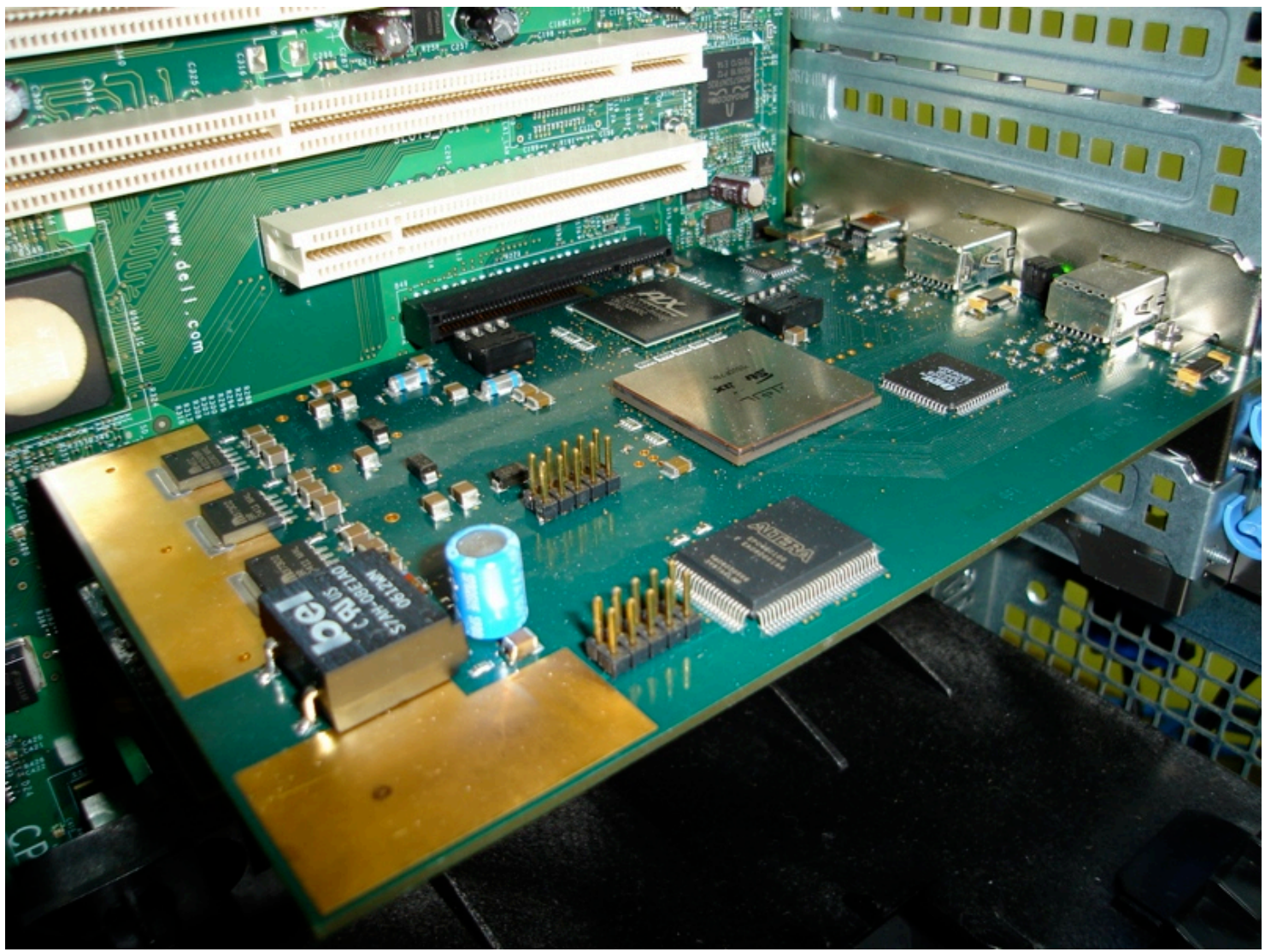


Test Setup



DAQ in PC

- DAQ card using PCI Express



Digital Data Flow/Testbed: Status

- All functionalities implemented in individual testboards using COTS
  - Allows for gradual replacement with prototypes & final components
- Full DAQ chain tested & debugged
  - Results as expected, can “analyze” data (pedestals)
  - User-friendly GUIs to be developed this summer
- Bought waveform generator to inject signal
  - Plan to start working with it over summer as well
- New postdoc will spend 50% FTE on project

MUX -> ADC

- In principle, at this stage planned to start design of MUX in .13 μm technology
- While this is an ASIC and will need corresponding attention, do not believe this presents significant technical or schedule risk
  - Large CERN-based effort means technology rather well understood
  - Our application in principle not particularly complex
- ADC, however, is a very different matter
  - Focus on ADC rather than MUX

ADC

- Issues:
  - Technology: .13 μm SiGe BiCMOS looks promising
    - Join SiGe radiation performance/qualification effort, will contribute proton irradiation studies
    - Got design kit, getting familiar with evolved software tools
  - ADC design
    - Planned to start with analog gain selector as “warm-up exercise”
    - Evolving into integrated gain selector/ADC
      - Pipelined architecture with digital correction logic
      - Initial ~3 stages in parallel, then gain selection is done and rest of stages in common

Radiation Tolerance Testing

- Putting together measurement setup at Nevis
  - Almost identical to UCSC and Penn/BNL setup
    - We have ~all components, putting together now (new postdoc has started) with help from Penn
- Experience with proton irradiation
  - Massachusetts General
    - Can get 10^{15} p/cm^2 in a few hours (equivalent to 2 10^{15} n/cm^2) for samples < 5x5 mm^2
    - Volunteering to irradiate samples when available, then measure - complementary to Ljubljana neutron irradiation
  - Will need to qualify components later as well

ADC Design

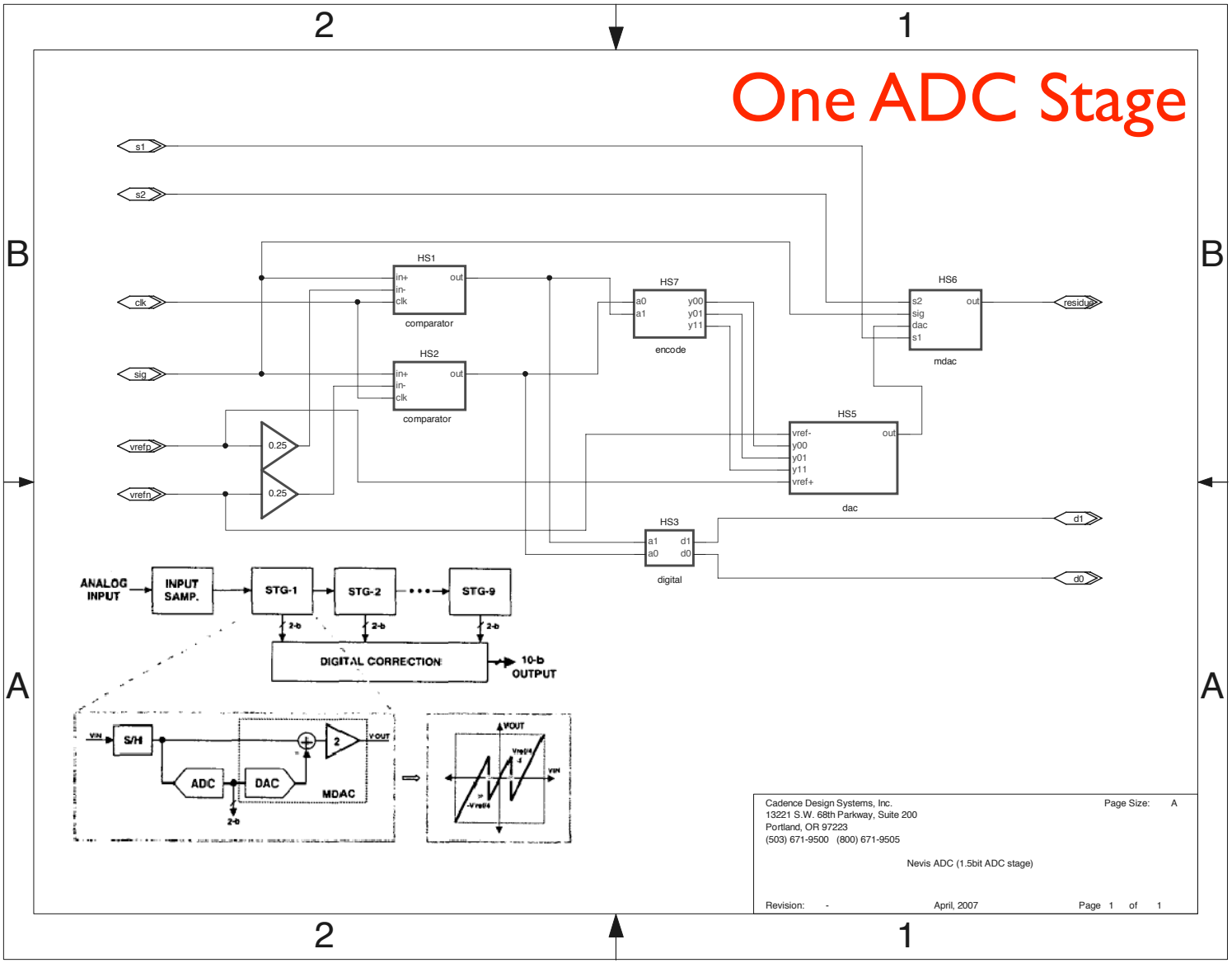
- Pipelined ADC with digital correction
  - Each stage resolves more bits than the subsequent amplification
    - Allows for inaccuracies in comparators, flash ADC
    - DAC/amplifier need to be accurate however
  - Sample & Hold capacitor ultimately limiting factor
    - Noise ~ sqrt(kT/C)
  - From design point of view, amplifier at stage output is critical
    - x2 is likely to be most stable
    - Implies each stage is 1.5 bits

Digital Correction

- Overlap between stages allows correction before outputs are “added”
  - Calibrate amplifiers starting from the back (LSB side) by digitizing known signal, store error terms
  - Apply correction from error terms when “adding”
- Question is where to store/apply error terms
  - On FEB: need a (redundant) “memory”
  - Off detector: almost double necessary bandwidth....
  - Note: commercial ADCs store info in RAM in chip -> rad soft!

Current ADC Work (I)

- "Schematic" in cadence done (10 bit, no gain selection)



Current ADC Work (II)

- Bill Sippach starting with full design of mdac amplifier in IBM 8WL
  - Precision most critical for this "component"
    - Will tell us what is possible
    - Initial experience will tell us something about timescales
  - Currently guessing in ~1 year will want to submit to MOSIS with some of the key structures
    - Amplifier
    - S&H cap

Budget

- E.E.:
  - 50% FTE B. Sippach + 50% FTE L. Zhang
- E.Tech:
  - 50% FTE N. Bishop
- Total personpower: $220k
  - (Physicists: 50% FTE postdoc - T. Gadfort, summer students, + John & me, all paid from other funds)
- Equipment/other costs:
  - Radiation testing $20k
  - Amplifier in IBM 8WL through MOSIS ~$50-100k (?)
  - “Small” items (improvements in test setup) $10k

Past Plan and Achievements

- We had planned to design a dataflow architecture, implement it in COTS and test it
  - We have done that, on the anticipated timescale
- We thought we would then develop the MUX ASIC
  - With our current, better knowledge, we think it is more important to tackle the gain selector/ADC
    - Technologically more challenging
    - Key to the whole digital architecture
  - MUX parameters will potentially depend on ADC
  - So we've started work on the ADC first

Conclusions

- Making steady progress, on timescale predicted two years ago
  - Slight revision of priorities (MUX <-> ADC), to be expected in evolution of an R&D project
- Stepping up physicist involvement by injection of 50% postdoc (started this week)
- Plan to continue steady progress, will need to increase budget in not-too-distant future (MOSIS submission, engineering increase: ASICs + integration)