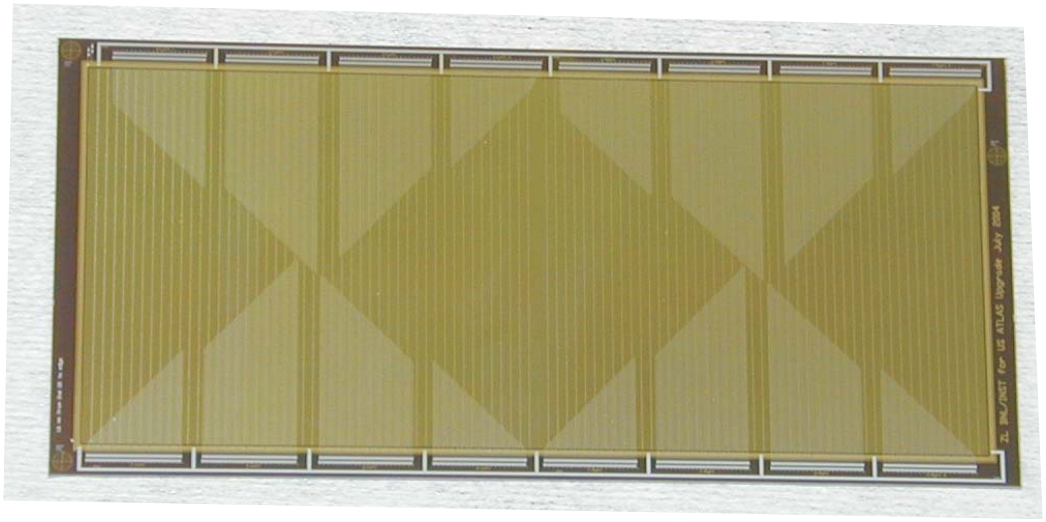
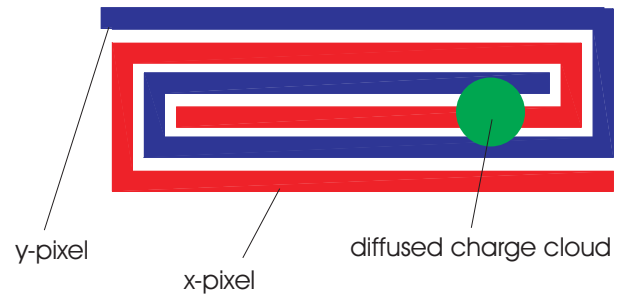
Stripixels and Mini-strips for Inner Staves

D. Lynn, Brookhaven National Lab

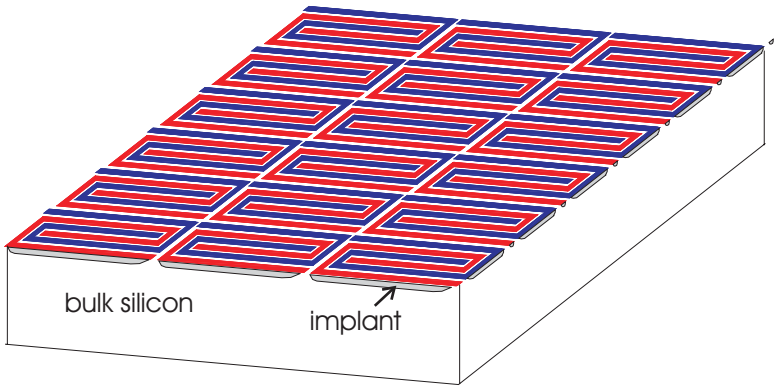


Atlas Tracker Upgrade R&D
Santa Cruz,Nov 10th,2005

Stripixel* Concept– Pixels



- A Pixel is formed by two interleaved (x and y) implants
- Line widths and spaces must be small compared to width of diffused charge cloud to insure signal is split evenly on x and y pixels

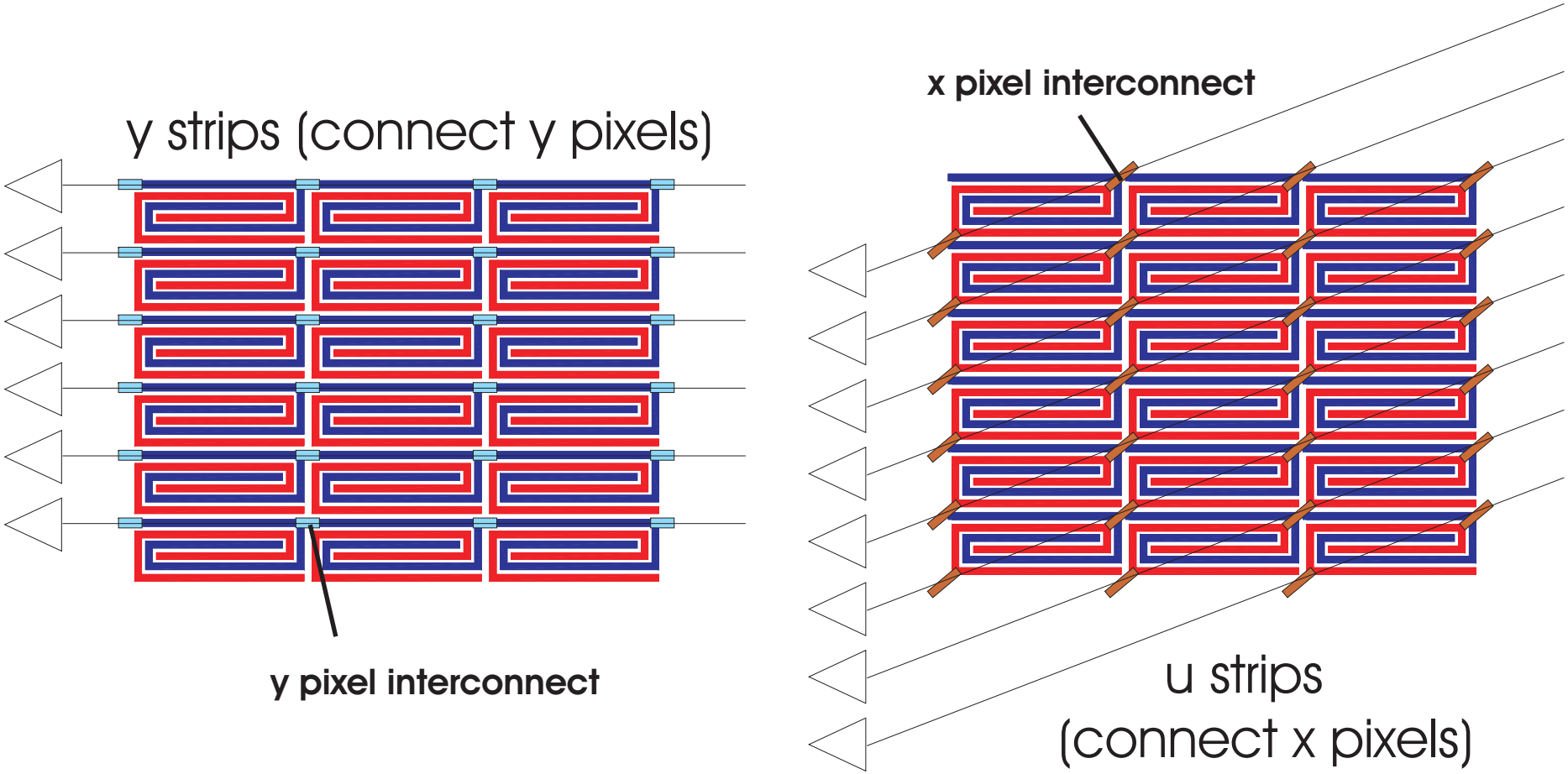


- Detector is a single-sided array of such pixels

Z. Li, Nucl. Instr. Meth A518 V3 (2004) 738

Stripixel Concept– Strips

- **Y-pixels are connected to form Y-strips, and X-pixels are connected to form stereo-angled U-strips**



Stripixels Development Plan

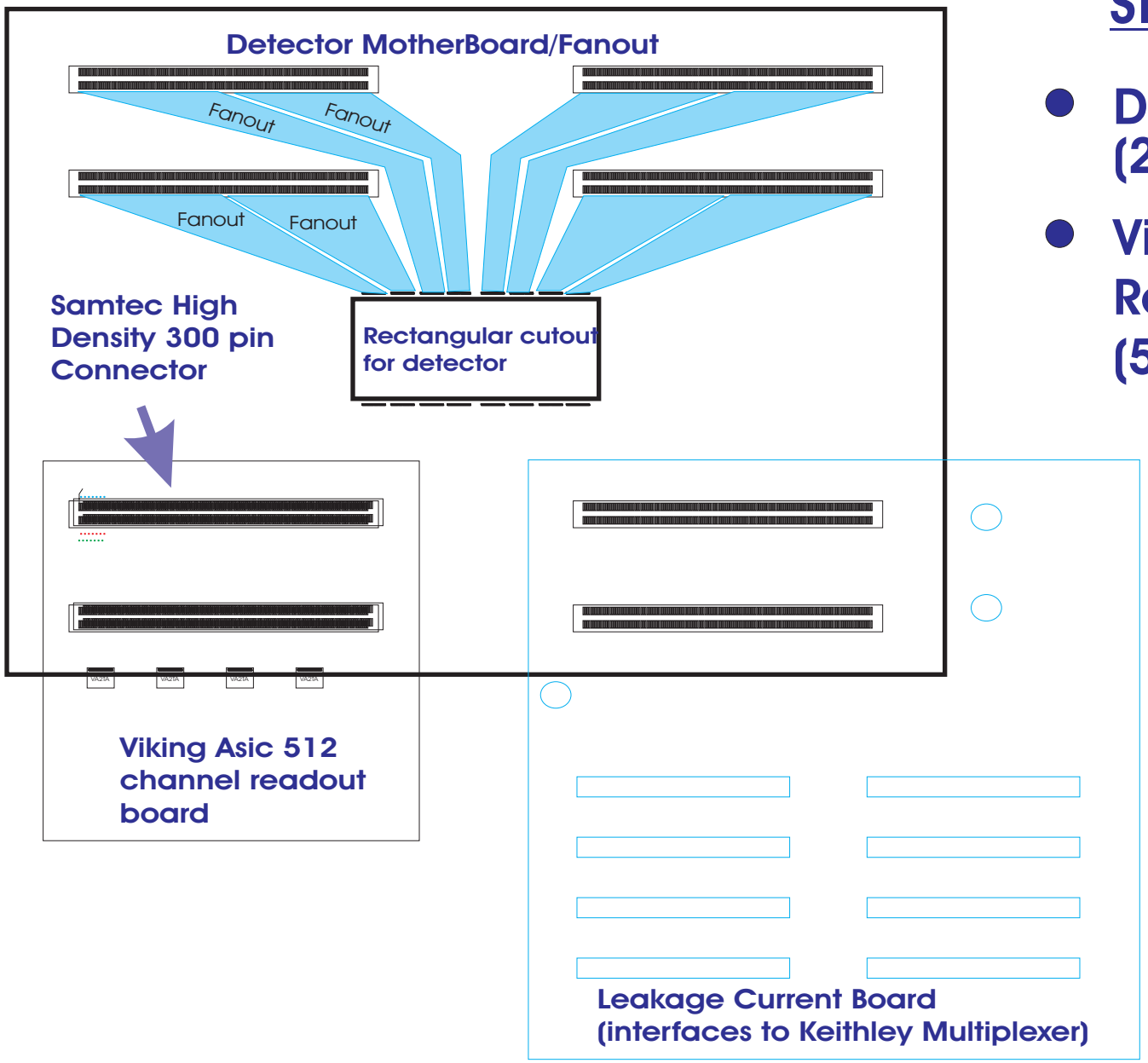
- Initial N-type and P-type stripixels fabricated
- Interleaved pixel used in prototypes
- Purpose
  - Measure/study interpixel capacitance
  - Study x-y charge sharing
  - Compare N-type and P-type properties
  - Measure CCE after irradiation
- Future
  - Explore alternative pixel geometries (uniformity of charge sharing vs capacitance tradeoff). Need to develop better simulation capability.
  - Introduce AC coupling??

Detector Characterization Approach

- Develop test system that permits:
  - Automated strip current measurement for all strips
  - Low noise readout of all strips for charge sharing studies
  - Capacitance measurement of large sample of strips (but not all)
  - Irradiation of powered detectors (but not electronics)
  - System that can be used for altnernative stripixel detectors or for strip detectors
- Therefore decided to build system that utizilizes
  - Motherboard designed for each detector variant
  - Plug in boards common to all detector variants

    1. Viking readout board (512 channels)
    2. 256 channel leakage current board
    3. 40 channel capacitance measuring board

Stripixel Testing Method



Stripixel TestBoards

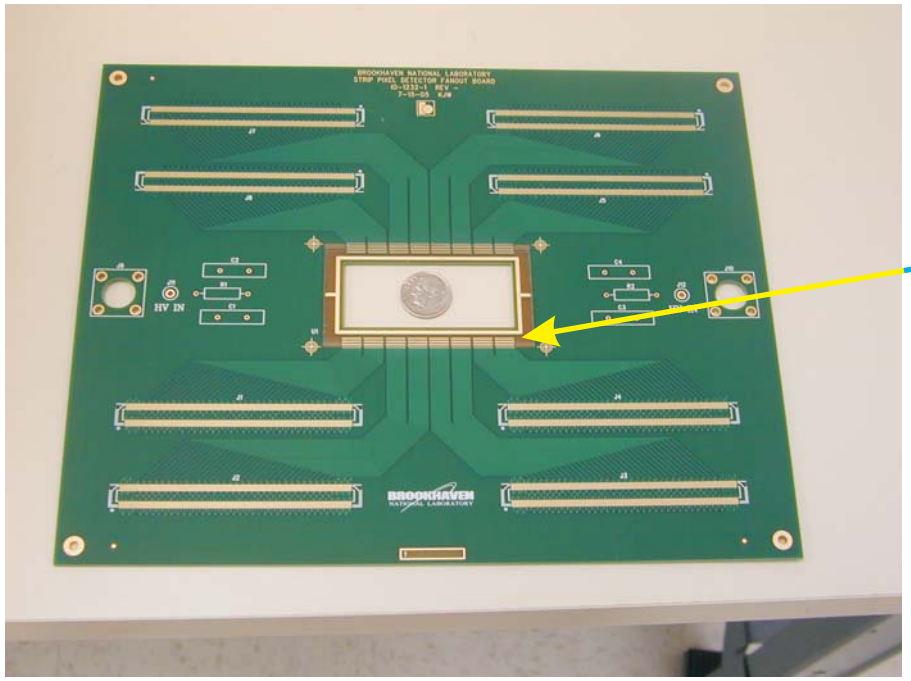
- Detector Motherboard (2048 channels)
- Viking (IDEAS, Norway) Readout Test board (512 channels=1/4 det)
- Detector Leakage Current Board (monitor 256 channels simultaneously)
- Capacitance Meas. Board (not shown)

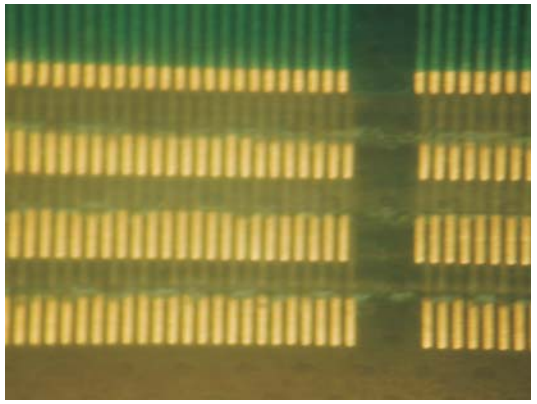
Stripixels Progress to Date-I

- Initial motherboards fabricated at BNL (qty=2)
- Leakage current boards fabricated at INFN-Milano
- Capacitor boards fabricated at BNL
- Viking board layout underway (INFN-Milano)
- Labview based measurement station for automated leakage current testing developed at BNL (INFO-Milano student Giovanni Ganzer)
- Intend to have two complete duplicate stations at BNL and INFN-Milano

Stripixels Progress to Date-II

- First two motherboards were finished last week at BNL (started in July)





Challenge — Achieve effective 2 mil wirebonding pitch with four staggered layers using 4 mil lines/space

- Checking with outside vendors in US and Italy to see if we can get faster turnaround .

Stripixels Progress to Date-III

Viking board

- Evaluation of VA1' and VA2TA concluded in July. Self triggering VA2TA chose and 100 chips purchased.
- Circuit diagram finished in August
- Layout underway at INFN-Milano. Board will need 1 mil lines/spaces for bonding to chips (similar to motherboard).
- Evaluation of VA2TA revealed ability to sink only very limited amount of leakage current. Therefore require AC coupling via RC circuits for each channel.
- Hoped to get custom RC circuits from Ohio State via SCIPP, but now am proceeding with surface mount (a complicated layout results).

Stripixels Progress to Date-IV

Summary

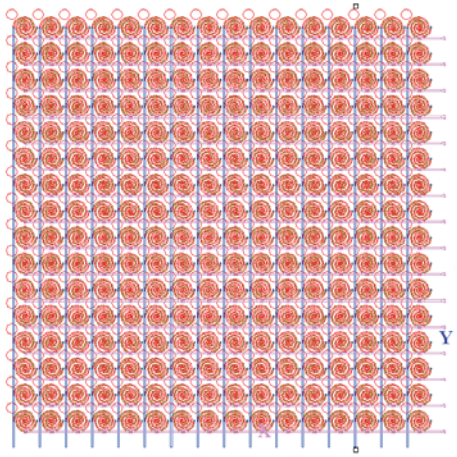
- Expect Leakage and Capactive measurements in about 3-6 weeks

- Expect initial charge sharing measurement early next year (with Viking boards and the use of a radioactive source–laser injection to be built later)

--> Full detector characterization capability almost online

Stripixel Capacitance

- Should have direct capacitance measurements in Dec.
- For the moment have the following:
  - Simulation by Gianluigi de Geronimo (BNL) using Ansoft Maxwell 2D programs gives about 6pF/cm = 18 pF/det
  - Measurements on mini-spiral 80 um pitch stripixel (Interstrip capacitance on Prototype Stripixel Detector, John Gerling and Aleksandr Polyakov, SCIPP, Sept 2005) gives 8.2 pF/cm = 24.6 pF/det
  - Phoenix stripixel most similar to ours except 80 um pitch rather than 50 um gives 5pF/cm = 15 pF.
  - For S/N estimates will assume ~ 18 pF/det

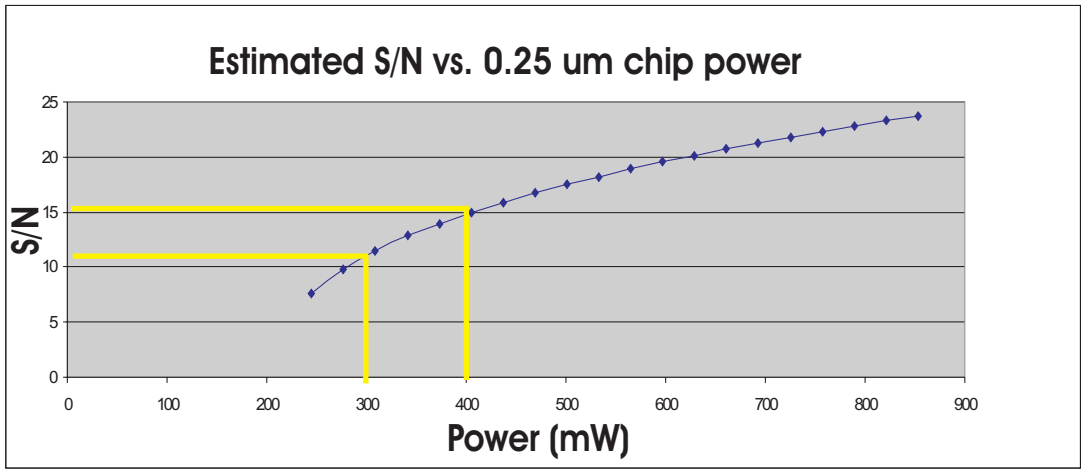


Stripixel S/N Estimates

- Use Paul O'Connor's (BNL) calculation of series (including 1/f) noise vs input power (at 18pF):
- Non input transistor power of .25 um APV 25 is about 240 mW, and that of ABCD (scaled down to 2.5 V supply) is about 215 mW.

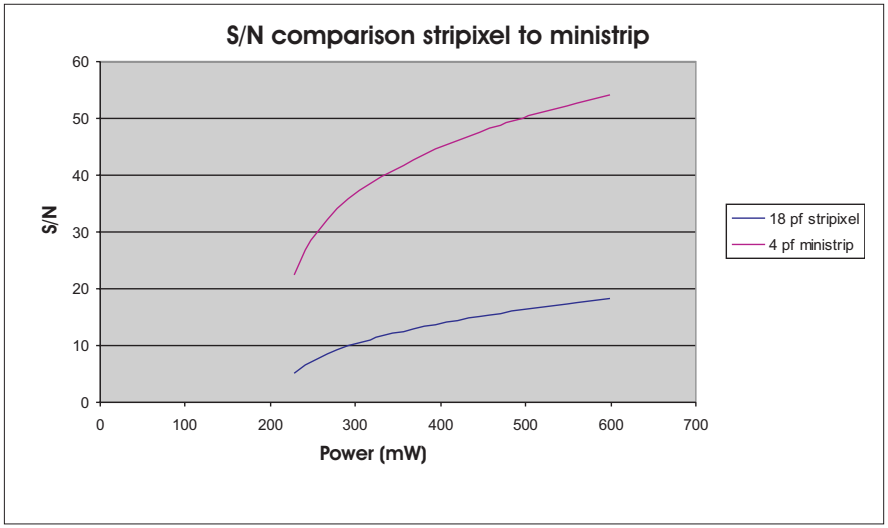
			Series noise (ENC)		
Feature size (um)	Supply Voltage	Power (mW) (preamp only)	18pF	36pF	54pF
0.18	1.8	0.1	2100	4100	6200
		1	780	1460	2118
		10	360	624	870
0.25	2.5	0.1	2480	4840	7170
		1	920	1730	2510
		10	430	740	1030

- Use chip power = 215 mW + input transistor power to generate an estimated S/N as a function of total chip power
- Get S/N 10-15 for power ranges similar to current ABCD (400 mW) and APV 25 (300 mW)



Stripixel to Ministrip S/N Comparison

- Using same calculation can generate S/N plot for presumed minstrip detector (3cm strips, ~ 4pF capacitance)



- Clear that in ministrip case S/N never a problem, and power should be dominated by the non-input transistor part of chip

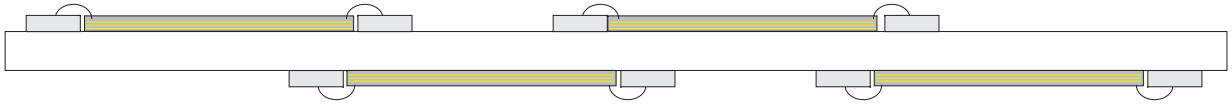
- Stripixel a candidate only if:
  1. We can signifcantly reduce capacitance
  2. *OR* 2d coordinate info essential and tiled 2d stave approach very difficult (see next slide)

Inner Radii Staves

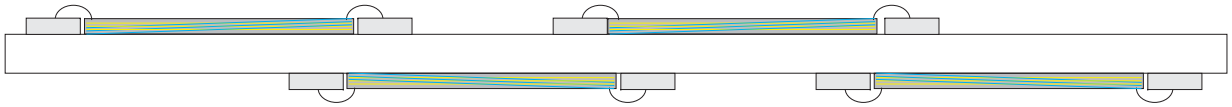
- Presumed strip lengths 3-3.5 cm
- Possible Variants *(x Super Module?)*

Increasing Complexity

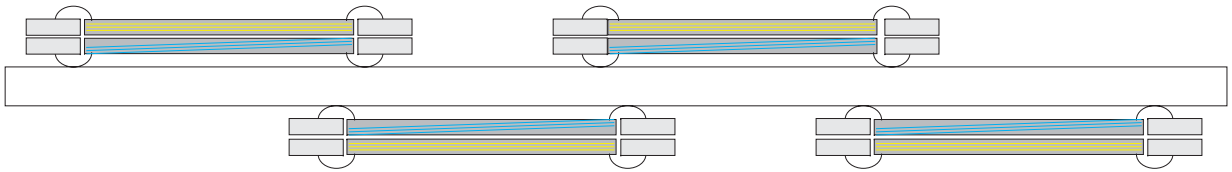
- Tiled 1-d Ministrips — *One coordinate info*



- Tiled 2d Detectors (stripixel or other) — *Two coordinate info*

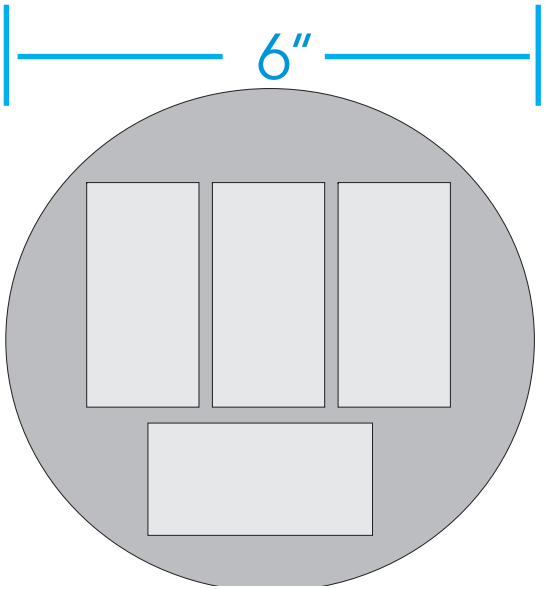


- Tiled back-back? dual 1-d Ministrips — Two coordinate info



Mini-strips for 1-d Tiled Staves

- Specifications (basically short versions of current sct dets)
  - Material — N-type (for ABCD readout), Float Zone
  - Orientation — <100>
  - Size — 6.6 cm x 3.4 cm, approx.
  - Thickness — 300 um.
  - Pitch — 80 um
  - Number of strips — 6 x 128+2=770
  - Coupling — AC
  - Bias Resistor — 1.25 +/- 0.75MΩ
  - Full Depl. Volt. — < 150V
  - Breakdown Volt — > 500 V (800 V preferred)
  - Fiducials — CDF style for alignment on stave



- Design to be done at BNL
- Quantity. Minimum for 1 meter stave
  ~ 33. Plan fabricate 20 wafers = 80 dets
- Sintef interested in making. Waiting for quote. They have 6" capability (necessary to keep down cost)
- Will fab several wafers at BNL to test our new 6" capability

Summary

- Full detector characterization capability to be soon ready at BNL and INFN-Milano

- – Will characterize first generation stripixel
  - – Will shortly thereafter begin irradiation studies
  - – Meanwhile will explore possibility for capacitance reduction (plan to develop simulation to guide effort)
  - – (will also submit alternative geometry in an upcoming RD50 submission)

- Plan to produce mini-strips for a 1-d tiled stave

Other inner stave activities at BNL

- Study serial power architectural questions (collaborate with RAL, LBNL)

- Develop new DAQ that permits parallel readout of inner 1d stave (33 hybrids) for noise studies

- Design ABCD board for stripixel readout

  Board to have capability to be powered with plug-in DC-DC converter. Want to look at noise at higher frequency switching (>1MHz)

- Looking into possibility for air-core buck converter DC-DC converter