U.S. ATLAS Upgrade R&D Proposals for FY2007

Collected below are the status reports and budget requests for the projects proposed for the Upgrade Program for FY07. The overall plan follows the WBS structure and projects developed over the past two years. An additional project proposed is in the area of System Design by BNL. In addition the work under WBS 4.5, set to terminate in FY06, is requested to continue at the level of $25k (this is for radiation measurements in the muon area). The program has several new institutions: NYU in the area of staves and short strips, U. Penn. in the area of Si-Ge frontend electronics for Liquid Argon. We also anticipate that Yale may want to participate in the area of staves. The detailed breakdown of requests, by institution, follows this section.

The budget requested for WBS 4.1 is about $2M. For WBS 4.1 this compares to the budget guidance of $1.593M. The management reserve number presented last year is $0.356M. The sum of the two would provide an adequate budget for WBS 4.1 in FY07. The item in the reserve was the development of a Pixel Chip in 0.13 micron technology by LBNL. This has already been delayed by a year. LBNL has hired an experienced analog designer (Abder Kekkaoui, who previously worked on the FPIX chip at Fermilab) and has worked out a good plan for the chip development. CERN is completing a frame contract for this technology, which will make it more cost effective than by using MOSIS. This is a high priority item and we request that the funds be moved out of management reserve and included in the base budget.

The budget requested for WBS 4.3 is about $1.2M. The budget guidance for WBS 4.3 is about $514k, only about two-thirds of last year's number. The management reserve number we had last year was $539k. The sum of the two numbers would allow a good fraction of the work to proceed. We again request that we be allowed to allocate the funds presently in management reserve. The reserve was spread across the whole WBS plan.

We have made significant progress on management and integration of the U.S. program into an international ATLAS framework. For WBS 4.1 and WBS 4.5 most of the areas are now part of ATLAS R&D plans with written plans scrutinized by an ATLAS steering group. The plans are also reviewed by two ATLAS referees, with a number of such reviews in progress and a number completed. We anticipate all parts of WBS 4.1 and 4.5 going through this process in 2006, except for one project. This is the 2-D detector work at BNL where the FY07 work will mainly involve finishing the plan from last. This is a unique project and we will decide in about a year whether we feel it fits into the proposed upgraded detector. This depends partly on whether it is decided to have two-dimensional information from the short-strip region and what the final value for the strip capacitance turns out to be given steps to minimize the value.

For the WBS 4.3 program I am planning to require that they provide a plan for scrutiny to the ATLAS steering group before the end of 2006. This effort is about a year and a half behind the tracker work and funding for it started significantly later. Working out the international framework will take some additional time.

In addition a Project Office for the Upgrade has been established under TC with David Lissauer serving as head. An Upgrade meeting is scheduled for CERN on Oct. 1 and 2 and a dedicated tracker meeting is scheduled for Liverpool on Dec. 6 – 8.

FUNDING REQUESTS

WBS 4.1		
Institution	Projects	Request Total
BNL	Stave, stripixel, power conversion, system studies	$347,000
NYU	Short Strips	$35,000
LBL	Staves, thermal design, power conversion, CMOS	$672,700
Hampton	Staves	$20,000
UCSC	n-on-p detectors, Si-Ge electronics, optoreadout	$316,000
Hawaii	3-D pixels	$184,500
New Mexico	3-D pixels	$85,000
Ohio State	Optical readout	$189,500
Oklahoma State	Optical readout	$53,000
Oklahoma	Optical readout	$38,900
SMU	Optical readout	$83,100
Total		$2,024,700
WBS 4.3		
Institution	Projects	
Arizona	Layer Buildup on Electrodes	$113,500
BNL	System Arch., Si-Ge Front.	$470,100
Nevis Lab	Digital Readout System	$332,000
Penn.	Si-Ge frontend electronics	$60,000
SMU	Novel Optical Readout	$234,300
SUNYSB	Frontend electronics	$25,000
Total		$1,234,900
WBS 4.5		
Institution	Projects	
Arizona	Muon system radiation levels	$17,500
GRAND TOTAL		$3,277,100

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WBS 4.1.1.1

Development and Testing of 3D Active-Edge Silicon Radiation Sensors with Extreme Radiation Hardness: Progress Report and Proposal

19 June 2006

S. Parker, [1] C. Kenney, [2] J. Hasi [3], C. Da Via[3], M. Hoeferkamp[4], S. Seidel[4], and I. Gorelov[4]

1. University of Hawaii, 2. Molecular Biology Consortium, 3. Brunel University, 4. University of New Mexico (see separate report)

Introduction and Review

We are fabricating 3D sensors with N and P electrodes perpendicular to, rather than in, the plane of the surfaces, as shown in Figure 1 [1 – 11]. This allows a small electrode pitch while still having short collection times, relatively low depletion voltages, and sensitivity to within a few microns of the physical edges. Details on earlier results, in particular, low depletion voltages, radiation resistance up to the low 10^{15} 1 MeV equivalent neutrons / sq. cm, and fast pulses, even from radiation damaged sensors, are given in the fy06 report.

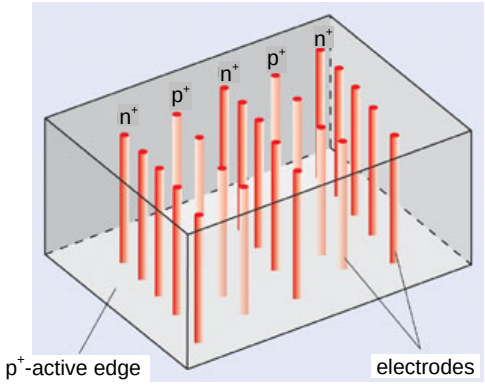

Figure 1. Sketch of a 3D detector. The p^+ and n^+ electrodes are processed inside the silicon bulk, which for ATLAS will be p^{--}. The edges are made from trench electrodes (active edges) that surround the sides of the 3D device, making an active volume sensitive to within a few microns of the physical edge.

The budget request for last year's proposal stated:

"For the coming year, we will assume, as is normally the case for other members of the group, that salary, benefits and overhead are fully covered by the Hawaii base grant. To be reasonably sure we finish on time and produce sensors that perform adequately, it

would be best to have two fabrication runs, allowing 2-3 months of testing between each run."

The amount in the fabrication budget table in that report, with a cost per run of $62,340, would have been covered by the amount available from ATLAS Upgrade funds ($129,000), had we not spent any funds on general-purpose and DAQ computer equipment, and only limited funds for LBL to Stanford trips, and possible trips to CERN and ATLAS Upgrade meetings. (We planned to use the anticipated FY 2006 ADR funds ($22K) for some of these items.)

Rather than covering even salaries, the actual Hawaii budget was cut again to $45,000, requiring all of the ATLAS funds and some of the ADR funds to be used for salaries. FP420 funds provided by Cinzia Da Via from the UK paid for one fabrication run, which has just been completed. No funds were spent for equipment. (The R&D project, FP420, is developing a proposal for forward detectors at 420 m from the ATLAS and/or CMS interaction points. They plan to use the same 3D sensors and readout electronics being considered for the ATLAS B-layer replacement.)

Beyond completion of the 3D fabrication runs, the planned tasks were:

1. Improve the yield of good devices,

2. Continue measurements on already completed devices for radiation hardness, speed, and most important, compatibility with ATLAS front-end readout electronics (particularly to check that the source capacitance was low enough).

All of this has been done.

3. A parallel testing program will take place in New Mexico, using laser and high-speed equipment unavailable here.

In addition, several programs, initiated by Cinzia Da Via and Steve Watts of Brunel University, have produced the following results:

4. Developed a second source for 3D and active edge sensors: SINTEF, which is a Norwegian commercial company that has, for many years, manufactured and sold silicon sensors, and is at the same time, a research institute supported by the Norwegian government. SINTEF shares a building in Oslo with a research group of the University of Oslo. We have formed a collaboration, visited their headquarters and clean rooms several times, and they have recently attended a 3D meeting at Brunel. They are now starting to develop their fabrication technology, which may differ somewhat from ours due to differences in fabrication equipment. Their first planned sensors will be the 3D – active edge / planar – central TOTEM sensors, which should be somewhat easier to fabricate. They plan to use their own funds to make the initial group.

5. Extended the collaboration to include the ATLAS group from the Czech Technical University of Stanislav Pospisil, Vladimir Linhart, Tomas Slavicek, and T. Horadzov. They have provided reactor irradiations that have allowed us to reach the 10^{16} per sq. cm. range and are developing measurement facilities. Early next year, they will acquire a small, tight-focus, specialized ion accelerator that will allow us to rapidly irradiate and test oxide damage in the presence of the stray electric fields in sensors under bias – a

possibly important item not tested by neutron irradiations. Working with C. Da Via, they are also developing equipment for testing irradiated sensors.

6. Started a new R&D project, FP420, mentioned above, that may extend the capabilities of ATLAS and / or CMS. Both the active-edges and high radiation hardness of 3D will be critical for FP420.

Fabrication Yield

The major changes to improve yield were to:

A. add process-checking steps,

B. add time,

C. if necessary (and if possible) undo and repeat a step with unsatisfactory results, and

D. in parallel, start more wafers than needed, and hold back some of them part-way through the process.

A. Examples of process-checking steps used in the current run are these from the first 20 (of 106) steps of the run sheet:

2) CLEAN at WBNONMETAL - YIELD FACTOR: Change chemicals/ Do at least two spins on the spin dryer

3) CLEAN at WBDIFF - YIELD FACTOR: Change chemicals/ Do at least two spins on the spin dryer

5) FIELD IMPLANT BOTH THE FRONT AND BACK SURFACES OF THE WAFERS - YIELD FACTOR : When picking up the double-sided device wafers, only pick up from the laser edged area of the wafer and Use clean tweezers

6) CLEAN at WBNONMETAL - YIELD FACTOR: Change chemicals / Do at least two spins on the spin dryer

7) CLEAN at WBD - YIELD FACTOR: Change chemicals / Do at least two spins on the spin dryer

8) GROWN THERMAL OXIDE USING TYLAN1-4 - YIELD FACTOR: Load with delrin tweezers and let wafers cool down before unloading the wafers from the furnace with the delrin tweezers.

9) PREPARE SURFACES FOR FUSION BONDING AT WBDIFF - YIELD FACTOR: Change chemicals, definitely for the HCL step prior to fusion bonding the wafers. Do at least two spins on the spin dryer.

10) FUSION BOND – YIELD FACTOR: Wear face shield to reduce particle generation. Perform after hours or on weekend when there aren't many people around.

11) FUSION ANNEAL AT TYLAN1-4 – YIELD FACTOR: Careful when placing the wider wafers into the furnace boats.
12) CLEAN AT WBNONMETAL - YIELD FACTOR: Change chemicals/ Do at least two spins on the spin dryer

13) CLEAN at WBDIFF - YIELD FACTOR: Change chemicals/ Do at least two spins on the spin dryer

14) DEPOSIT NITRIDE ONTO THE WAFERS TYLANNITRIDE (TYLAN #10) - YIELD FACTOR: Load with delrin tweezers and let wafers cool down before unloading the wafers from the furnace with the delrin tweezers.

15) CLEAN AT WBNONMETAL - YIELD FACTOR: Change chemicals/ Do at least two spins on the spin dryer

17) COAT WITH RESIST AT SVGCOAT - YIELD FACTOR: Purge and Clean the nozzle of the resist tube with acetone and a swab, removing all the clogged up resist around the entrance of the plastic tubing.

18) N ELECTRODE OXIDE ETCH CONTACT LITHOGRAPHY - YIELD FACTOR: Practice various exposures on a few dummies before attempting on the real device wafers. Observe the exposures through the optical microscopes. Blow-dry every wafers before exposing. Clean the mask before every exposure with acetone, methonal and isopropyl.

19) DEVELOP RESIST USING SVGDEV - YIELD FACTOR: Observe that the wafers get coated with LDDW-26W (developer) during the program. If not, use the air gun to allow the liquid to flow over the uncovered areas of the wafer.

B. All these specific steps take extra time, of course, but in a work flow in which many of the individual tasks are automated, while the over-all process is not, adequate time helps reduce errors in important non-specific ways as well.

C. The undo and repeat, under ideal circumstances, is more a learning tool to understand sources of trouble for the redesign of the process flow. Under the present circumstances, however, it was also a rescue mechanism.

An example of A. combined with C. (process-checking plus undo and repeat) came at the end of the fabrication run, where the 8,640 diodes of the 3-electrodes per pixel ATLAS sensor were checked by deposition of a layer of temporary metal. The number of sub-divisions was set so all diodes could be checked with a reasonable number of probe points while preserving diagnostic capabilities. Figure 2 shows part of an ATLAS 3-electrode per pixel sensor with temporary metal on the left and with permanent metal on the right.

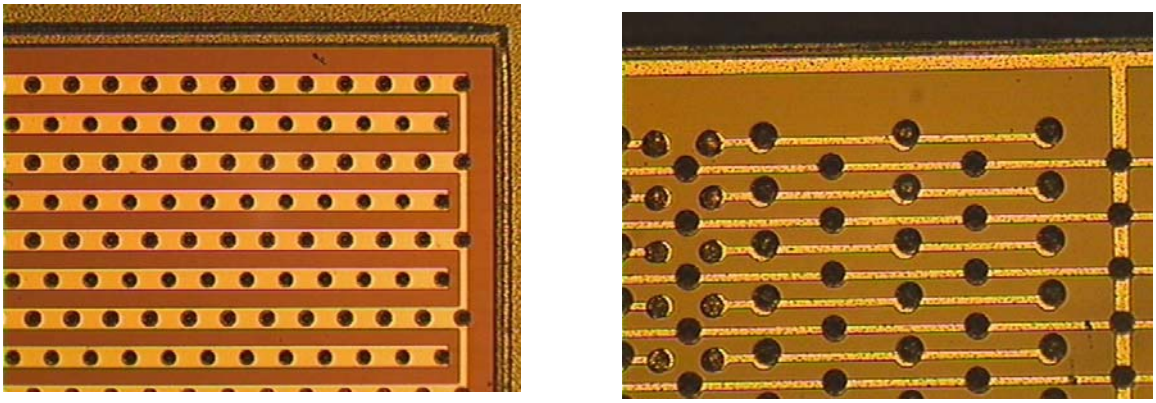

Fig. 2 ATLAS 3-electrode per pixel sensors with temporary (left) and permanent (right) metal. Temporary metal connects 320 pixels to one contact point. The top strip connects n electrodes, the next p electrodes, etc. (P electrodes are connected along the left edge.) Bump pads can be seen on the left side of the permanent metal. New permanent metal uses wider strips and a ring around the electrode depressions.

Ten wafers were started (each with 20 3-electrode, 5 4-electrode, and 5 2-electrode full-size and 22 quarter size ATLAS sensors) and carried to the step before temporary metal, which was put on three wafers. The substrate is p type, 200 μm thick, 12.5 KΩ material. Testing showed two had significant regions of open contacts between the electrodes and the metal, a condition that was seen in the previous run. It is correlated with a residual, hazy film and is likely due to incomplete removal of an oxide and nitride capping layer, used in earlier steps, to keep dopant atoms from spreading during subsequent high-temperature steps. These wafers are being held back for further investigation. (One good wafer should have enough devices for all of this year's planned beam tests.)

The third tested satisfactorily, except the edge strips had high leakage currents. They went back to normal when the next regular step, a forming gas anneal, was done. Permanent metal was deposited, patterned, and spot-checked by probing many electrodes directly, rather than risk damage to the bump-bonding pads. A protective layer of low-temperature oxide was deposited and patterned with openings just for the bump-bonding pads. However, a final check now showed many open circuit conditions!

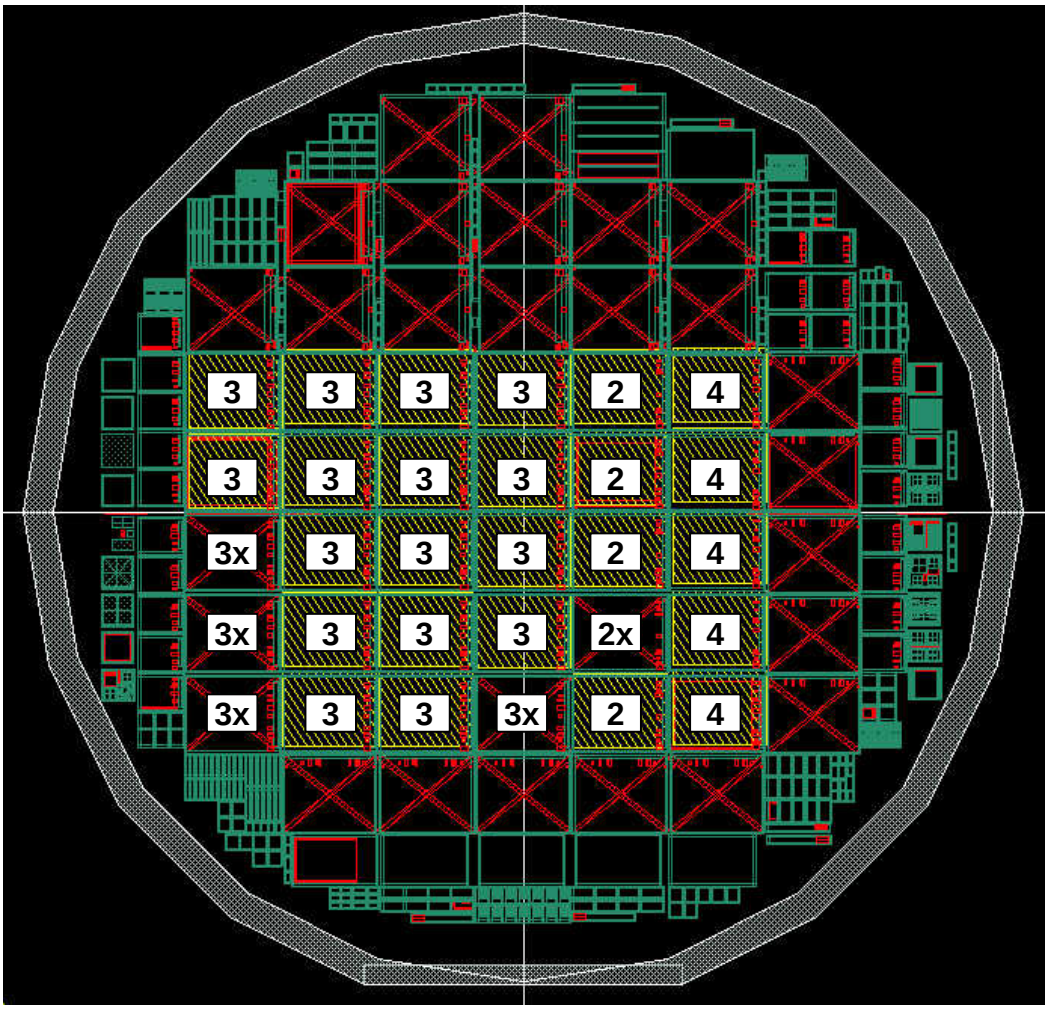

Figure 3. Diagram of the wafer sent to IZM for solder-bump bonding. Chips for ATLAS are in the central 5 x 6 array and show the number of electrodes per pixel.

Twenty five of the thirty are recommended for bump bonding. The number of electrodes per pixel is indicated. The 25 wafers recommended for bonding do not have an "x" after the number.

Given the dips along the edges of the electrodes, and the narrower metal lines, evident in Figure 2, a likely cause was breaks in the deposition at those dips. A new mask was made for permanent metal, featuring wider lines and a larger metal circle over the electrodes. The metal and protective glass were removed and a new, thicker metal layer was deposited and patterned with the new mask. Spot checks indicate this probably solved the problem. A new layer of glass has been finished, more spot checks have been completed, and the wafer has been shipped to IZM for bump bonding.

A diagram of the wafer is shown in Figure 3. Unmarked chips are either test devices or are for other projects such as FP420 which plans to use ATLAS units, half of them oriented at right angles (with a modified bias contact location) to provide 50 μm x 50 μm resolution units.

Diagnostic tests have also started on the open-contact condition. Wafers that had been completed and had metal removed, were put in a scanning electron microscope. Fluorescent X-rays were recorded. Figure 4 shows a typical scan of an electrode in the region where poor contacts were common. Only slight amounts of oxygen and no nitrogen were seen, corresponding to an upper limit of 20 nm of SiO_2 now present. Yet enough voltage was applied to the poor contacts to break down that amount of material. This will remain a topic for investigation, including the question of how much underlying SiO_2 is removed when a layer of aluminum is deposited and etched off.

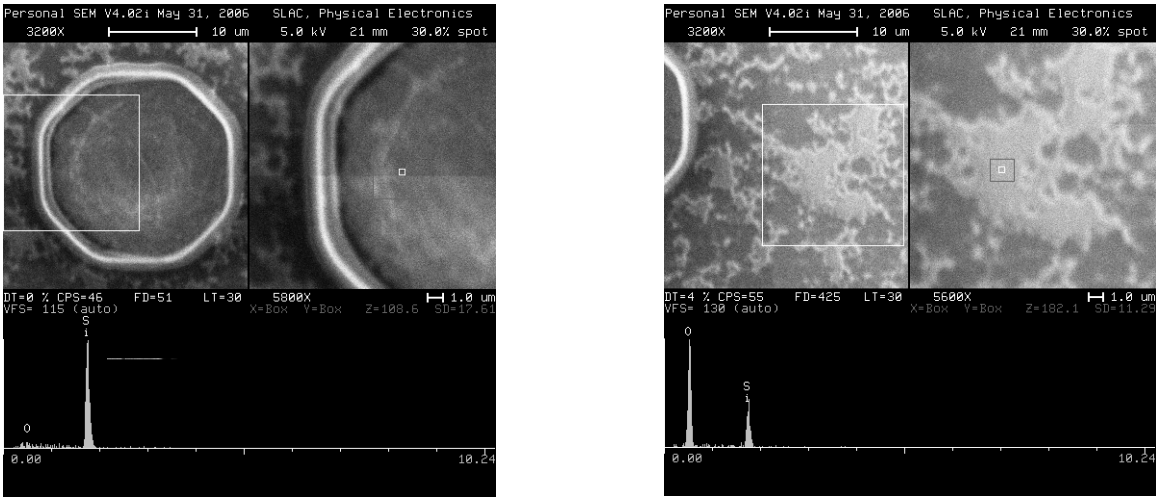

Fig. 4. (left) Image and spectrum from an n+ electrode using 5 keV electrons. The sampled area is indicated by the small square inside the right-hand, magnified part of the image. (right) Sampled area in the field oxide. The lower plots shows the X-ray intensity spectra, with the higher energy silicon line on the right. In the right spectrum, with the beam incident on the field oxide in a region used for control, the oxygen peak can be seen on the left.

D. In addition to the two wafers that will be investigated for contact problems, the remaining seven can be finished in a reasonably short time, and will be available for additional tests.

Measurements

We were again limited this year, to measurements of sensors that had been fabricated in the original fabrication run and ATLAS pattern sensors made during a 5-week run (2 – 3 months is normal). Both were completed before the start of ATLAS Upgrade Funding and before the development of yield-enhancement steps.

A. Performance of sensors bonded to ATLAS front end readout chips.

From last year's report:

"The initial batch of ATLAS sensors, made in the low-yield 5-week run, had the standard n-type signal electrodes, p-type bias electrodes all tied together, and n-type bulk. They were tested with no prior irradiation, so a single leakage point at the diode junction could disable the entire detector. We plan to irradiate them to invert the bulk, placing separate diode junctions at each electrode, to see if the bias voltage can be raised from 1.5 V to the full depletion voltage (≈ 5V)."

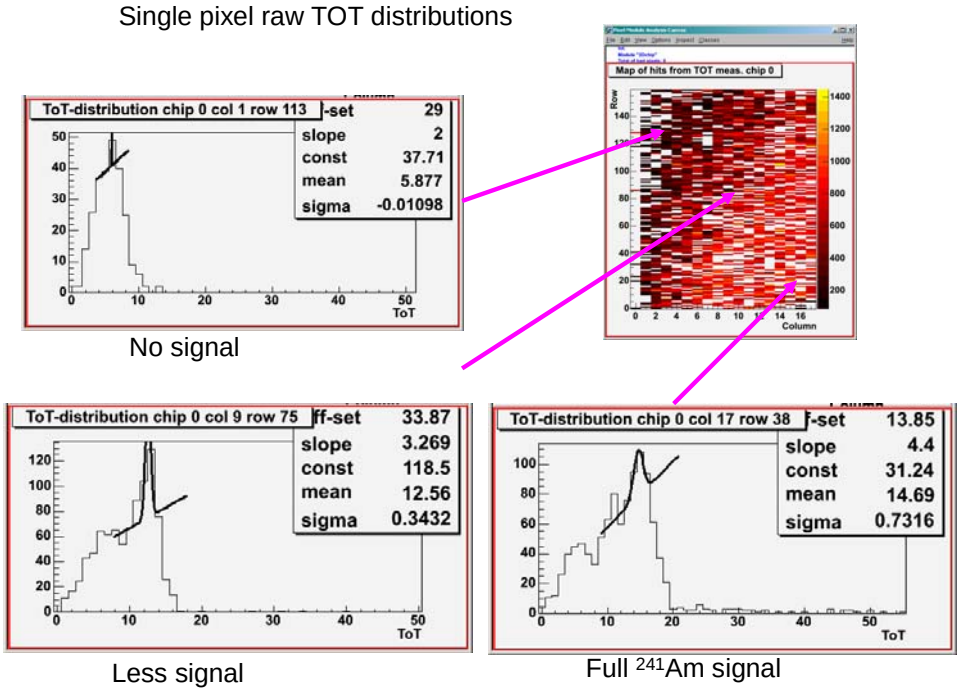

Figure 5. Test results from sensors made in the 5-week run, bonded to an ATLAS readout chip, and irradiated to past type reversal. (from Maurice Garcia-Sciveres)

Type inversion occurs at a tiny fraction of the radiation limit of these sensors, so this should not cause any problems. Full depletion can now be reached for some of the

sensors, allowing completion of the original test, to see whether the capacitance of 3D sensors would be within the operating range of the front end circuit. First indications are that the capacitance is within the range. (Other measurements, including those in New Mexico, also indicate it may be less than originally expected.) Figure 5 shows one of the slides from Maurice Garcia-Sciveres of the first test results of the irradiated sensors.

We will wait for tests of the new sensors before deciding if we need to reduce that capacitance, which can be done as shown in Figure 6. This method, allowing the bias electrode voltage to float in response to the fast, small signals from tracks, has been a possibility for several years, but would take an extra mask step to form the resistors, and so would only be done if needed.

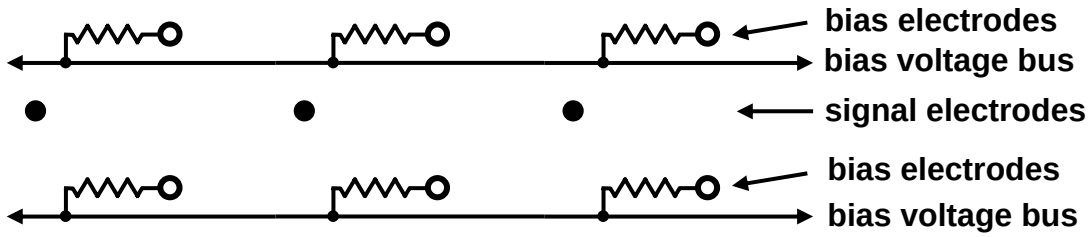

Figure 6. Method for reducing the effective capacitance of the signal electrodes. The capacitance between each signal electrode and the bias-electrode network is effectively removed if on average, τ (pulse to pulse) >> RC >> τ (pulse length), where C is the individual bias electrode capacitance. The resistors would be formed from a deposited layer of polycrystalline silicon.

B. Speed

Speed is not one of the formal requirements of the B-layer replacement or of the ATLAS upgrade. It is, however, possible that the collision interval may be reduced. In addition, if FP420 is accepted to measure far-forward protons in ATLAS, and is to work at high intensities, measurements of their vertex location must be made to identify related tracks in the main detector. Neither x nor y measurements are useful to determine anything other than the tracks came from the intersection region, due to its narrow transverse dimensions, which are comparable to the resolution of both the central detector and to the uncertainty, due to Coulomb scattering (even at 7 TeV!) of tracks extrapolated back 420 m. Precise timing measurements are planned, using some form of Cerenkov counter at the ends of the ± 420 m groups. Since sensors similar to those being developed for ATLAS are planned for FP420, it seems worthwhile to investigate the time resolution possible if a group of 3D sensors, specialized for speed, was added at or near the end.

With appropriate electronics, high speeds are readily available from 3D sensors because:

1. The lateral cell size can be smaller than wafer thickness, making shorter collection distances.

2. The field lines end on cylinders rather than on circles, so for any given maximum field, the average drift field is higher (price: larger electrode capacitance).

3. Since most of the signal is induced when the charge is close to the electrode, where the electrode solid angle is large, planar signals are spread out in time as the charge arrives, while 3D signals are concentrated in time as the track arrives.

4. Landau fluctuations along the track arrive sequentially in planar sensors, adding time variations to the pulse, while they arrive nearly simultaneously in 3D sensors. Time jitter from Landau pulse height variations would be minimized by using constant fraction discriminators.

5. Time variations due to track location within 3D cells do need to be corrected. Since both types of electrode can be contacted on the same side, this could be done by adding a capacity-coupled readout of the p electrodes. However, multiple layers will probably be used to reduce jitter from amplifier noise, and so they could be easily staggered to help measure track locations.

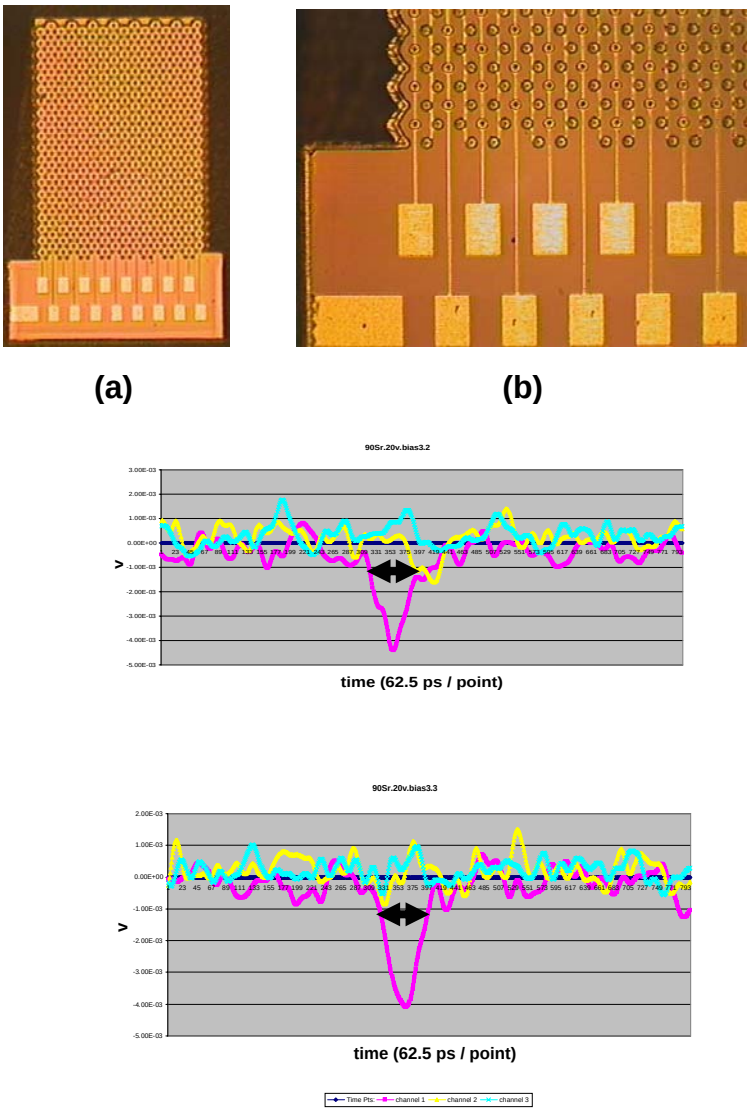

Figure 7. (a) A hexagonal-cell sensor with 16 channels, each having 20 hexagons with 50-µm sides tied together. (b) A magnified view of the bottom of the sensor. (c)

The first two of 100 ^{90}Sr pulses from the multi-channel, transimpedance, 0.13 μm, radiation-hard amplifier used for the sensor readout. The arrows are 5 ns long.

Figure 7 shows part of the initial results, using a 0.13 μm transimpedance amplifier [12 – 14]. The main source of error for a constant fraction discriminator is likely to be amplifier noise rather than track width or delta ray ranges. Overlapping pulses will not cause errors, since 3D pulse widths are shorter than even the shortest bunch interval being considered, unless the sensor channel area is large enough to produce double hits. Larger pulses would be expected to have smaller errors. Measuring such errors for the first 20 pulses of the run gave an average of 131 ps, with the largest expected error of 286 ps and the smallest of 40 ps. It should be emphasized, these are very preliminary results. Direct measurements of time variations between two similar sensor – readout circuit combinations are planned.

C. Radiation hardness tests.

With the first rough calculations in 1995, and more precise ones for the first publication [1] it was clear 3D sensors could be designed to be radiation hard if narrow enough electrodes could be put closely together. Results showing a signal-height plateau over a range of bias voltages from 105 to 150 V for 10^{15} 1 MeV equivalent neutrons / sq. cm., signal efficiency, and other topics were published some time ago [5, 7, 8]. Cinzia Da Via with the group of S. Pospisil, V. Linhart, T. Slavicek, and T. Horadzov (Czech Technical Univ. – ATLAS), using reactor neutrons and an ATLAS–pitch sensor, have now extended the range studied by nearly an order of magnitude as shown in Figure 8.

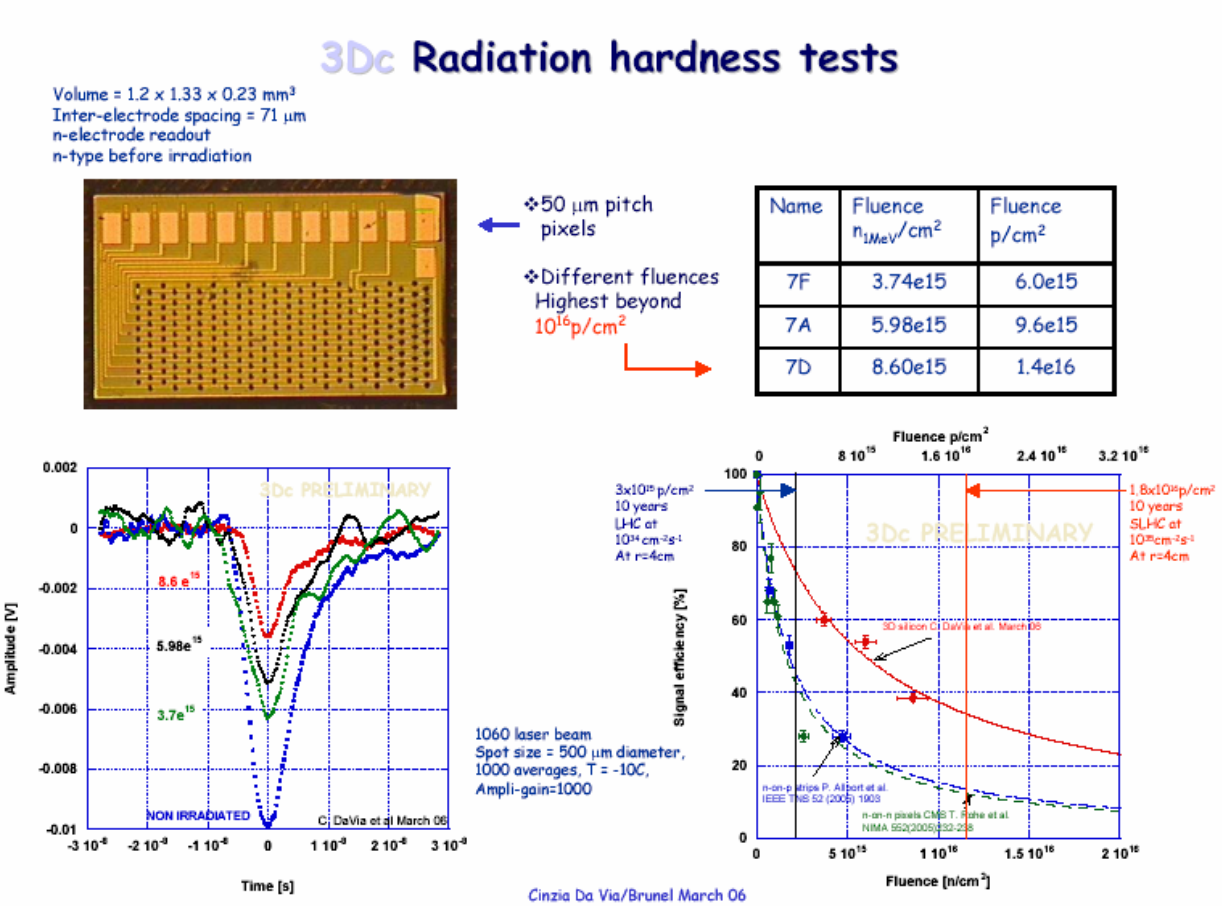

Figure 8 – Irradiation results for small 3-electrode / pixel ATLAS – spacing sensor. From the upper-left clockwise: the sensor, irradiation fluence exposures, signal efficiency as a function of radiation fluence, and averaged infrared laser pulses.

Note that **signal efficiency**, or:

received signal (irradiated sensor) / received signal (unirradiated silicon)

is used rather than charge collection efficiency, since charge that drifts from a region where the collection electrode subtends a small solid angle (equivalently, has a small Ramo weighting potential) to one where both are large, but is captured before reaching the collection electrode, can still give a significant signal. In general it will not polarize the sensor since it can usually be released from the trap within microseconds.

While major improvements are possible and very desirable, and the important topic of oxide damage must be investigated and designed for, ATLAS–pitch 3D sensors already meet what are expected to be two of the great challenges for survival in the LHC: high depletion voltages and high charge carrier capture rates in damaged silicon.

Plans for the coming year.

It is easy, in general, to specify what we should do:

1. Fabricate enough sensors to satisfy the ATLAS and FP420 research needs.

2. During the fabrication run(s), make changes to improve the yield.

3. Have special developmental fabrication runs to improve the basic sensor performance and radiation hardness. Be prepared to try new materials if ones with much better resistance to radiation damage are developed.

For example, data from (1) a tagged and localized 120 GeV muon beam run [16] and (2) several runs using x-ray microbeam scans at two different synchrotrons [9] indicates the polycrystalline silicon electrodes, which were expected to have nearly zero efficiency, in fact have efficiencies ranging from about 1/3 to about 2/3. These results cannot be totally due to tails on the x-ray beams overlapping single-crystal silicon, or to unexpected inaccuracies in the muon beam silicon telescope, since the efficiency regularly changes back and forth from about 1/3 to about 2/3, rather than remaining at some constant value. The higher efficiency electrodes are all n ones. In the fabrication process, they are made first, spend the most time at high temperatures, and so should have larger grain sizes and consequently longer polycrystalline silicon charge carrier lifetimes. Higher efficiencies could imply effectively narrower electrodes with lower capacitances (but higher electric fields), and might allow an increase in electrode density and decrease in electrode separation.

4. Test the sensors both separately and bonded to readout chips, electronically, with light beams, with sources, and with high energy beams.

5. Start advanced planning for B-layer replacement items that could affect current developments, such as preliminary mechanical, cooling, and hybrid designs. One example of an early decision: should we use the high-yield and possibly fast parallel readout available from a one-sensor – one-readout chip arrangement or should we just use a modification of the present design with many chips on one sensor? Wafer saws may play a role.

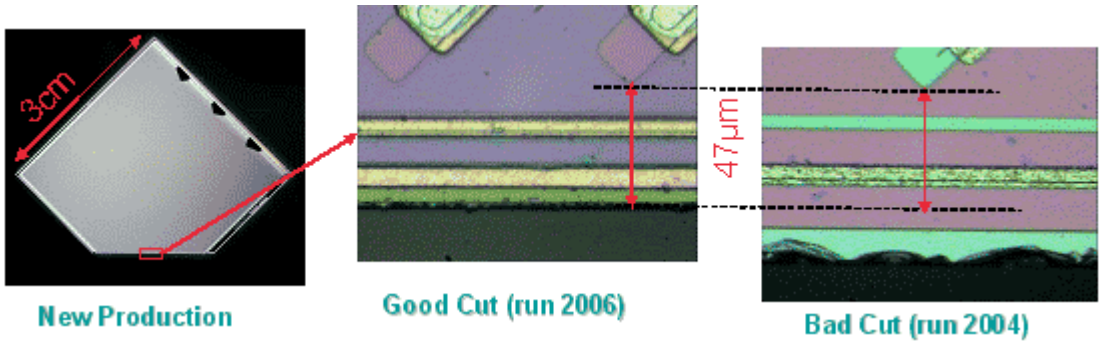

Figure 9. Improvements in wafer dicing. (From a talk by Gennaro Ruggiero at the June 2006, TOTEM collaboration meeting.)

Given the value of VLSI circuit wafers diced in one day by a diamond saw and so, the advantages of narrow saw lanes, the improvement shown in Figure 9 comes as no surprise. With our active edge technology, this is important for us for use only in dicing the readout chips. We may, using variable-offset bump pads, similar to those for our synchrotron x-ray detector, be able to make one-sensor – one-readout chip assemblies without needing long, or ganged pixels along the edges. We might use pixels a few

tenths of a micron larger than those of the readout circuit, providing a sensor overhang of some tens of microns beyond the readout chip on all sides but the one with the control electronics and the wirebond pads.

The complexity in making specific decisions comes from current uncertainties in experimental results – mainly the yield for good sensors from the current fabrication run – and on funding. During the period FY1997 – FY2006, while this advanced work has been underway, the rest of the Hawaii group has had a 6 % increase from $1,375,000 to $1,455,000, we have had an 82% decrease from $245,000 to $45,000, have lost our post-doc position, and have gone from 15% of the Hawaii budget to 3%. For purposes of this budget, I will tentatively assume:

1. The cost for fabrication runs is reduced by FP420 (Brunel University, UK) covering the salary of the associate engineer (Dr. Jasmine Hasi), as they did last year.

2. In addition, they provide, as planned, 30,000 pounds, approximately **$55,500.**

3. ATLAS covers the entire year's salary of the senior engineer, Dr. C. Kenney. If the funds are routed through the Molecular Biology Consortium, with no overhead, this will be **$113,732**, including benefits. If they are routed through the University of Hawaii with 20.6% overhead, as was chosen for the 3-month amount in this year's funds, it would be **$137,161**, or possibly less, as Hawaii does not charge overhead on some individual contracts after the first $25,000. The time not spent by Dr. Hasi and Dr. Kenney on fabrication will be spent on testing sensors and running experiments for fabrication and sensor improvements.

4. Instead of one production (item 1 above) and one developmental R&D fabrication run (item 3 above), we have just 1.1 runs:

A. Complete the processing of the remaining nine wafers of the present run, investigating the effect of etching on the aluminum – electrode insulating barrier seen in the earlier fabrication run and now mainly seen in parts of two of the three wafers with deposited metal. This will provide (300 x yield) ATLAS sensors in addition to specialized sensors for FP420, which should be enough for ATLAS and FP420 for the coming year.

B. Complete one developmental fabrication run, to improve the basic sensor performance and radiation hardness.

The table in last year's report shows the basic costs of a 3 month fabrication run. Completion of the present run should take about a month, and only lab expenses of $2,500 x 2 plus $1,000 for miscellaneous supplies will be needed: **$6,000.**

Modifying the table for the developmental run, omitting the first two salaries, gives:

Developmental Run

				Totals	
Fab Time per person	$2,500.00	per month	12 months	Total Fab =	$30,000.00
FZ Wafers	$80.00	per wafer	12 wafers	FZ Wafers =	$960.00
CZ Wafers	$25.00	per wafer	20 CZ wafers	CZ Wafers =	$500.00

Implants	$550.00	per batch	2 per batch	Implants =	$1,100.00
Polishing	$40.00	per wafer	12 per batch	Polishing =	$480.00
Misc. Supplies	$1,000.00	per batch		Supplies =	$1,000.00
Senior Eng.	$10,000.00	per month	3 months	Senior Eng =	
Associate Eng.	$1,600.00	per month	3 months	Ass. Eng. =	
Consulting Eng.	$80.00	per hour	75 hours	Consulting Eng. =	$6,000.00
				Cost for Run =	**$40,040.00**
Masks	$500.00	per mask	8 masks	Masks =	$4,000.00
Sputter (Au, In, Ti)	$2,500.00			Sputter Sources =	$2,500.00
				Total =	**$6,500.00**
GPIB Board	$600.00				
DAQ Software	$1,600.00				
DAQ Computer	$3,000.00				
Analysis Software	$2,000.00				
MicroProbes	$500.00			**Total Equipment =**	**$7,700.00**

Total Funds Needed: **$54,240.00**

.

5. I assume the DOE. Hawaii contract covers my salary, benefits, and overhead of **$184,787**, still less than the $245,000 in Hawaii funds in 1997 when this work was just starting. I also assume that my equipment and travel expenses come from the Advanced Detector Research funds of **$22,000.** Then, unlike last year, when Hawaii funds were further cut to $45,000 these items would not affect this budget or the work we are able to do this year.

6. The total expenses would then be:

($113,732 or $137,161) + $6,000 + $54,240 = $173,932 or $197,401.

Available funds would be:

$129,000 + $55,500 = 184,500.

Sherwood Parker

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[16] We have extensive, as yet unpublished, data from both X-ray microbeam and muon beam runs (the latter nearly ready for publication).

WBS 4.1.1.1

Development and Testing of 3D Active-Edge Silicon Radiation Sensors with Extreme Radiation Hardness: Progress Report and Proposal

16 June 2006

M. Hoeferkamp, S. Seidel, and I. Gorelov
University of New Mexico

Progress, 1 October 2005 – 16 June 2006

Introduction

Our activities during this period were of two types. The first type involved characterization of leakage current, depletion voltage, electrode capacitance, and charge collection speed in non-irradiated and irradiated 3D sensor prototypes. The second set of studies was based on laser testing of the same devices, and included measurements of depletion voltage, charge collection uniformity (using "position scans"), and capture time. Results of these measurements were presented at the UCSC Inner Detector ATLAS Upgrade Workshop on November 10, 2005, at the 3D and p-type Workshop at Trento on February 13, 2006, at the US Pixel and Upgrade meeting at LBNL on March 3, 2006, and at the 3D Workshop at Brunel University on June 1, 2006. The results will be presented at the Eighth RD50 Workshop in Prague on June 26, 2006.

All measurements were performed on early generation sensors obtained from Sherwood Parker. The irradiated samples received a fluence of 1 x 10^{14} cm^{-2} 55 MeV protons, 2 x 10^{14} cm^{-2} 55 MeV protons, and 1 x 10^{15} cm^{-2} 55 MeV protons. They are arrays with alternating columns of n and p-type electrodes whose pitch between adjacent electrodes of the same type is 100 microns in one direction and 200 microns in the perpendicular one.

Leakage Current

The measurement of reverse bias leakage current on the non-irradiated n-electrode (see Figure 1) confirms that prior to irradiation, n electrodes are not fully isolated from each other due to oxide surface charge. After irradiation to a fluence of 10^{15} cm^{-2} 55MeVp, the n electrodes are isolated and the leakage current for a single isolated n electrode is 475 nA (measurement normalized to temperature T_{norm} = 20ºC) at 80 V bias (see Figure 1). The p-electrode shows a leakage current of 365 nA (T_{norm} = 20ºC) at 80 V bias (see Figure 2).

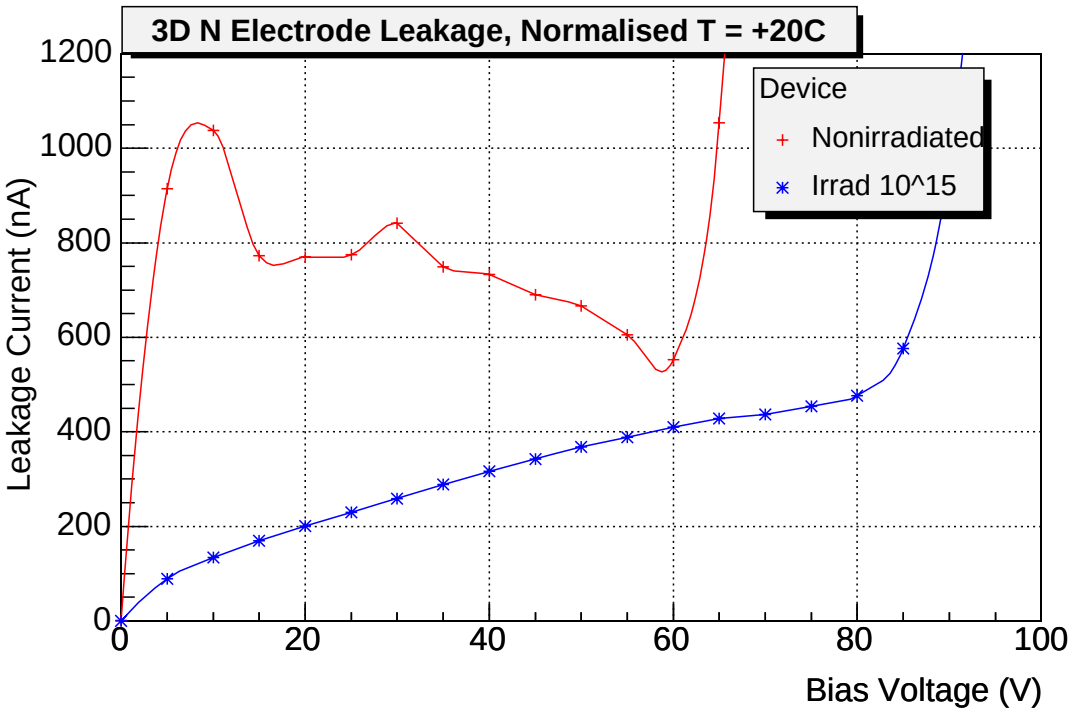


Figure 1: n-type electrode leakage current versus voltage.

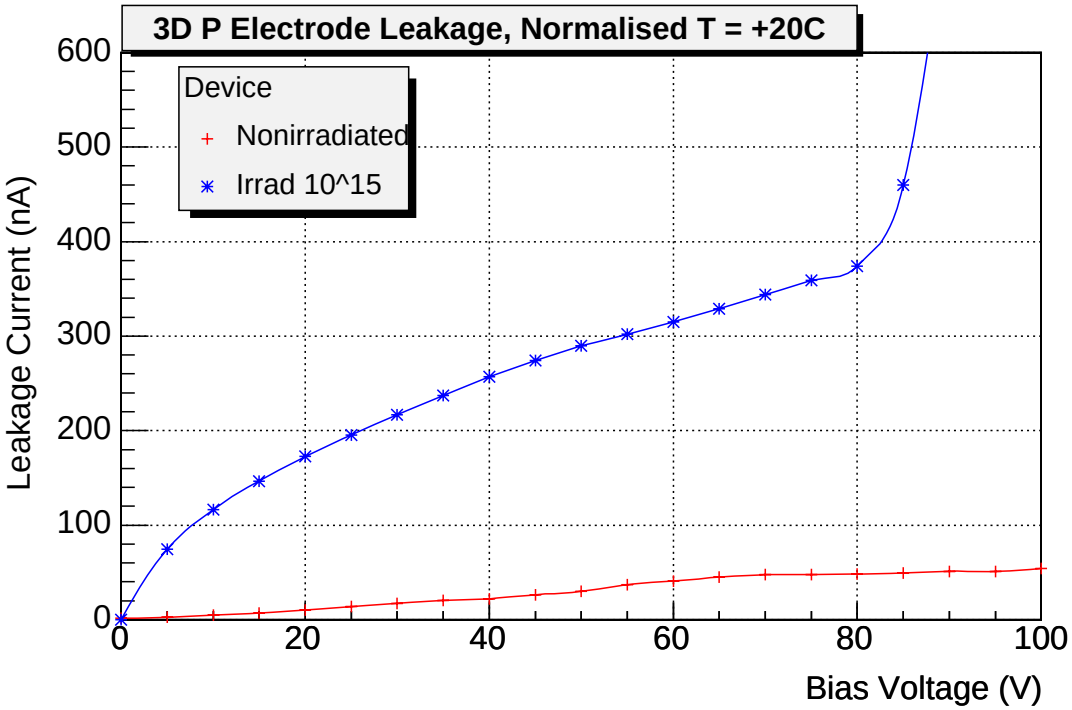


Figure 2: p-type electrode leakage current versus voltage.

Depletion Voltage

Depletion voltage was determined two ways: through a CV measurement using an LCR meter, and by observing the plateau of a signal response to a pulsed laser. The two methods yielded results that are consistent. Preliminary results indicate $V_{depletion}$ = 10V for the non-irradiated sensor and $V_{depletion}$ = 80V for the irradiated (10^{15}/cm^2 55MeVp) sensor (Figures 3 – 6 show examples of the measurements for the cases of the p-electrodes in the unirradiated device and the n-electrodes in the irradiated one). These depletion voltage measurements were performed on single isolated n- and p-type electrodes.

The depletion voltage of the entire device, that is the full array of n-electrodes and the full array of p-electrodes, was characterized separately. This was done by completely flooding the 3D sensor chip with a uniform IR (1064 nm wavelength) laser spot, and scanning the bias voltage from zero volts to above the point of full depletion (see Figure 7). The laser was pulsed with a fast (0.5 ns rise time) short duration (100 ns) pulse, and the signal pulse heights from the n-electrode and the p-electrode arrays were read out on an oscilloscope. The same three 3D sensors were tested: a non-irradiated sensor, a sensor irradiated to 2 x 10^{14}/cm^2 55MeVp, and a sensor irradiated to 10^{15}/cm^2 55MeVp. The most highly irradiated sensor was measured at -20ºC to inhibit leakage current, and the others were measured at 0ºC. The signal collection results were then normalized to the non-irradiated values. The 2 x 10^{14}/cm^2 sensor showed ~95% signal collection relative to the unirradiated one, and the 10^{15}/cm^2 sensor showed ~88% collection. Depletion voltages measured for full arrays are about 15V in the non-irradiated case, ~ 58V for the 2 x 10^{14}/cm^2 sensor, and ~ 125V for the 10^{15}/cm^2 sensor (see Figure 8).

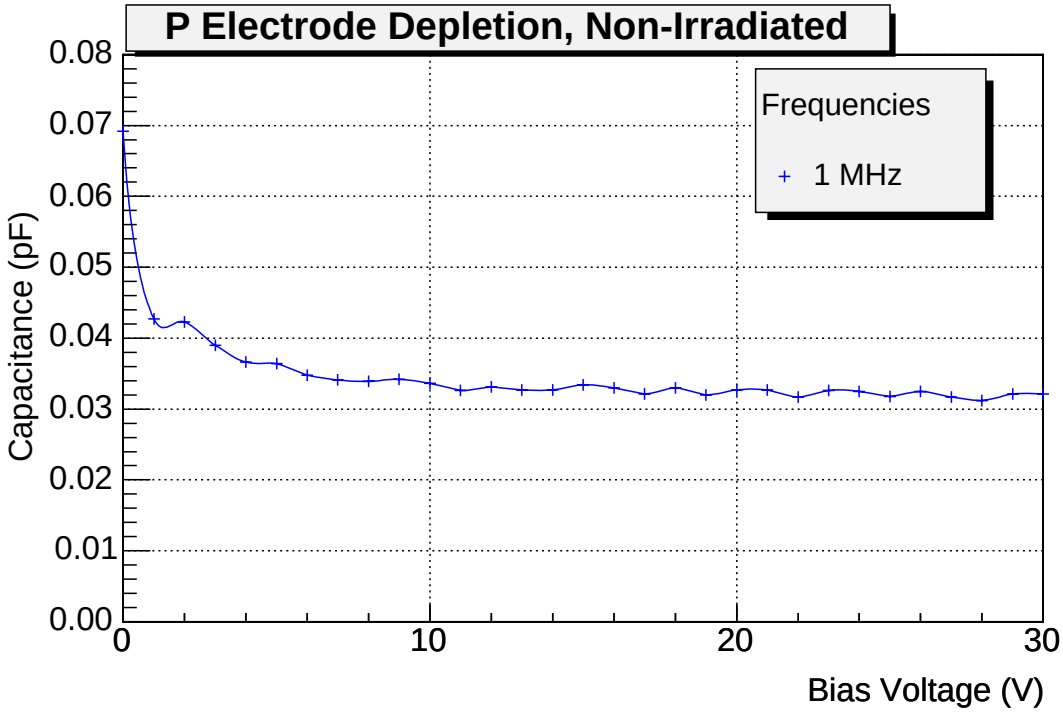


Figure 3: Capacitance versus bias voltage for the p electrode single cell in the unirradiated sensor.

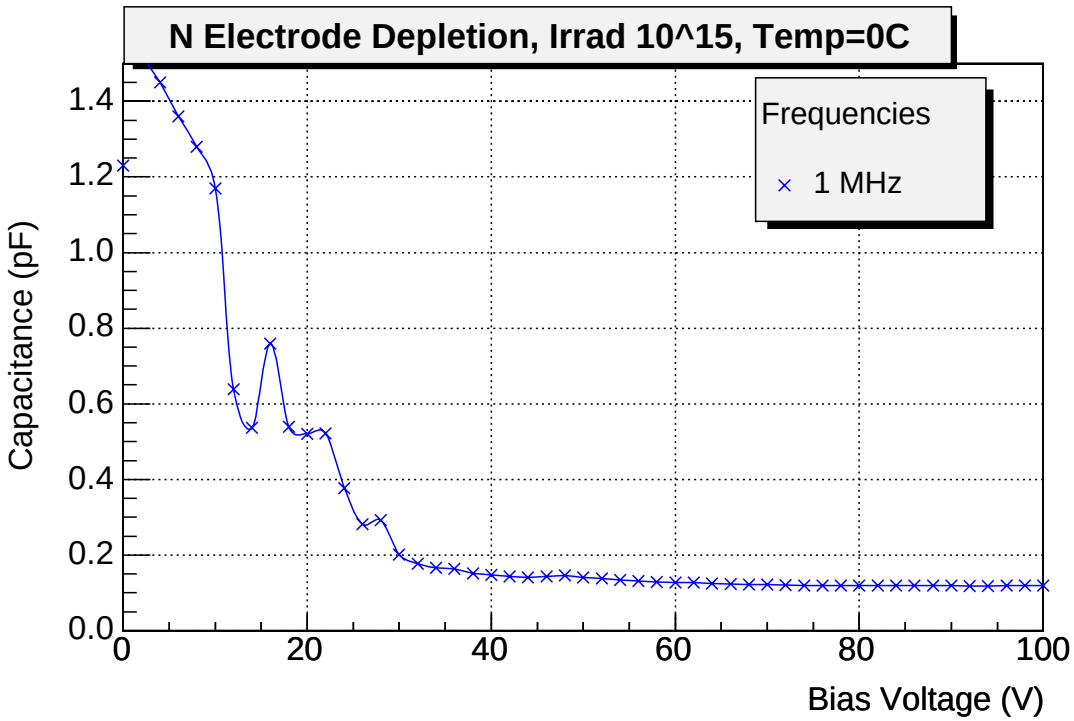


Figure 4: Capacitance versus bias voltage for the n electrode single cell in the highly irradiated sensor.

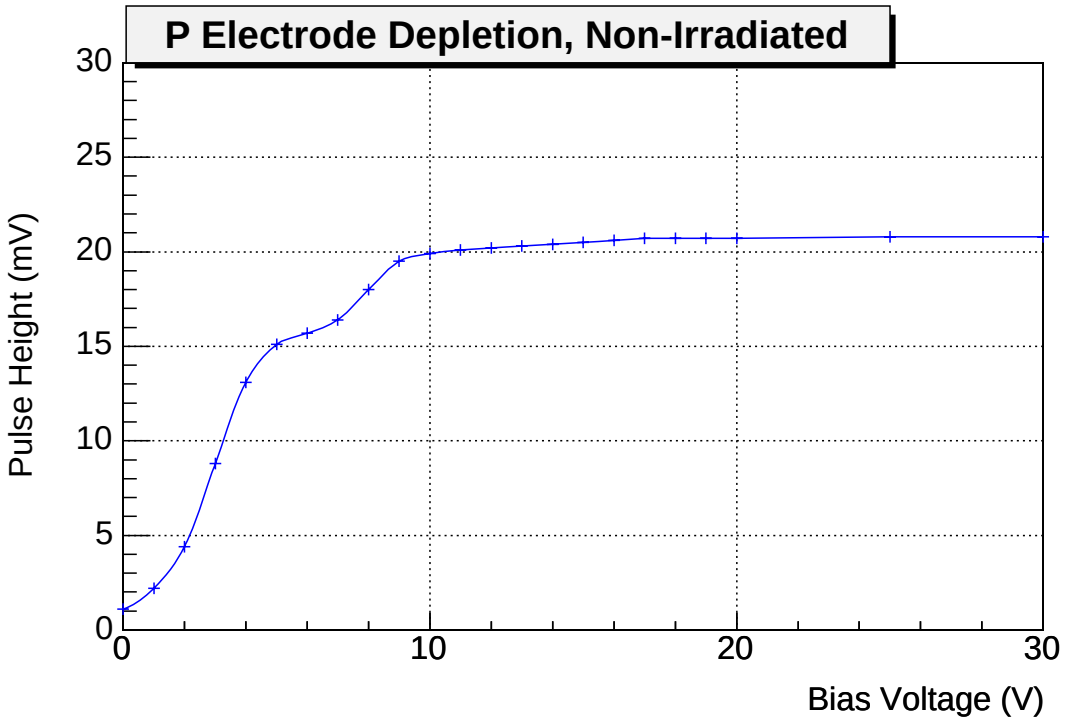


Figure 5: Pulse height recorded by the isolated p electrode in the unirradiated sensor, as a function bias voltage, under stimulation with a pulsed laser.

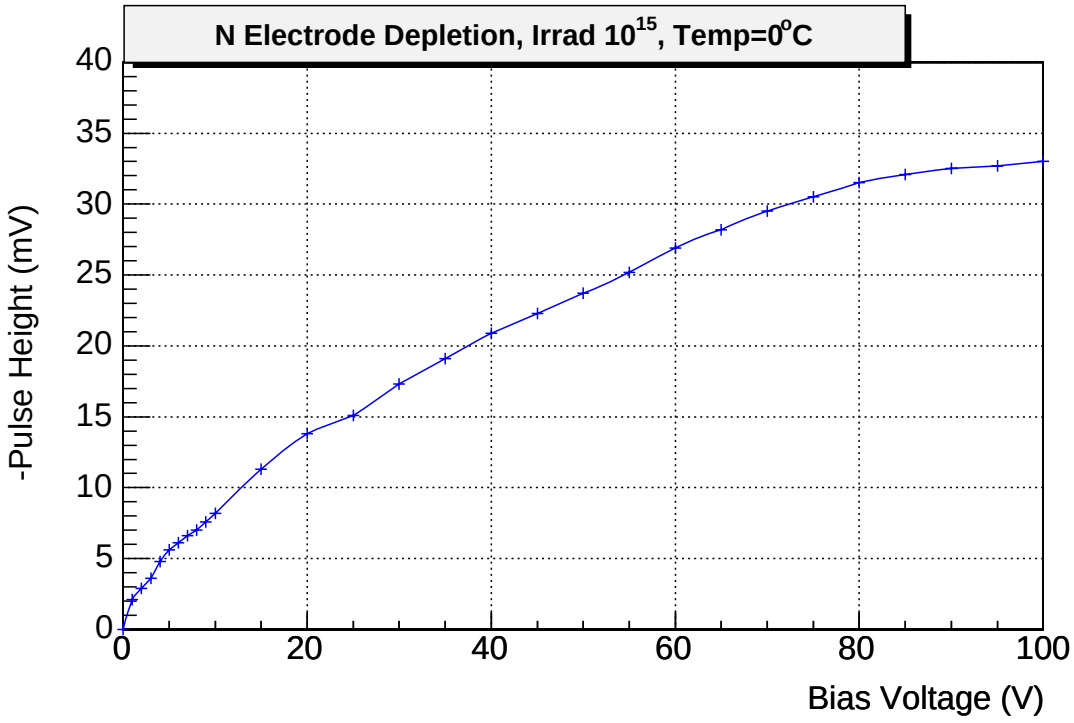


Figure 6: Pulse height recorded by the isolated n electrode in the highly irradiated sensor, as a function bias voltage, under stimulation with a pulsed laser.

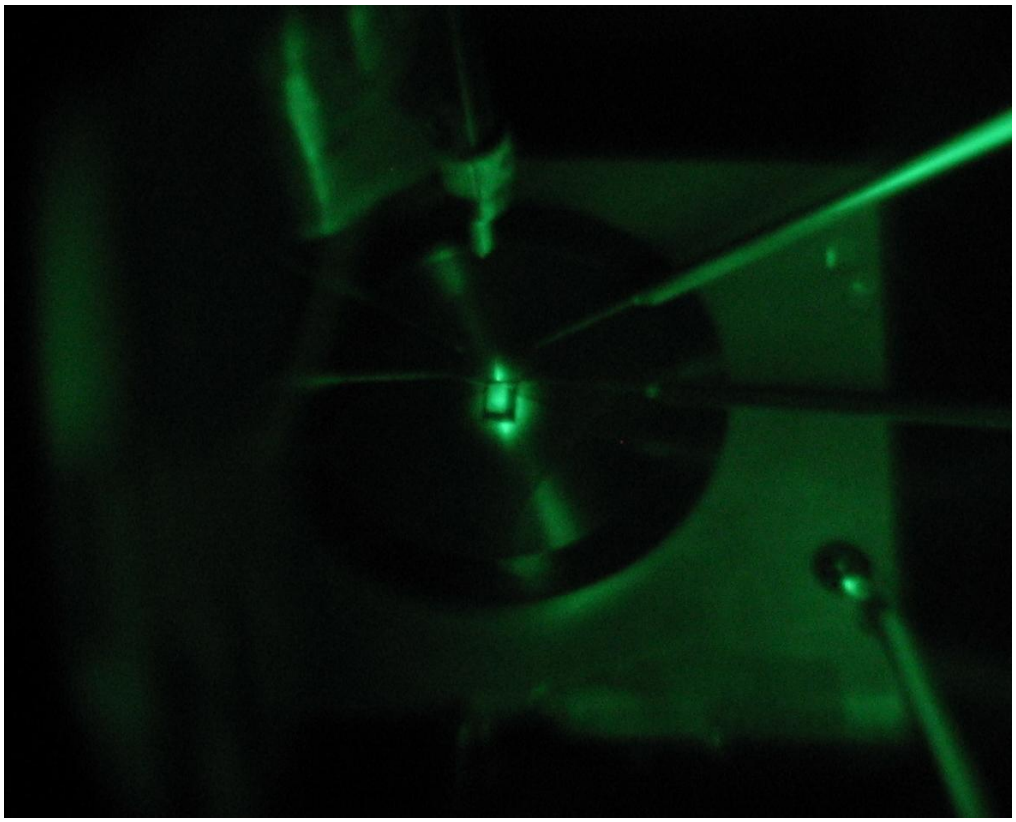


Figure 7: Photo with IR filter of 3D device completely flooded with uniform laser spot.

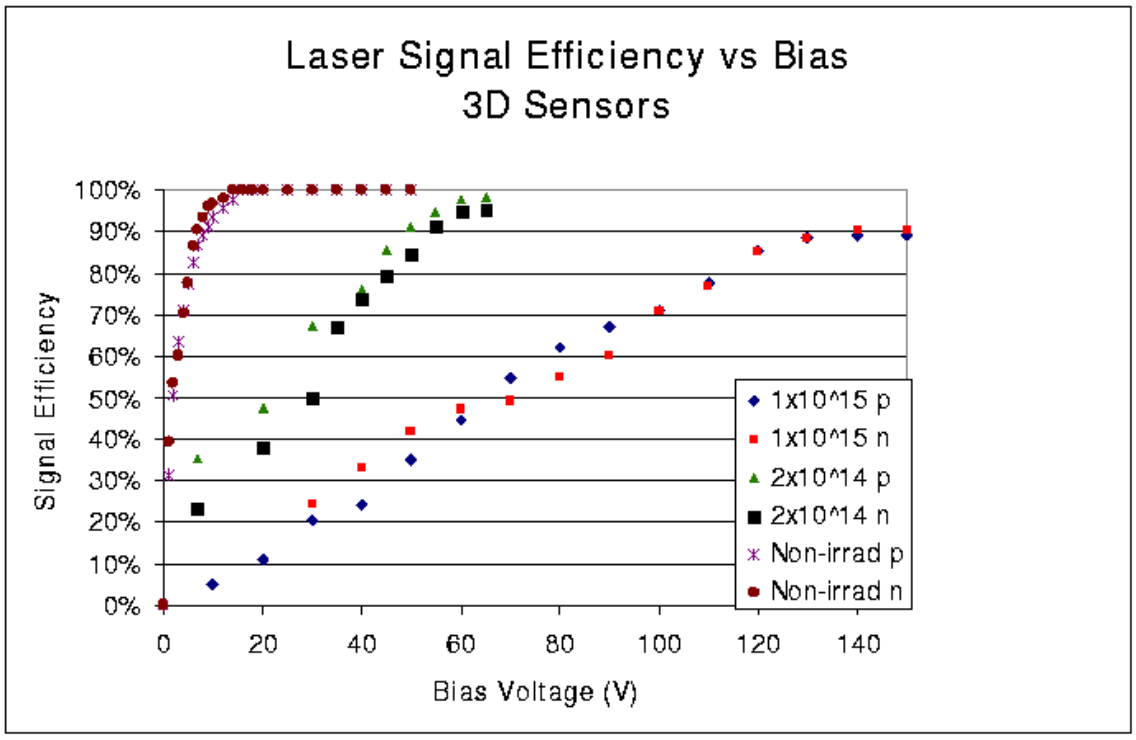


Figure 8: Signal efficiency versus bias voltage, entire sensor array stimulated with pulsed laser.

Electrode Capacitance

Electrode capacitance was measured directly using an LCR meter and indirectly by extracting capacitance from the decay time of a Picoprobe35 to a pulsed laser. The results of the direct measurement are 68 fF for the non-irradiated n electrode (Figure 9), 120 fF for the irradiated (10^{15} /cm^2 55MeVp) n electrode (Figure 10), 32 fF for the non-irradiated p electrode, and 59 fF for the irradiated (10^{15} /cm^2 55MeVp) p electrode. A diagram of the configuration used for the indirect measurement, and a example of the pulseheight observed, are shown in Figure 11. The results of the indirect method of measuring capacitance are 71 fF for the non-irradiated p electrode (Figure12) and 91 fF for the irradiated p electrode (Figures 13 and 14). Figure 13 shows the response of the irradiated p-type electrode on linear (upper) and log (lower) scales. It is evident that this response involves two different time constants. Figure 14 plots the two halves of the curve separately, each versus a straight line on the log scale. The time constant for the upper plot of Figure 14 is 152nS and, being associated with the first 350 ns of the decay, is the one used to extract the electrode capacitance. The second time constant is 278 ns and, being associated with the period from 550 ns to 800 ns, is probably due to the release of the trapped charge in this very highly irradiated sensor. To further validate these measurements, we implemented a three-dimensional electrostatic field simulation of the sensor using the Coulomb package distributed by Integrated Engineering Software, Inc. Based on the geometry of the sensor electrodes the predicted electrode capacitance of an unirradiated device is 31 fF.

Measurements of electrode capacitance for different sensor temperatures and different LCR meter frequencies are shown in Figure 15.

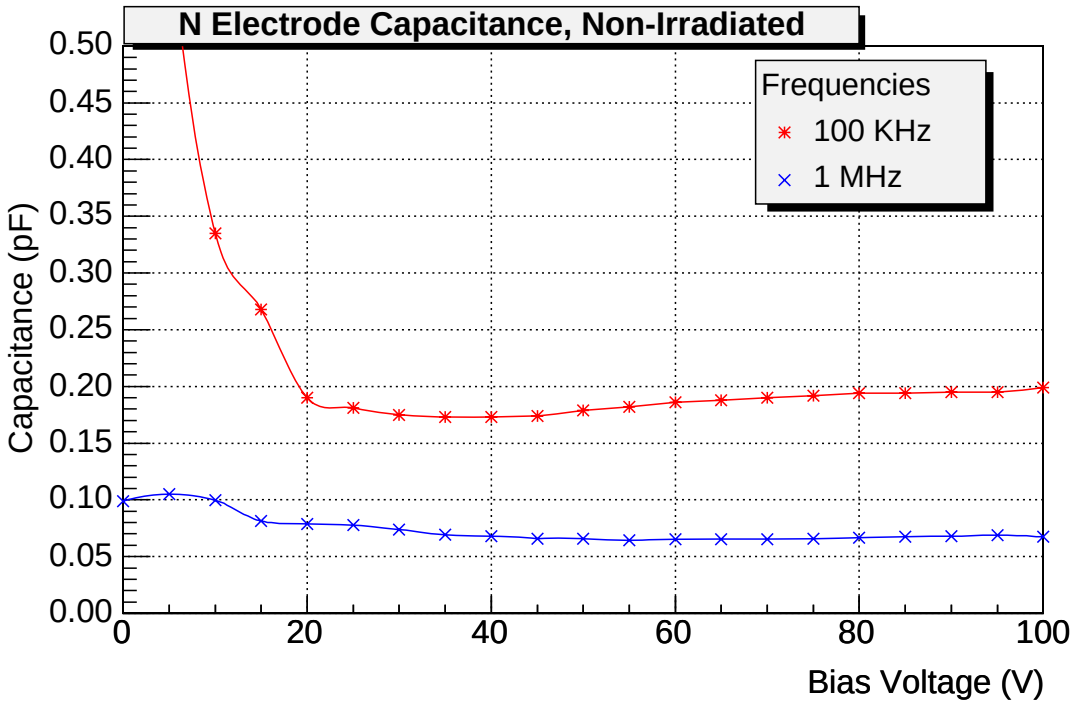


Figure 9: n-type electrode capacitance versus bias voltage for an unirradiated sensor, measured with the LCR meter.

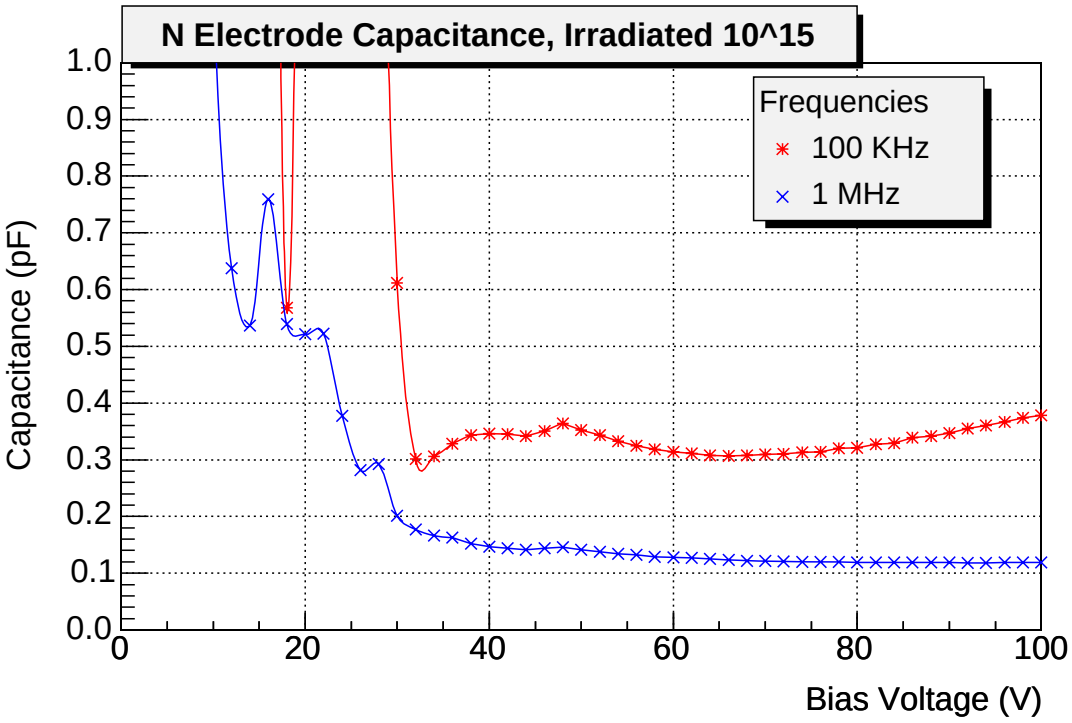


Figure 10: n-type electrode capacitance versus bias voltage for an irradiated sensor, measured with the LCR meter.

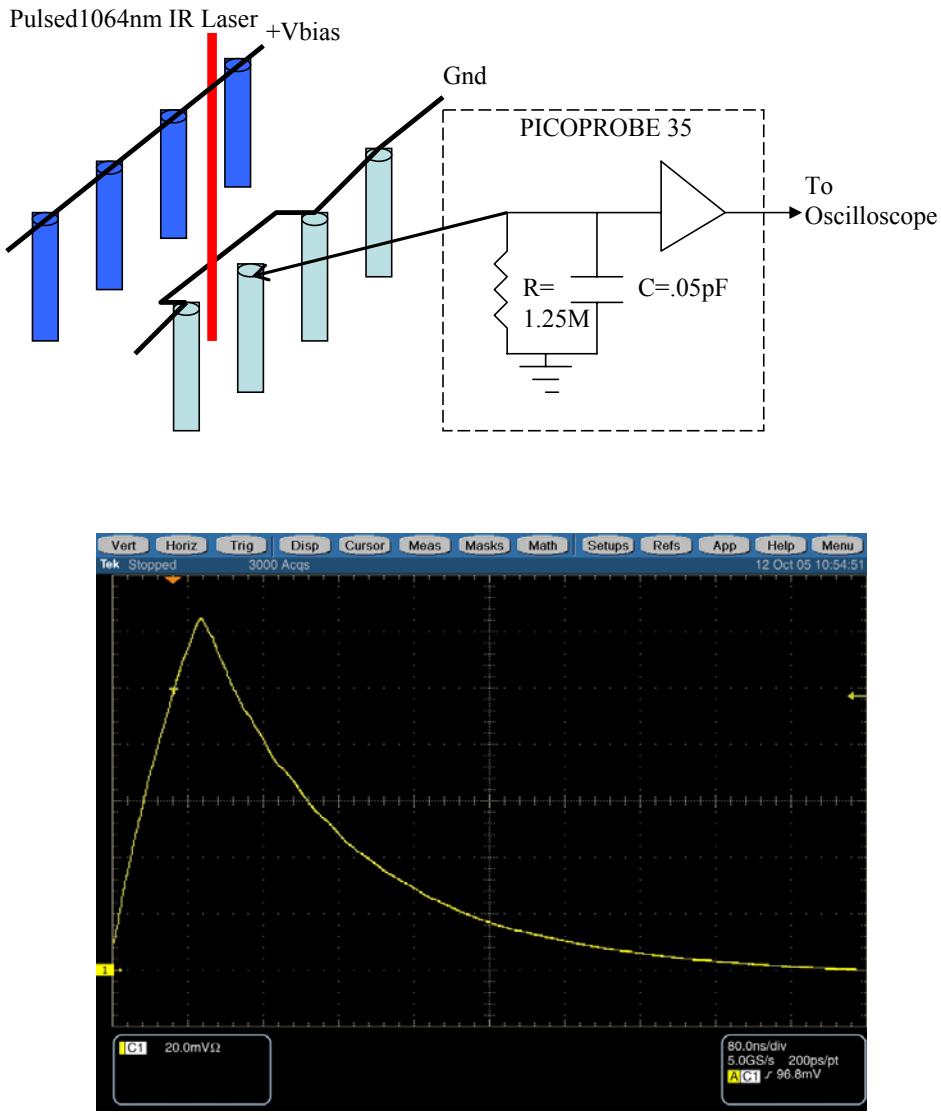


Figure 11: Experimental configuration (upper) for an indirect measurement of capacitance using the decay time of the signal (lower) on the Picoprobe35.

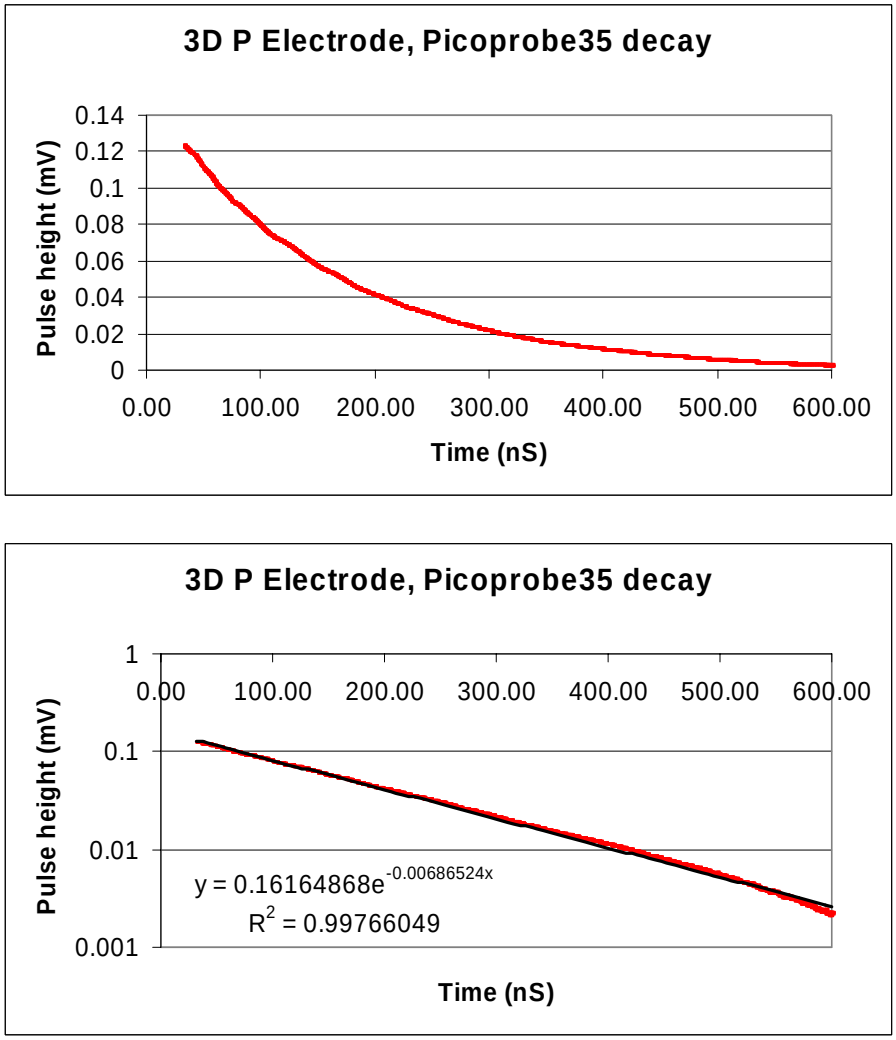


Figure 12: Pulse height versus time as an indirect measurement of p-electrode capacitance for the unirradiated 3D sensor.

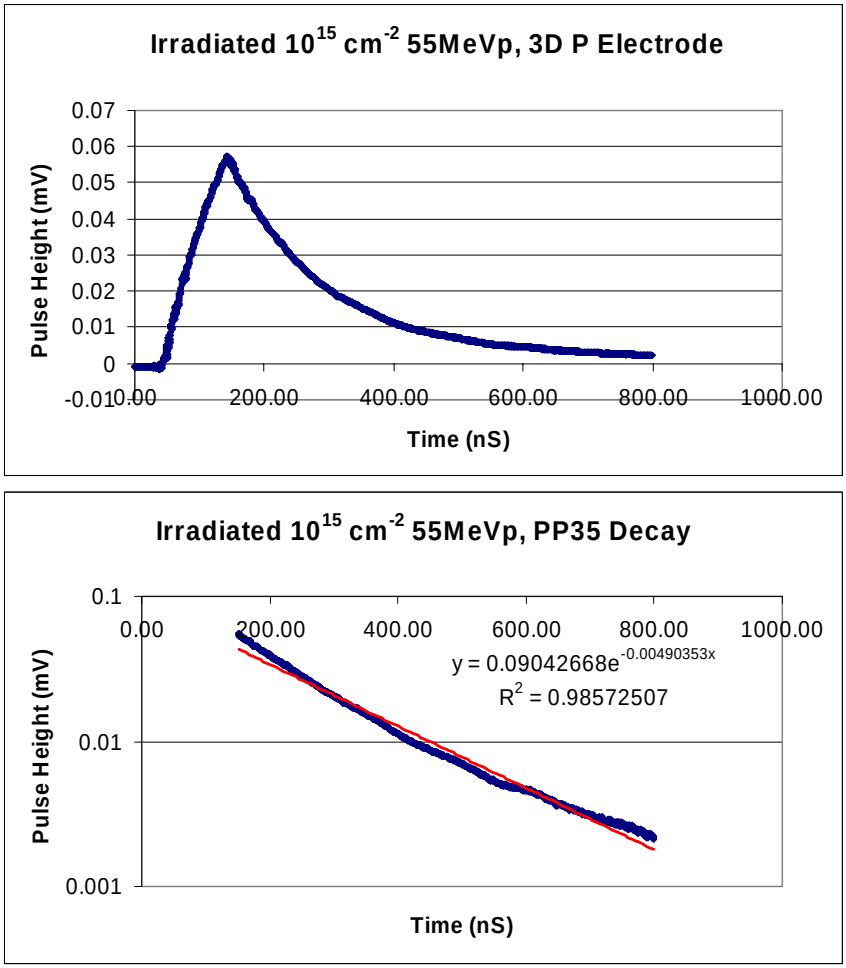


Figure 13: Pulse height versus time as an indirect measurement of the p-electrode capacitance in a highly irradiated 3D sensor. A single exponential decay does not fit the curve.

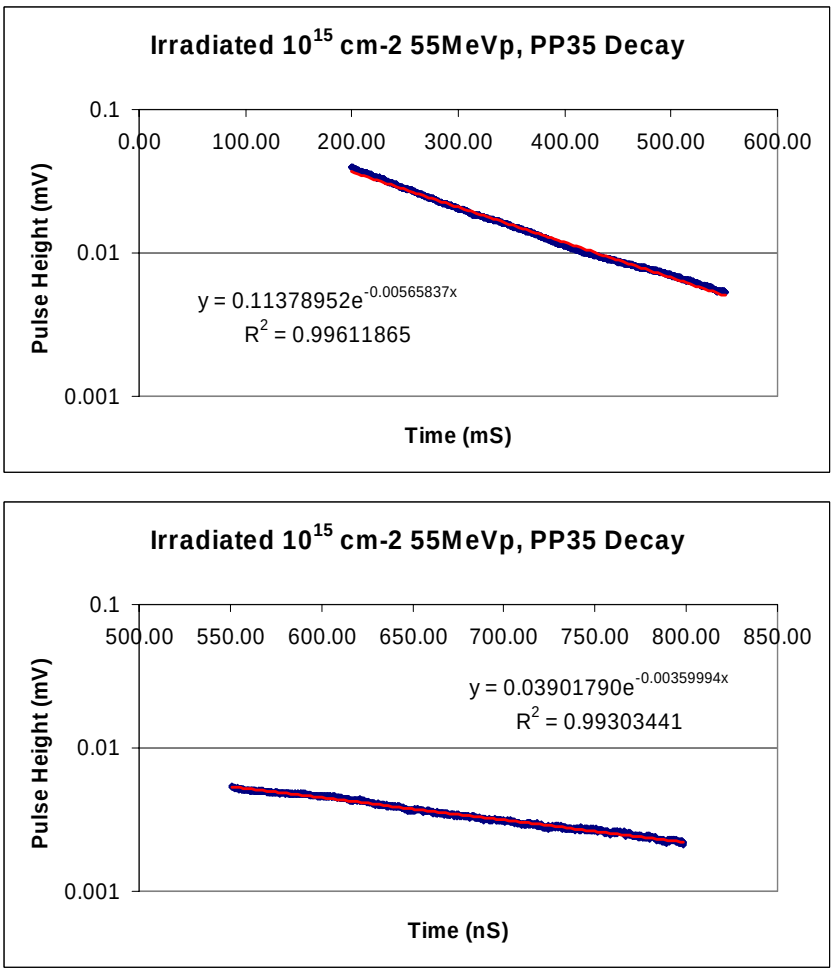


Figure 14: Pulse height versus time for two different time intervals in the response of a p-type electrode to laser stimulation of its irradiated sensor. The two time constants associated with this signal are indicated by the straight lines in the two graphs.

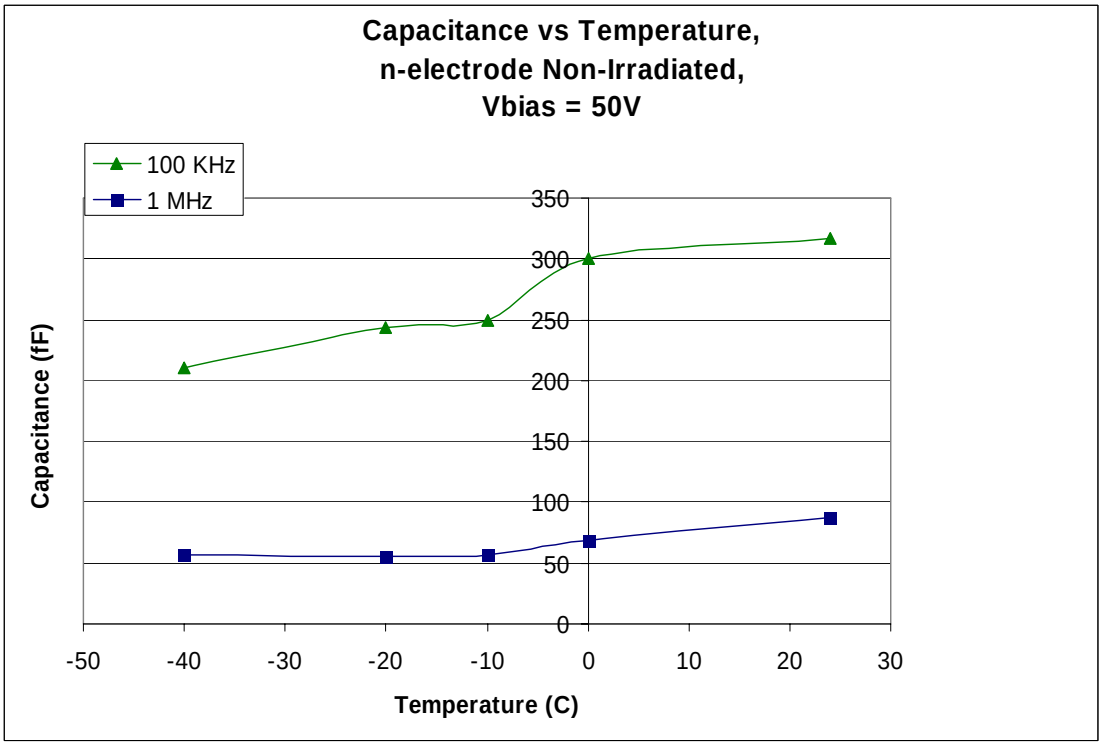


Figure 15: n-type electrode capacitance versus temperature and frequency for a fully depleted unirradiated device.

Signal Uniformity (Position Scan) Measurements

For the laser position scans the 1064nm laser was focused to a diameter of approximately 10 um. This laser spot was then scanned across one electrode cell while the response was measured through a Picoprobe35 (Figure 16) to characterize the uniformity of signal collection. The unirradiated p-electrode shows very uniform signal collection within the pixel cell for scans in both the Y and X directions (Figure 17). The signal drops to 50% when the laser is positioned halfway between electrodes, as expected. The unirradiated n-electrode scan (Figure 18), however, shows poor isolation between neighboring electrodes due to the oxide surface charge, as was reported above in the leakage current studies.

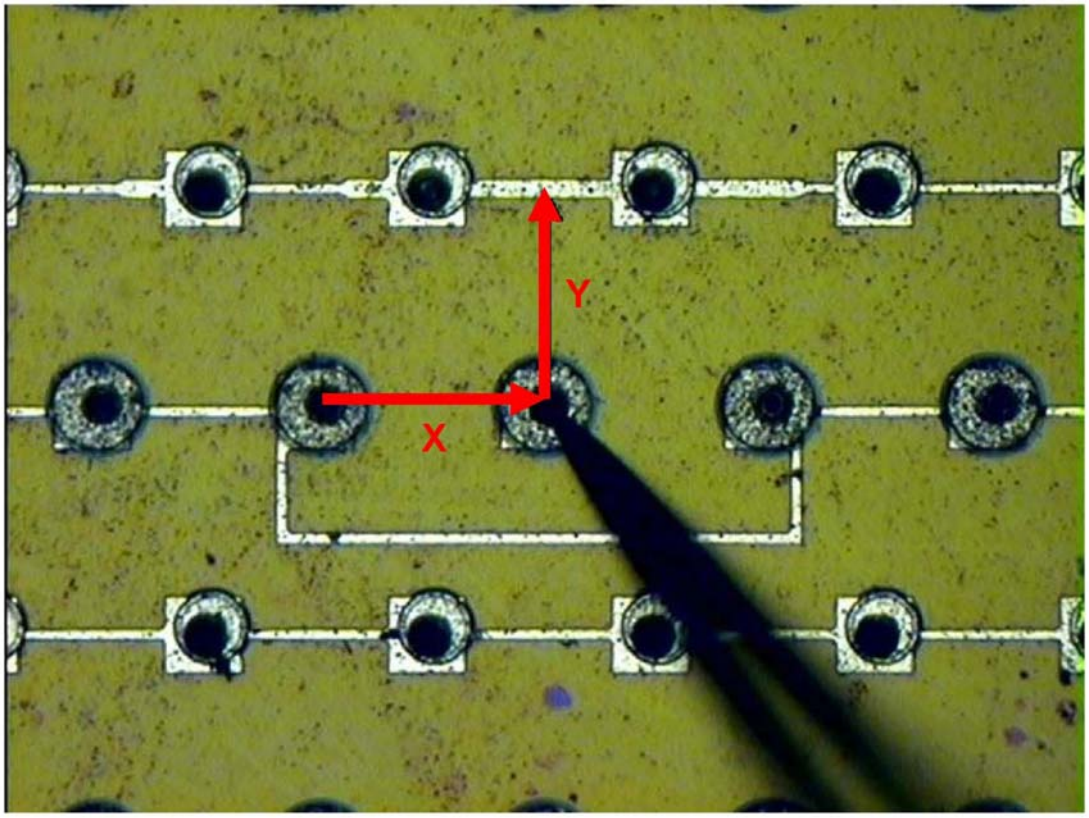


Figure 16: Isolated p electrode, showing the coordinate system for the scanned laser spot to measure the uniformity of the signal collection.

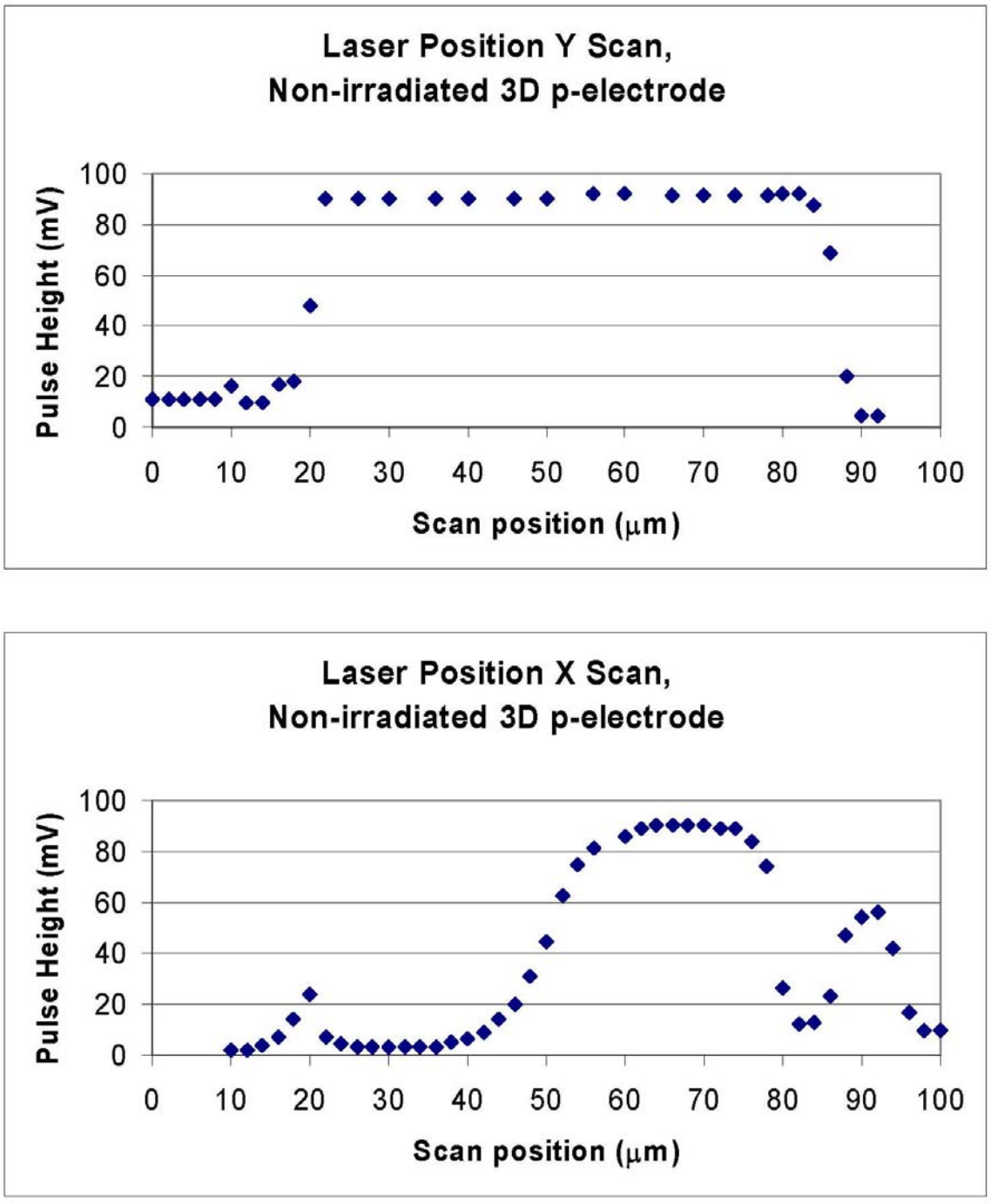
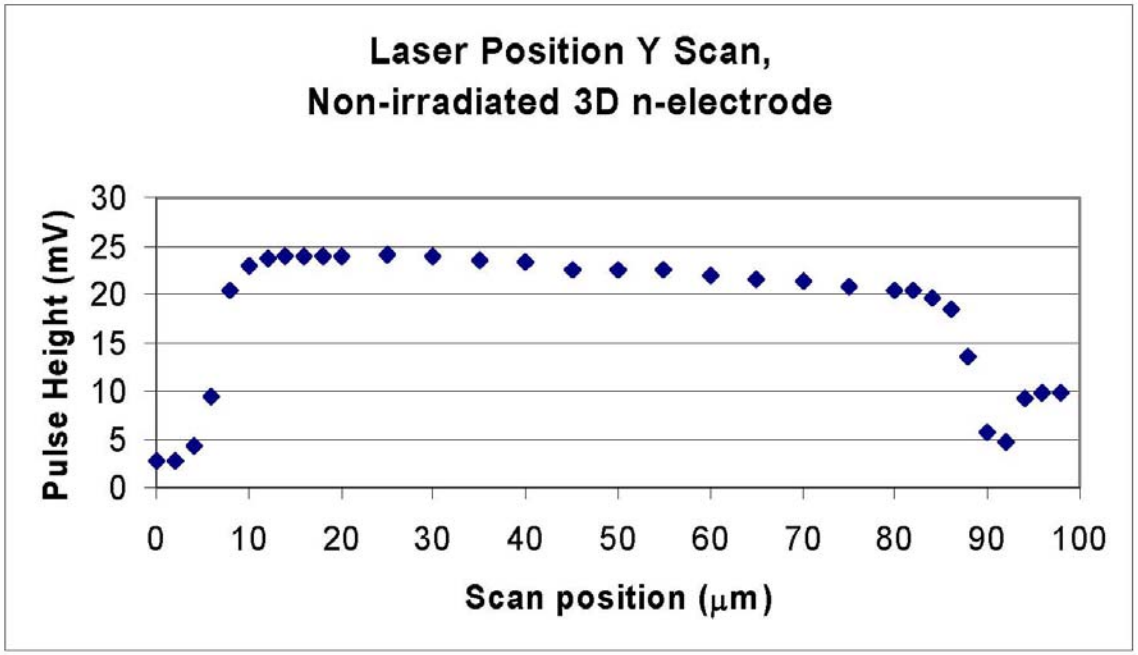


Figure 17: Pulse height recorded at the unirradiated isolated p-electrode as a function of the distance to the stimulating laser spot.



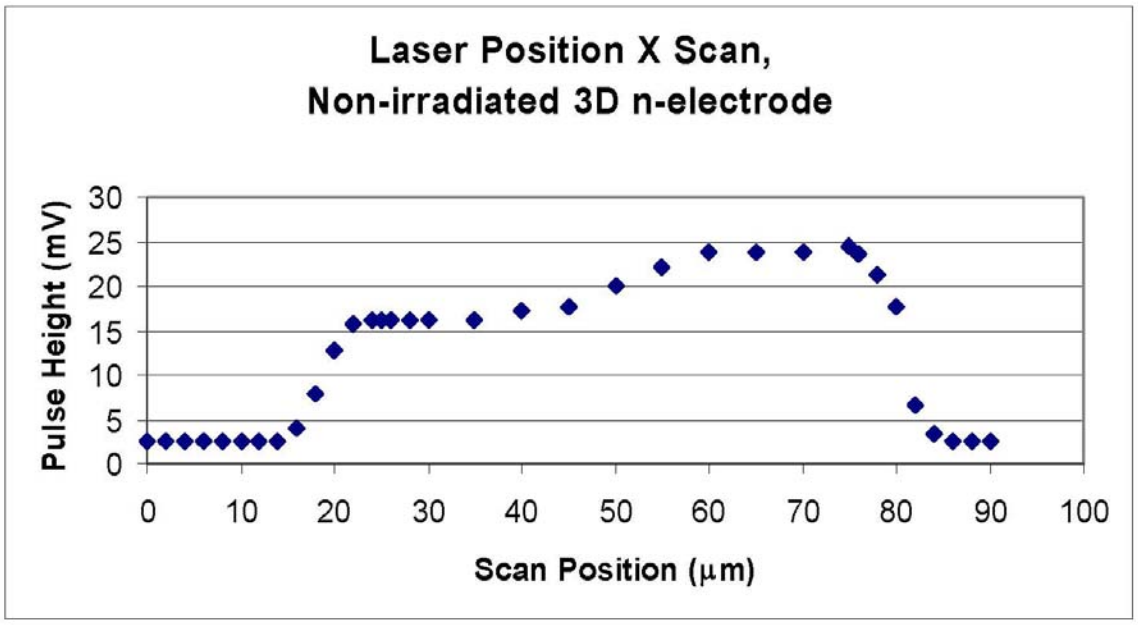


Figure 18: Pulse height recorded at the unirradiated n-electrode as a function of distance from the stimulating laser spot.

Charge Collection / Capture Time

The goal of this study is to measure the mean times between charge generation and collection for different drift distances (see Figure 19). The laser is initially pulsed with the spot at a distance of 30 μm from the electrode where the charge is to be collected. The procedure is repeated with the laser spot at a distance of 90 μm from the electrode. The capture time is obtained by taking the difference in time of arrival of the signals recorded for the two positions.

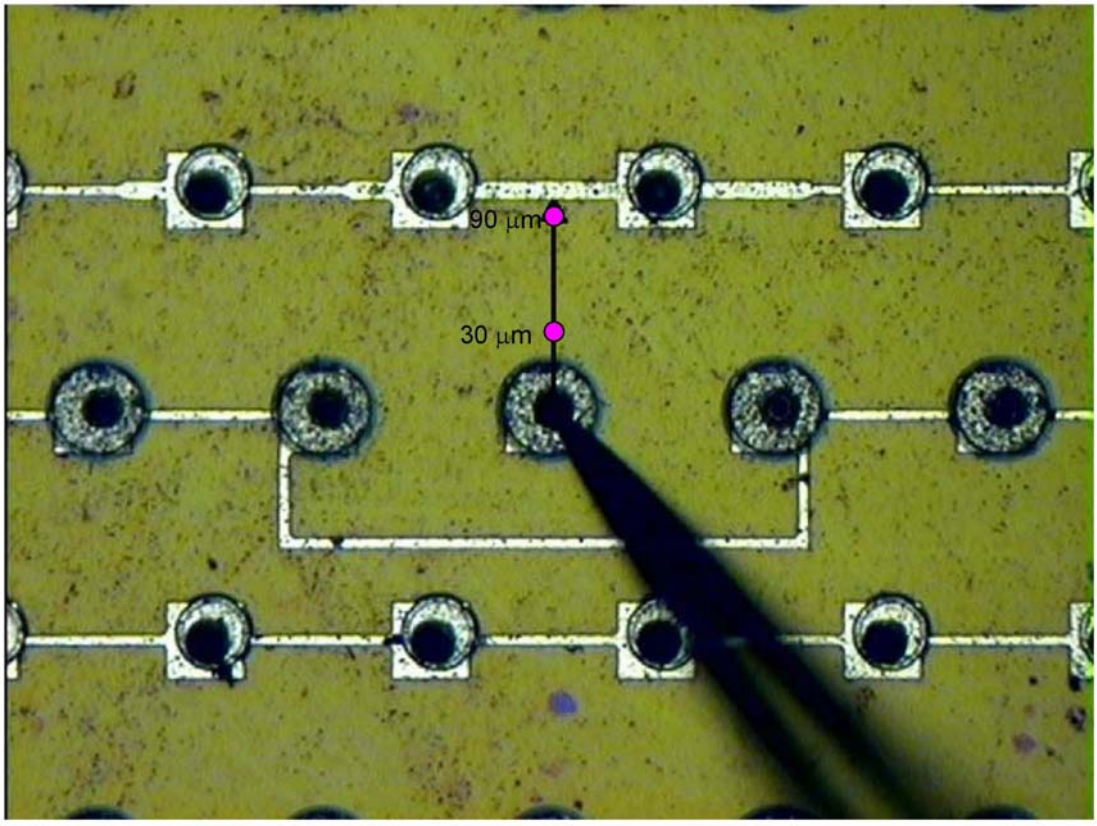


Figure 19: Diagram showing the laser spot locations used for the capture time measurement.

The study was performed on the p electrode of the most highly irradiated sensor (10^{15}/cm^2 55MeVp) at -20^{o}C and 140V bias. The time from the reference signal to the peak of the collected charge for a laser spot distance of 30 μm to the electrode was measured to be 50 ns (Figure 20). The time from the reference signal to the peak of the collected charge for a laser spot distance of 90 μm to the electrode was measured to be 51 ns (Figure 21). This very preliminary result suggests that under these conditions a 60 μm drift distance requires 1ns to capture the equivalent charge.

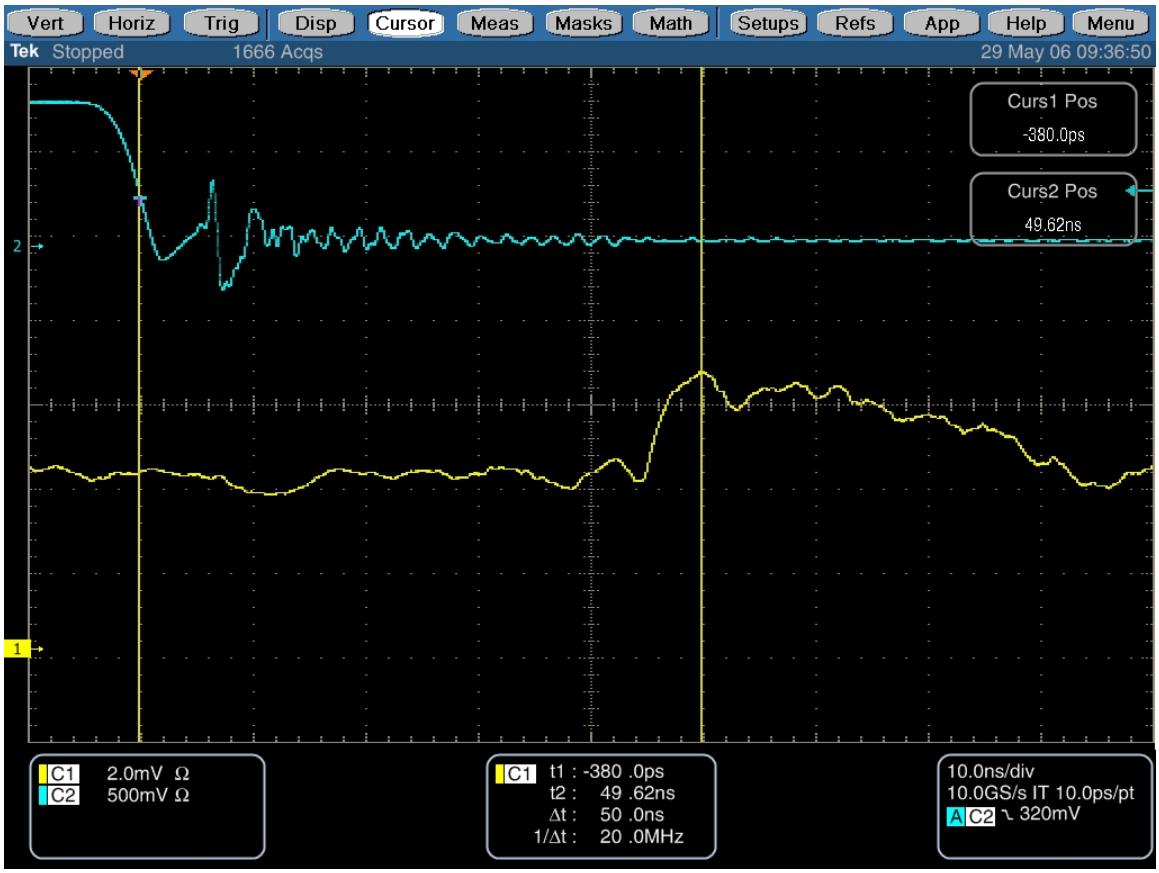


Figure 20: Laser trigger (upper) and Picoprobe35/electrode response (lower) versus time. With the laser spot at 30 μm from the electrode, the time from the reference signal to the peak of the output pulse is 50nS.

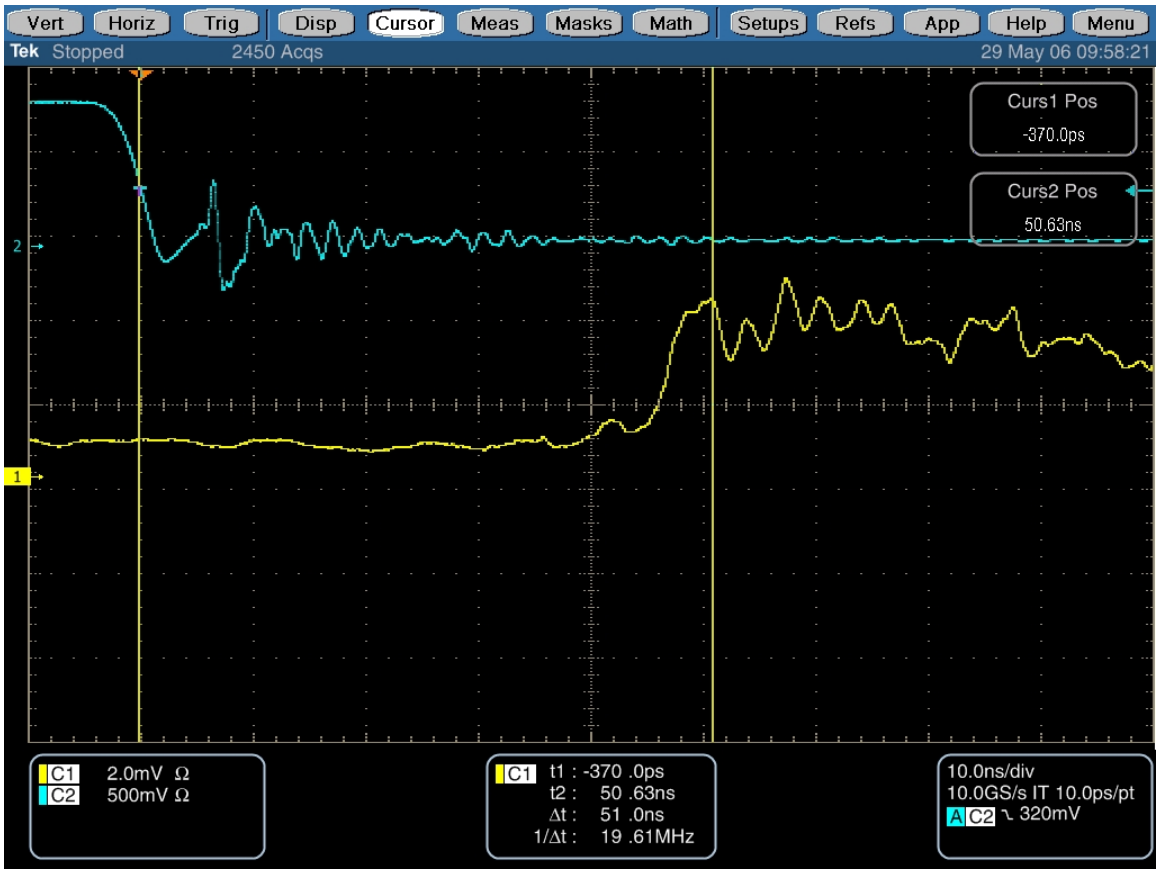


Figure 21: Laser trigger (upper) and Picoprobe35/electrode response (lower). With the laser spot at 90 μm from the electrode, the time from the reference signal to the peak of the output pulse is 51nS.

Plans, 17 June 2006 – 30 September 2006

In the remaining 3 months of this funding cycle, we expect to complete the following:

1) Repeat the direct measurements of capture time and capacitance and the indirect measurement of capacitance and refine those measurements for all the irradiated 3D (1.8, 3.6, and 18 x 10^{14} 1-MeV n/cm^2) devices that we have in our lab. Estimate systematic uncertainties.
2) Repeat the laser measurements with a 670nm and a 980nm IR laser to assess systematics.
3) Implement the ISE TCAD device simulator from Synopsis, and initiate a device simulation to validate the position scan and charge collection measurements.
4) Allow the irradiated devices to warm (and anneal) in a controlled way and measure capture time as a function of effective annealing time.
5) Implement a ^{90}Sr / scintillator setup for timing measurements.
6) Receive the ATLAS-geometry 3D devices and repeat the characterization process.

Proposal for 1 October 2006 – 30 September 2007

1) Irradiate the ATLAS-geometry 3D sensors to $10^{15}/cm^2$ at the LBL 88" cyclotron and characterize them.
2) Implement a method for drift time measurements involving simultaneous measurement of p- and n-electrode signals.
3) Receive the next generation 3D devices, characterize them, irradiate (two to 5 x $10^{15}/cm^2$ and two to $10^{16}/cm^2$), and repeat the characterization.
4) Examine options for test beam measurements on irradiated devices as necessary. Operate irradiated 3D devices in a testbeam with the goal of selecting the baseline design for the ATLAS upgrade.
5) Work with collaborators to develop the production design.

Budget request

Budget Justification
The University of New Mexico requires salary for an engineer with extensive experience in silicon sensor studies. This proposal requests support for 0.7 FTE engineering. We request as well support for his travel to four domestic destinations (two ATLAS upgrade meetings and two collaborative meetings with the Parker group at SLAC) at $800 per trip and two international upgrade meetings at $2000 each. A request for $5000 for materials and services, including special fixtures, small tools, software, and postage, is included as well.

Budget

Item	Requested Funds
Electrical engineer salary (0.7 FTE)	$43,651
Fringe benefits (26.5%)	$11,567
Materials and services	$ 5,000
Travel	$ 7,200
Total Direct Costs	*$67,418*
Indirect Cost (26%)	$17,529
Total request for FY2007	**$84,947**

Status Report for ATLAS Upgrade R&D
WBS 4.1.1.2.1 Strip Technology
WBS 4.1.2.2 SiGe
WBS 4.1.3.3 Optical Fibers
WBS 4.1.4.2 Hybrids

David E. Dorfan, Alexander A. Grillo, Jason Nielsen,
Hartmut F.-W. Sadrozinski, Abraham Seiden

SCIPP, UC Santa Cruz, CA 95064

Summary of Project Goals:

- Identification of the optimum technology and layout of the tracking detectors for the upgraded ATLAS ID and construction of silicon detector (SSD) modules with sufficient radiation hardness for the intermediate and outer tracking region in the upgraded ATLAS ID.
- Evaluation of integrated circuit technologies for the readout of the upgraded ATLAS ID, in particular the evaluation of new SiGe biCMOS technologies and the design of a prototype readout IC.
- Work on enabling system issues, i.e. hybrids and optical fibers, as needed for the progress of the module work, and to identify suitable technologies for the upgrade.

1. Summary of FY 2006 R&D Plan and Results

FY2006 goals:

4.1.1.2.1 Strip Technology

Manufacturing of short-strip silicon strip detectors in the geometry appropriate for the intermediate region of the ATLAS upgrade ID
Build hybrids for short strip SSD
Construct single detector modules with fast low-noise readout.
Collaborate with international partners on developing, irradiating and characterizing test structures and prototype detectors and the design and fabrication of hybrids and readout DAQ.

Irradiate the detectors with fluences up to $3*10^{15}$ p/cm^2

4.1.2.2 Frontend ASIC

Sample test structure of several vendors of SiGe, among them IBM, IHP, in some cases with more than one of their generations.
Irradiate samples with neutrons, gammas and protons.

Update technology files to reflect post-rad parameters.
Design and fabricate a chip with a few channels of a front-end readout using one of the available technologies in order to advance our understanding of the true power savings beyond the level of calculated estimates.

4.1.3.3 Optical Fibers

Identify a limited number of rad-hard and standard fibers that would be appropriate for further testing.
Procure a limited number of samples and prepare for testing.
Measure sample attenuation and recovery as a function of wavelength before and after irradiation with gammas, neutrons and pions.
Due to late arrival of funds, this work could not be started until summer-06 and will be completed during FY07.

4.1.4.2 Hybrids

Build hybrid for short strip detectors characterization.

Milestones for FY '06

	Original	Cmplt/Frcst
Layout of short-strip SSD	10/1/2005	3/1/2006
Layout of short SSD hybrid	3/1/2006	6/1/2006
Short strip SSD fab'd	6/1/2006	9/1/2006
Short SSD hybrid fab'd	6/1/2006	9/1/2006
Efficiency measurements on short strip SSD	10/1/2006	ongoing
Layout of SiGe proof-of-principle IC	12/1/2005	4/13/2006
Layout of test board for SiGe proof-of-principle IC	2/1/2006	7/14/2006
SiGe test structures characterized from multiple vendors	3/1/2006	5/15/2006
SiGe proof-of-principle IC fabricated	4/1/2006	7/28/2006
SiGe test board fab'd	4/1/2006	8/15/2006
SiGe test structures irradiated from multiple vendors	7/1/2006	8/1/2006
SiGe proof-of-principle IC characterized	10/1/2006	10/1/2006
SiGe technology files updated for at least one process	10/1/2006	10/1/2006

The milestones have been met or there is good progress to meet them during this year.

2. Detailed Results for FY2006

2.1. WBS 4.1.1.2.1 Strip Technology

The R&D efforts in the last years have identified silicon strip detectors (SSD) as the tracking medium of choice for the LHC upgrade. Lessons learned from the development program of the ATLAS SCT indicate that using SSD based on the same technology as in the SCT would require prohibitive operating costs in terms of cooling and services like high bias voltage. Thus, the emphasis of current R&D into the LHC upgrade SSD is to find new silicon substrates which might result in lower depletion voltages and do not

invert, i.e. allow operation below depletion with modest bias voltages. A very promising option is to use n-on-p detectors (instead of p-on-n) on Magnetic Czochralski (MCz) wafers (instead of Float Zone (FZ)), where the p-type bulk assures that there is no type inversion, and the high oxygen content of MCz results in lower depletion voltage after radiation [1].

The time scale for the LHC upgrade is extremely short, requiring working SSD by 2009 so that one can then start a pre-production program. In addition, the manufacturing costs for SSD are high. To overcome both obstacles, we have worked on assembling an international collaboration of universities, laboratories and manufacturers for the development of p-type detectors. This involved organizing two workshops dedicated to p-type substrates (Trento 2005 [2] and 2006 [3]), organizing a fabrication run of SSD and test structures in a commercial process [4] and submitting an R&D proposal on p-type SSD [5] to the ATLAS Upgrade Steering Group [6] for advice and consent. This proposal is signed by essentially all institutions which have contributed to the SCT, ensuring a broadly based R&D program.

In anticipation of technical suitability of the p-type SSD, we have investigated the parameters for the operation of these novel SSD at the LHC upgrade. Expected performance in signal-to-noise ratio, and the system requirements of cooling and readout speed have been discussed in Ref [7].

2.1.1. Layout and submission of SSD fabrication run

Fabrication of p-type detectors for the LHC upgrade is just beginning. Much of the effort has been done by non-commercial institutes with wafer processing capability. It is important to understand which results are generic to the p-type wafers and which might be specific to the manufacturing facility. Thus it is important to fabricate SSD with commercial manufacturers. We have submitted an order to Micron Semiconductors Ltd. for production of 6” wafers with a layout of a variety of strip detectors and test structures which will enable us to understand better the processing of p-type SSD. A wafer map of the different designs is shown in Fig. 2.2, indicating the large amount of test SSD available in the near future.

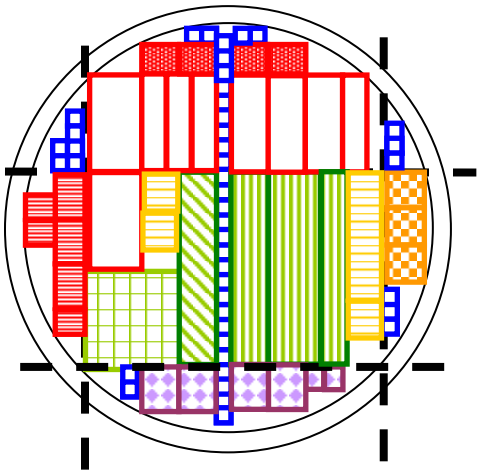


Fig. 2.1 Evolution Wafer map of the SSD submission to Micron

The submission is supported by many institutions, e.g. BNL from the US-ATLAS collaboration. The type and number of wafers to be processed are indicated in Table 2.1. One technical detail is the strip isolation. We decided, based on last year's findings [2], to use a combined p-stop/p-spray approach.

Table 2.1 Wafer Type and Number and Structures for the Micron SSD Submission

Substrate Type	Orientation	Silicon	Ohm-cm	Thickness (μm)	No. Of wafers	Structure
P-Type	<100>	FZ	11000	300	36	N – P
P-Type	<100>	MCZ	1000	300	25	N – P
N-Type	<100>	MCZ	500	300	20	P – N
N - Type	<100>	FZ	3000	300	5	P – N
N - Type	<100>	MCZ	500	300	5	N – N
N - Type	<100>	FZ	3000	300	5	N - N

2.1.2. Test of alternative short strip structures: 2D

One novel idea concerning the geometry of SSD is so-called 2D detectors [8] which permit the readout of two coordinates using single-sided processing. They would replace conventional double-sided SSDs, which are not radiation tolerant. One potential draw-back is the increased parasitic capacitance of the 2D detectors, in part due to many crossing traces, in part due to very closely spaced traces. We have tested the interstrip capacitance of both 2D test structures and a full-size short-strip 2D SSD supplied by BNL.

Fig. 2.2 shows the bias dependence of the interstrip capacitance for a detector of 2.6 cm length. Since much of the parasitic capacitance is to the crossing strips, and only ¼ of the strips were bonded out, we predict a total capacitance of 15 pF/cm once the full detector

is bonded out. This is about a factor 10 larger than in ordinary SSD, and if confirmed, will make this technology unsuitable for the ATLAS upgrade.

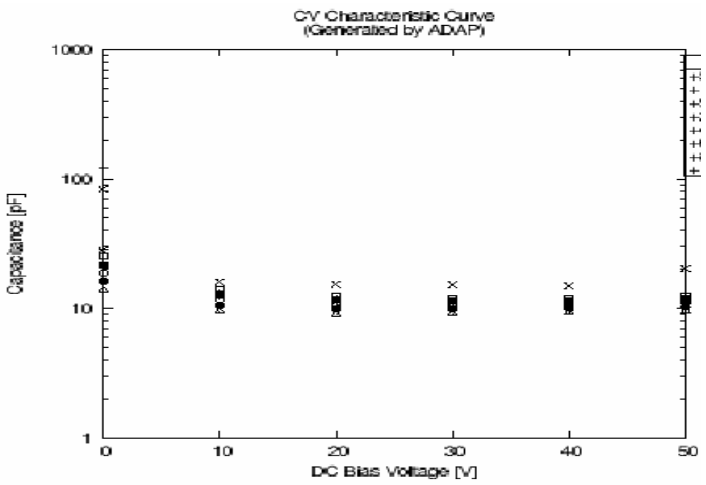


Fig. 2.2 Interstrip capacitance for a 2.6cm long 2D detector at various frequencies from 1 kHz to 1 MHz. Only ¼ of the strips are bonded out, meaning that the measured capacitance needs to be scaled up by 4 to calculate the full interstrip capacitance.

2.1.3. TID Testing of MOS and SSD test structures

We have teamed with the SMART collaboration (funded by INFN) to investigate the electrical performance of p-type short strip SSD and test structures after proton, neutron and gamma irradiation. Using our in-house ^{60}Co source, we have tested MOS transistors and interstrip capacitance test structures both pre-rad and post-rad to extract the saturation behavior of the oxide charge for different substrates (p-type FZ and MCz with both high- and low-dose p-spray, and n-type FZ). The data are shown in Fig. 2.3. Clear saturation is seen for all wafer types. Since the irradiations were performed unbiased, a fairly large degree of annealing is observed, indicated by data points shown for the same dose. This data will be used by the manufacturer (ITC-irst) to understand and tune process parameters.

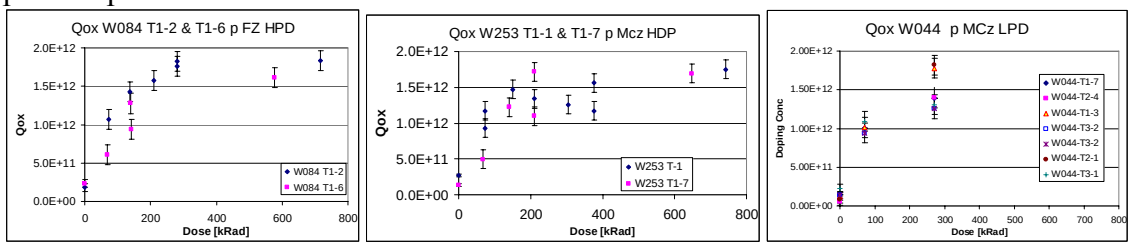


Fig. 2.3 Evolution of the oxide charge with total dose for different wafer and p-spray dose (FZ high. MCz high, MCz low)

2.1.4. Charge collection studies on p-type single-column 3D detectors

There is very little operating experience with p-type SSD. Among many different SSDs, we have investigated p-type 3D detectors with cell readout configured as strips [9]. Most

of the measurements have been electrical studies of detector parameters like leakage current, depletion voltage, and bulk and interstrip capacitance. It is one of the important parts of our program to establish charge collection benchmarks pre-and post-rad and correlate them with the electrical parameters. Our electron telescope using a ^{90}Sr source permits us to measure the charge collection efficiency (CCE), yielding information on depletion voltage (independent and more relevant to detector operation than electrical C-V) and trapping. Fig. 2.4 shows the collected charge from the 500 μm thick p-type 3D detector as a function of bias voltage. The depletion voltage is about 200 V. The rapid increase at low bias is due to the very fast depletion in between columns. This is the region where the 3D detector has un-depleted areas, which has very low efficiency. This is shown in Fig. 2.5. The body capacitance was measured at the same time, and the depleted region x and the expected charge was extracted (C ~ 1/x), which is shown in Fig. 2.4. The agreement is very good.

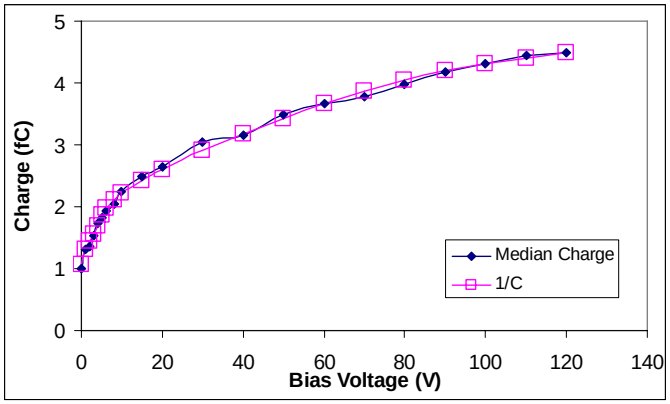


Fig. 2.4 Median charge as a function of bias voltage collected in the p-type single-column strip-like 3D detectors fabricated by ITC-irst, compared to

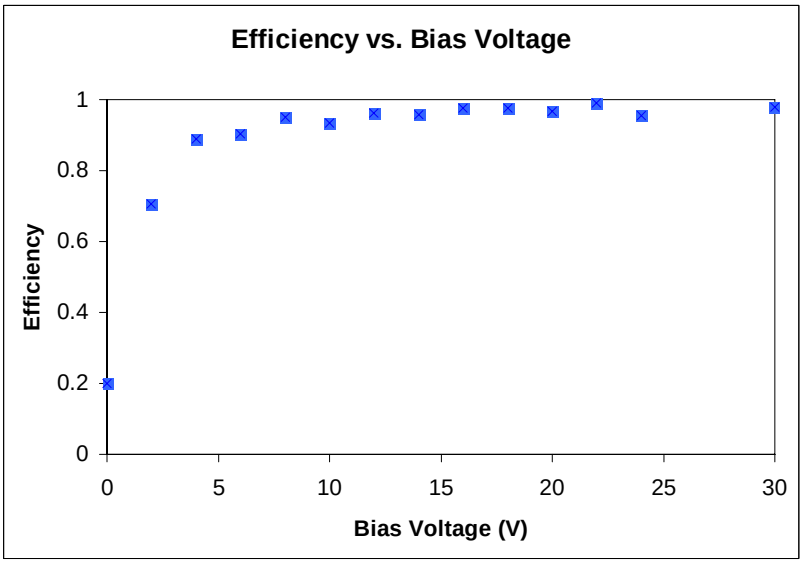


Fig. 2.5: Efficiency of charge collection as a function of bias voltage in the p-type single-column strip-like 3D detector fabricated by ITC-irst. The low efficiency at very low bias is due to the un-depleted regions in between columns.

2.2. WBS 4.1.2.2 Frontend ASIC

Last year we reported that test structures of one SiGe biCMOS technology were irradiated with protons to several fluences up to $1x10^{16}$ p/cm^2 and that reasonable electrical performance was measured after irradiation demonstrating that the SiGe bipolar devices can be quite radiation hard. This year test structures from three generations of IBM SiGe technologies have been tested and prepared for irradiation. Irradiations with neutrons and gammas have been performed. Proton irradiation is scheduled for July as soon as the CERN PS restarts. Preliminary post rad testing of the parts irradiated up to 10 Mrad of gammas indicates good operation. Post-rad neutron data has been delayed by problems with shipping but is expected to be completed in August along with the proton data. Our collaborators in Barcelona have performed similar tests on two technologies from the German company IHP also obtaining encouraging results. A prototype, proof-of-principle, front-end circuit was designed and submitted for fabrication. We expect it back from the foundry by the end of July.

2.2.1. Irradiation of Test Structures

We obtained test structures for three generations of IBM SiGe technologies (5HP, 7HP and 8HP). These were obtained from our collaborators at Georgia Tech. The arrays of test structures included at least eight different size transistors, resistors and capacitors. Sufficient devices were received for irradiations of gammas, neutrons and protons to at least five doses/fluences each.

To facilitate the electrical testing of such a large number of devices, new test cards and a semi-automatic test system were designed and assembled. See Figure 5. A new test card to hold each test structure array was designed. The wire test structure pads are wire bonded to metal traces that run to a micro-connector at the side of the card. This micro-connector can then be used to electrically connect the devices to either: (1) external test equipment through a connector card, (2) a small shorting connector which shorts all the pads together for safe transport or irradiation or (3) a small biasing card to bias the devices during irradiation. The test card then has no components except the test structure array and a minimal amount of metal. This minimizes the activation of the card during irradiation. For testing, the connector card connects through cables to a programmable switching matrix and then to the test instrument, either a parameter analyzer or an LCR meter. The switching matrix and the test instrument are under computer control so that the various measurements can be made automatically with results stored on the computer for analysis. This system, which replaced our manual operated probes, has shortened the test time by more than a factor of 10.

Figure 6 shows some of the pre-radiation test results along with one post-radiation curve from last year's proton irradiation. The 7HP and 8HP start out with significantly higher

DC current gain, which could afford better post-radiation performance if the degradation is no worse than in Fig. 6.

Figure 5: Test Structure Test Setup
Left photo shows connector card and small test card. Test card contains only test structure array and bondable leads to micro-connector.
Right photo shows test system including probe station, parameter analyzer and switching matrix in foreground.

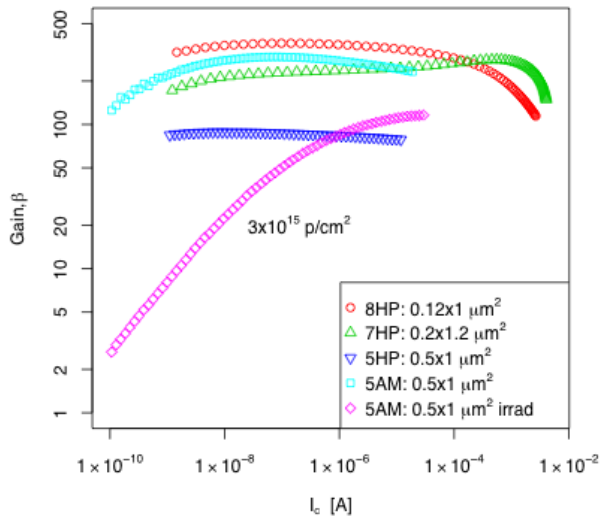


Figure 6: Pre-radiation data for three IBM technologies (5HP, 7HP, 8HP) along with pre- and post-radiation data from 2004 (5AM).

One set of parts were irradiated with neutrons by our collaborators at Ljubljana in January. Unfortunately, because of new regulations and bureaucracy instituted in Slovenia since our last neutron irradiations there, we discovered that the company previously used to ship parts back to us will no longer handle irradiated material. We have been struggling since February to find a new shipper to handle this material. It

appears that we have now found a solution and hope to have the parts returned for testing by the end of July, but at this time we do not have any post-irradiation data for neutrons.

The irradiation with gammas was initiated at BNL in May with the help of our BNL-LAr collaborators. At this time, the irradiations are still taking place, but we have some preliminary data which is discussed in the next section. The parts for proton irradiation are at CERN awaiting the re-start of the PS. This is now expected to take place at the beginning of July so we should have post-irradiation results with protons in possibly September.

2.2.2. *Irradiation Test Results*

Preliminary results for gamma irradiation of the 8HP technology are shown in Figure 7. This plot shows the DC current gain (β) as a function of collector current bias for various doses up to 100 Mrad. The current gain at a very low bias current of 1 μA is still above 50 (our typical minimum operating value for reasonable circuit design) even though this transistor has a large area. The smaller transistors planned for use in most of the front-end circuit will have an area approximate ¼ this size and thus x4 the current density at the same bias current. Given our past results with other bipolar technologies and the 5AM SiGe technology last year, that radiation damage scales with current density not current, we would expect the performance of the smaller transistors to be comparable to about 4 mA on this plot, i.e. β~100. The larger transistor shown in the Figure 7 is approximately what one would use for the front transistor, i.e. first stage amplifier, and would normally be biased at about 150 mA. (See next section on circuit design.) At such a bias, there is little of no radiation damage evident.

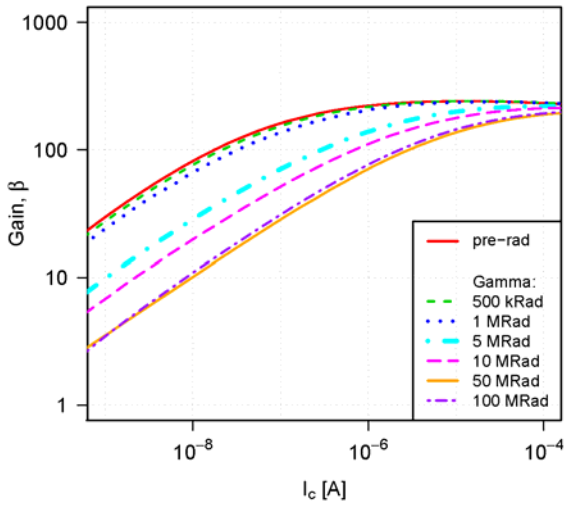


Figure 7: DC Current gain (β) for one large 8HP transistor (0.12x4.0 μm^2) for several total ionization doses up to 100 Mrad.

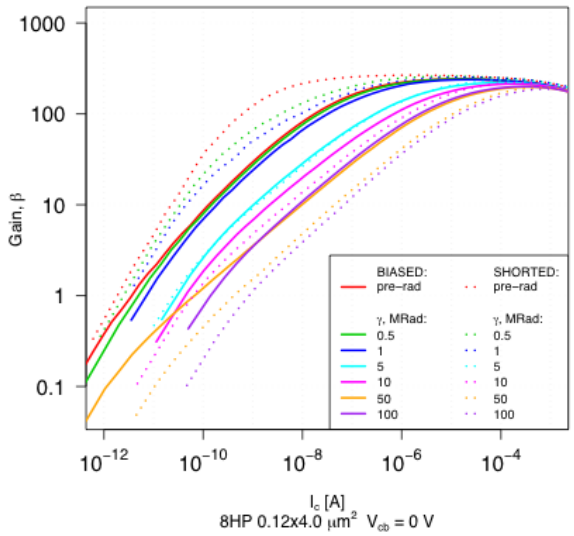


Figure 8: DC Current gain (β) comparison for biased vs. shorted leads during irradiation for one 8HP transistor (0.12x4.0 μm^2) at several total ionization doses.

For the gamma irradiations, some devices were biased with typical operating bias currents while others were left with their terminals sorted together. While the shorted condition is much easier to effect depending upon the logistics of the radiation facility, it has been noted in previous studies that such condition creates worse damage. We repeated this biased vs. shorted condition for these tests to re-confirm this conclusion for the SiGe technologies. Figure 8 shows the results for this same sized 8HP device. The increased damage of the shorted case is confirmed. Note then that the proton irradiations reported last year (See Figure 6 for an example.) were done in the shorted condition and can be expected to be worse than a comparable irradiation under bias. Since in the case of particle detectors, the exposure to irradiation occurs during operation, the less severe biased irradiation more closely tests normal use of the technology. The proton irradiation scheduled for later this year will again be split between biased and unbiased devices.

These are only preliminary results as the gamma irradiation is still on going with more device sizes and the remainder of the IBM technologies. Also, we need to test the devices irradiated with neutrons and repeat the proton irradiations on all the technologies. However, if displacement damage to the 8HP process (neutron and proton irradiation) does not show some striking and unexpected problem beyond what we say with the 5AM technology last year, the 8HP technology looks very much like it will meet ATLAS requirements for the upgraded Inner Detector at the mid and outer radii.

2.2.3. Demonstration IC

A demonstration IC was designed in the IHP SG25H1 technology and submitted for fabrication in April. This IHP technology is one whose radiation hardness is being evaluated by our collaborators in Barcelona. It was chosen over one of the IBM technologies for cost reasons. Our access to this technology through Europractice is, for the time being, much less expensive than our access to the IBM technologies through the US MOSIS or other programs. The IHP technology chosen is representative of the others

in terms of electrical performance. Since the primary goal of this demonstration IC is to provide a concrete example of the power savings vs. noise and timing of the SiGe technologies compared to deep submicron CMOS, this low cost option is most prudent until the number of possible SiGe technologies is shortened to a few for radiation hardness, cost or other considerations.

The design of this 8-channel IC has been optimized for low power and low noise while operating with short strips at a planned $\geq$ 20 cm radius and long strips at a planned $\geq$ 50 cm radius. Figure 9 shows the SPICE simulations of noise for these two running conditions. One can see that the noise requirements ($\leq$ 1500 e^- pre-irradiated) can be met for a ~ 6 pF load at ~ 40 mA front transistor bias and a ~ 15 pF load at ~ 150 mA bias.

The SPICE simulation of power consumption is tabulated in Figure 10. The total power for the analogue section of 360 μW/channel is about a 70% reduction over what has been achieved with a comparable CMOS front-end circuit. It remains, of course, to demonstrate that the fabricated silicon IC produces the same power savings as the SPICE simulations indicate. We expect silicon samples to be back from the foundry for testing by the end of July.

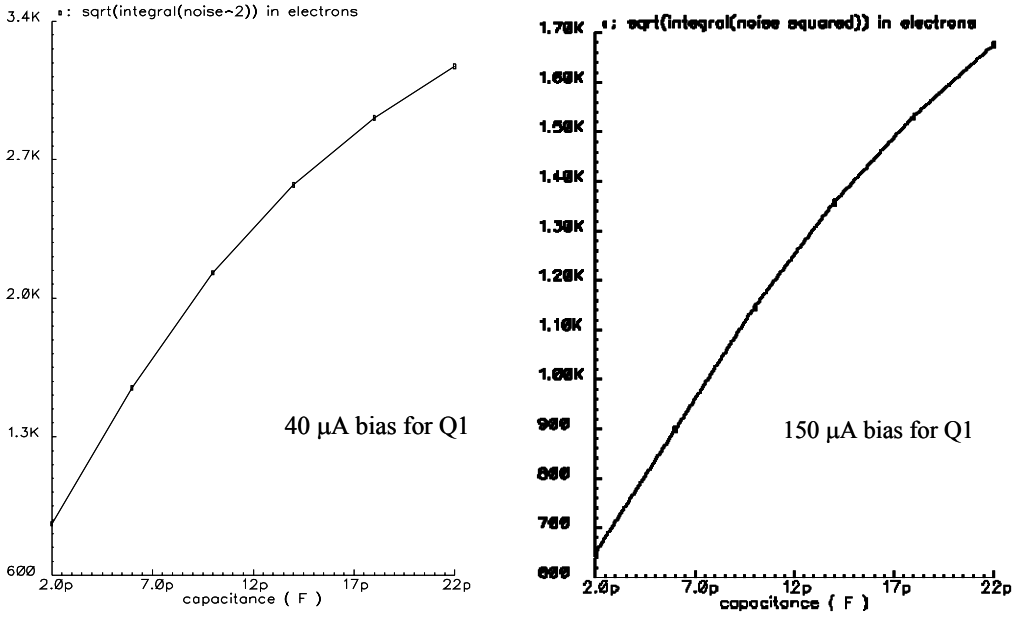


Figure 9: SPICE Simulations of Noise vs. Input Load Capacitance
Noise for short strips (estimate ~ 6pF) shown at 40 μA front transistor bias.
Noise for long strips (estimate ~ 15 pF) shown at 150 μA front transistor bias.

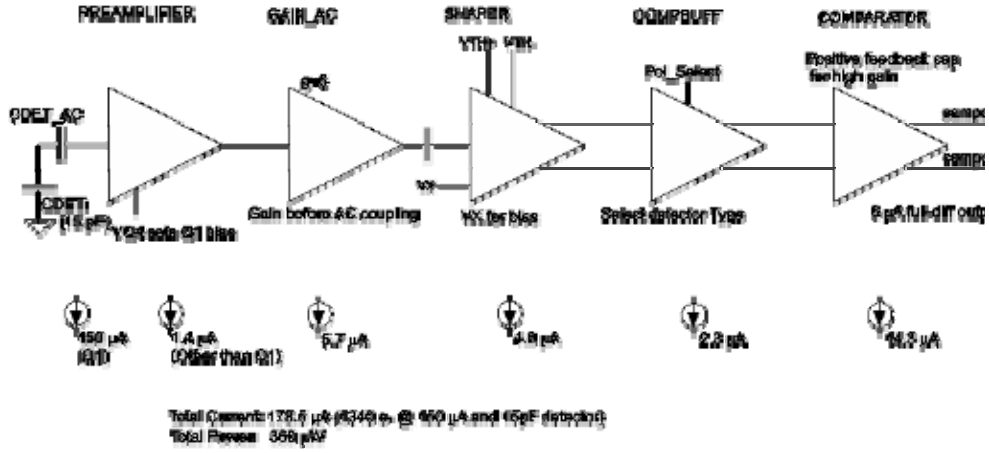


Figure 10: Block Diagram of Demonstration IC.
Bias values for each block are shown beneath as results from SPICE simulations.

2.3. WBS 4.1.3.3 Fibers

Funds for this activity only arrived in June of this year. Therefore, no work has yet been completed. The radiation hardness of single mode and multi-mode fibers from several vendors, as proposed for this year will be carried out starting this summer now that funds have been made available.

2.4. WBS 4.1.4.2 Hybrids

New hybrids were assembled to be used with PMFE frontend amplifier-shaper-comparator ASIC with 100ns shaping time, which allows readout of both positive (hole) and negative (electron) signals. The test structures and SSD without AC coupling were assembled with RC chips to eliminate the direct detector current. Marked differences in charge collection efficiency were observed when compared with pad detectors with 2 μsec shaping time. The work to convert the SCT hybrid to permit reliable readout of negative pulses, the main goal of this exercise, is on going.

3. R&D Plan for FY 2007

WBS 4.1.1.2.1 Strip Technology
WBS 4.1.2.2 SiGe
WBS 4.1.3.3 Fibers
WBS 4.1.4.2 Hybrids

3.1. WBS 4.1.1.2.1 Strip Technology

There will be a large number of SSD and test structures available for testing from the manufacturing run at Micron. First will come parametric electrical testing, followed by charge collection studies to establish pre-rad signal-to-noise benchmarks. We will perform irradiations with protons (CERN), gammas (BNL) and neutrons (Ljubljana) and

repeat the characterization post-rad. The main issues will be depletion voltage and trapping as a function of fluence, and the noise due to excessive interstrip capacitance and leakage current. In addition, for p-type detectors, the robustness of the inter-strip isolation and the headroom in breakdown voltage is important.

A few of the detectors will be "paired" SSD to allow readout by a common hybrid straddling the sensors. We will investigate how we can best integrate them with the SiGe prototype ASICs (see below).

The lessons learned in the detector program will be applied to new designs. We will learn if our design of a combined p-stop/p-spray isolation is sufficiently efficient and robust so that it can be the baseline for LHC upgrade detectors. Another issue is the question of whether n-type MCz detectors invert.

3.2. WBS 4.1.2.2 SiGe

In the remainder of this year, we plan to complete the total dose/total fluence tests of the three IBM technologies while Barcelona completes the same for the IHP technologies. As reviewed above, the parts are now being irradiated with gammas, the neutron irradiation is complete awaiting return of parts to Santa Cruz in July for post-rad testing and the proton irradiation is scheduled for completion this July barring any problems with the PS at CERN. Once this work is completed, we plan to reduce the number of technologies to possibly two for further study. This selection will be based upon the results of our radiation studies to select the technologies most likely to meet ATLAS requirements.

CERN is also in the process of negotiating a Frame Contract for foundry service for a 130 nm CMOS technology. The tendering process lists SiGe as an option for the supplying foundry. If a Frame Contract is signed which includes a SiGe option, this may influence our selection of technologies for further study.

These further studies will include tests for "low dose rate effects" (LDRE) which have been observed in some but not all bipolar processes. This LDRE results in larger damage to bipolar devices if the dose rate is very low. We conducted such an LDRE study prior to accepting the technology for the present SCT. It requires conducting irradiation tests at several different dose rates in such a way that dose rate effects can be measured for the same total ionization dose (TID). The past study took in excess of one year but we may be able to shorten that time given our familiarity with the protocol.

For these follow-on studies we plan to continue to collaborate with other ATLAS institutions. In particular M. Ullán from Barcelona developed a very comprehensive LDRE study when he was a post-doctoral fellow at SCIPP several years ago. His experience will be very valuable in this second-year work. We will also continue our collaboration with J. Cressler's group from Georgia Tech. Cressler is an expert in SiGe technologies and has been very helpful with our past work including providing us with the IBM test structures used in our studies.

We will also want to study any anomalies which may manifest themselves in the remaining work this year with total dose/total fluence studies.

As for circuit design, we will be able to complete pre-radiation testing of the demonstration chip we expect back from the foundry in late July. Once that is completed, we plan to do some irradiations of a sample of these ICs to correlate post-rad circuit performance with the post-rad electrical tests conducted by Barcelona on the same technology.

With successful completion of pre and post radiation testing of the demonstration IC and good agreement with SPICE simulation, we will choose one of the technologies chosen for follow-on radiation studies and begin the design of a full prototype front-end IC. This will not only further test our power savings goal but it will allow for more complete testing of subtle circuit design questions such as channel-to-channel matching, power bussing across a large chip and feedback between digital comparator firing and small signal input. The goal would be to have this IC ready for submission near the end of FY07.

3.3. WBS 4.1.3.3 Fibers

Given the late start on this work due to late arrival of funds, we plan to complete the previously approved work before we apply for more funds in this area. Future requests will depend upon the results of the present work.

3.4. WBS 4.1.4.2 Hybrids

Work will continue on adapting the SCT hybrids to the readout of the “paired” SSD. These are 6 cm long detectors electrically divided into two separate strips, which will be read out by a common hybrid. One option would be to use the SiGe test ASICs for readout.

FY 07 Milestones

WBS 4.1.1.2.1 Strip Technology

Pre-rad Electrical testing of Micron Detectors	3/1/2007
Pre-rad CCE of Micron Detectors	3/1/2007
Irradiation with neutrons	6/1/2007
Irradiation with gammas	6/1/2007
Irradiation with protons	8/1/2007
Post-rad Electrical testing of Micron Detectors	10/1/2007
Post-rad CCE of Micron Detectors	10/1/2007

WBS 4.1.2.2 SiGe

Complete total dose/total fluence studies	11/30/2006
Down select two technologies for further radiation study	12/31/2006
Establish plan for LDRE study	12/31/2006
Complete LDRE study	9/30/2007
Radiation test demonstration IC	12/31/2006
Begin design of full prototype front-end IC	4/1/2007
Submit full prototype front-end IC for fabrication	9/30/2007

WBS 4.1.3.3 Fibers

WBS 4.1.4.2 Hybrids

Readout of negative pulses with SCT DAQ	12/31/2006

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5. FY 2007 Budget

	UCSC FY 2007			
WBS	**Activity**	**Labor ($k)**	**M+S ($k)**	**Total (k$)**
4.1.1.2.1	**SSD Technology**			
	Short strip SSD Module			
	SSD Samples		5.000	5.000
	Pre rad Electrical Characterization	9.688		9.688
	Assembly	4.449		4.449
	DAQ	14.862	0.000	14.862
	Pre-rad Efficiency Measurements	9.688	0.000	9.688
	Irradiations			0.000
	Post-rad Electrical Characterization	2.775		2.775
	Post-rad Efficiency Measurements	9.120		9.120
4.1.2.2	**FEE**			
	Technology Qualification			
	Test development and analysis	34.369		34.369
	Electrical Characterization	10.348		10.348
	Technical Support	14.121		14.121
	Irradiation PCBs		2.500	2.500
	Georgia Tech sub-contract		20.000	20.000
	ASIC			
	ASIC design	0.000		0.000
	ASIC simulation	5.174		5.174
	ASIC layout	8.826		8.826
	ASIC fab		0.000	0.000
	ASIC test	11.768		11.768
	ASIC test board			
	Design and layout	5.670		5.670
	Fab		1.800	1.800
	Parts		2.200	2.200
	Test	4.012		4.012
	Assembly	4.886		4.886
4.1.4.2	**Short strip Hybrids**			
	Design and layout	22.833		22.833
	Fab		1.800	1.800
	Parts		2.003	2.003
	Test	28.090		28.090
	Assembly	4.814		4.814
	Total Labor and M+S	**205.491**	**35.303**	**240.794**
	Travel			
	Domestic travel		4.000	**4.000**
	Foreign Travel		6.000	**6.000**
	Equipment			**0.000**
	Total direct			**250.794**
	Indirect 26%			**65.206**
	Total FY2007			**316.000**

6. Manpower

David Dorfan	Physicist	ASIC technology and design
Alex Grillo	Physicist	ASIC coordination & evaluation, system
Jason Nielsen	Physicist	ASIC evaluation, system
Hartmut Sadrozinski	Physicist	SSD coordination & evaluation
Abraham Seiden	Physicist	Physics, layout, rates, system
Vitaliy Fadeyev	Physicist	Test development, elect. measurements
Ned Spencer	EE Eng.	ASIC design and layout, system aspects
Sergei Kashiguine	EE Eng.	Hybrid layout, elect. measurements
Max Wilder	EE Tech.	Interfaces, hybrids, characterization
Maureen Petterson	E.E. Tech.	Efficiency measurements
Jason Feldt	E.E. Tech	DAQ
Kunal Arya	u.g. student	DAQ
Alek Polyakov	u.g. student	Efficiency measurements
Chris Betancourt	u.g student	Efficiency measurements
Jed Pixley	u.g student	Electrical characterization
Rob Heffern	u.g student	Electrical characterization
Ashley Jones	u.g student	ASIC characterizations
Dominic Lucia	u.g. student	ASIC characterizations
Paul Mekhedjian	u.g. student	ASIC characterizations

WBS 4.1.1.3.2

Short Strip Development FY06/07

1. FY06 Plans and progress

A. Finish VA1' evaluation Result: Finished

The evaluation of the two candidate readout chips (the VA2TA and the VA1' from IDEAS, Norway) was completed in August 2005. The VA2TA was selected on the basis of better noise performance as well as its self-triggering capability. A quantity of 100 die was ordered to cover all future testing.

B. Finish building test station Result: 3/4 Finished

The stripixel test station envisioned the design and fabrication of four types of boards to completely characterize stripixel (or any type of strip) detectors. The boards are;

- Detector motherboard
- Leakage current board
- Capacitance Board
- Viking readout board.

All boards except the Viking readout board have been designed and built over the last year. The Viking board is in its final stage of design. From its original conception, its design has been split into a "RC" board and what we now call the Viking board. The RC board provides AC coupling of the detector to the Viking board. In may be omitted in the test setup for testing of AC-coupled strip detectors. The RC board has been designed and fabricated. The Viking board is expected to be completed toward the end of July, 2006. It should be noted that a complete duplicate test station exists at INFN Milano.

We also mention that while the initial motherboards (total of 4) are being or have been fabricated at BNL, a commercial vendor is necessary to produce a larger quantity. INFN Milano has been actively pursuing a suitable vendor.

An automated LabView based system that interfaces to the test station and permits monitoring of individual channel leakage current was developed by a student from Milano at BNL and now exists at both locations.

C. Test stripixel submission A Result: testing begun but now delayed

Submission A was the p-type stripixel fabricated with the same geometric layout as the original n-type prototype. Leakage current and capacitance measurements were begun on

the prototype stripixel with the test station. However, it was soon discovered that the prototype detector had abnormally low interstrip resistance making measurements unreliable. We therefore instituted a program of manually probing detectors on uncut wafers to pre-select detectors before mounting. From the four wafers originally fabricated, we now have three detectors that passed our pre-selection criteria. One is currently being mounted and bonded in Italy, with a second one to be bonded at BNL on a redesigned and improved motherboard.

UC Santa Cruz has also measured the capacitance of submission A. They measured a very large value for the interstrip capacitance, one that exceeds simulations by a factor of 3. However, all non-used strips were not grounded and the results are somewhat difficult to interpret. We believe testing on the full scale test station is required.

D. Submit stripixel submission B Result: submitted as planned

The original plan for submission B is below.

Submission B designed and submitted	*04/06*
Submission B received, testing begins	*10/06*
Submission B testing concluded	*02/07*

Submission B was a design intended to test various stripixel geometries. It was decided to submit this design through RD50. A design featuring 8 different pixel structures and sized to mate with the existing motherboard was completed in January 06. The RD50 submission is expected later this calendar year.

E. Other progress

Simulation

2-D simulations of total strip capacitance were performed for a variety of stripixel gaps and line widths. Results suggest that total strip capacitance may be reduced to on the order of 10pF for 3 cm long strips provided an effective x/y strip pitch of 20 um (currently 8 um in submission A and the prototype) can be tolerated. Here the large Lorentz angle of about 17 degrees expected for electrons in the 2 Tesla Atlas field may provide sufficient charge sharing but needs study.

Commercialization

Hamamatsu is currently making stripixels for the Phoenix experiment at RHIC and could be expected to be a future supplier of stripixels should the concept prove viable.

2. FY07 plan

Fully functional test stations are slated to exist at both BNL and Milano by the end of FY06. It is envisioned that a number of detectors from all three submissions (prototype,

A, and B) will be fully tested. Definitive conclusions are expected in particular from the B (RD50) submission that should determine the viability of the stripixel option.

NYU has begun and will set up an x-y stage fine-focus laser injection system that will permit us to make charge sharing studies on the stripixel detectors. These will complement studies that we intend to make with a radioactive source using the VA2TA self-triggering feature.

Additionally, we will make source-based charge sharing measurements in an adjustable 0.8 T magnetic field that is available at Brookhaven. It is expected that the stripixel design may advantageously utilize the large electron-drift Lorentz angle to maintain intra-pixel charge sharing while reducing input capacitance.

Some of the detectors will be irradiated with different sources at various locations including the BNL Solid State Gamma-ray Irradiation facility. Information on the radiation hardness of the p versus n-type stripixels should prove of interest to a more general audience.

We do not at this time expect the need for a further stripixel submission until the present set of detectors are fully characterized and modeled so that a definitive answer on the viability of a stripixel in an Atlas application is obtained. We will conclude the program of testing the stripixel submissions in Fy07.

We envision that the infrastructure we have developed for the stripixel program will evolve into a complete teststation for silicon detectors. We will continue with a full program of short strip testing, characterization, and irradiation studies as detectors become available through our collaboration with other efforts.

3. FY07 budget requests

BNL

item	**Materials**	**Labor**
Short strip(SS) motherboards	$10,000	
SS motherboard layout		$5,000
Irradiation fixtures	$5,000	
1/3 Elec/Rad test tech		$30,000
Total	**$50,000**	

NYU

item	**Materials**	**Labor**
T&M equipment	$7,000	
Travel	$3,000	
1/3 technician		$25,000
Total	**$35,000**	

5. Manpower

Institution	Personnel	Type	FTE
BNL:			
	Z. Li	Engineer	.10
	D. Lissaaur	Physicist	.05
	D. Lynn	Physicist	.20
University of California Santa Cruz:			
	H. Sadrozinski & undergrad	Physicist	.05
Hampton University			
	O.K. Baker*	Physicist	
	K.W. McFarlane	Physicist	
New York University			
	Chris Musso	Technician	.8
	Peter Nemethy	Physicist	.2
	Allen Mincer	Physicist	.1
INFN Milano (non US collaborator):			
	M. Citterio	Engineer	.3
	G. Alimonti	Physicist	.3
	M. Taccola	Student	.3

*Relocating to Yale University in FY07

WBS 4.1.2.1
FY07 LBNL ATLAS Pixel Upgrade Proposal

(Deep Sub-micron for Pixels)

LBNL has hired Abder Mekkaoui *specifically* to work on this project. Abder is an experienced analog designer with pixel expertise, having previously worked on the FPIX chip at Fermilab. His hire follows a long search period started after the design team that produced the present ATLAS pixel chip left LBNL. Both the present ATLAS pixel chip and the FPIX chip are implemented in 0.25 micron CMOS technology. The change to 0.13 micron technology is needed for integration density and digital speed at fixed power as much as for increased radiation hardness. However, this change makes several analog design elements more difficult. Work to be done is as follows: Task 1: given the potential weaknesses of the current analog design (where 0.25 um technology was pushed to the limit) understand the broad design changes that are essential to transition to 0.13 micron. Task 2: with task 1 and a previous 0.13 um test chip, envisage an architecture suitable for 0.13 micron as well as possible higher speed operation. Task 3: With tasks 1 and 2, determine the development program for the next-generation pixel chip. The submission cost is based on a modest test chip fabricated through the new 0.13 micron prototyping frame contract at CERN, which is still its start-up phase, but should be accessible on the time scale needed for this project. It should be noted that this level of effort is still well below what is needed for a full chip engineering run. Other fabrication avenues such as MOSIS would be more expensive even for this modest chip and are therefore discounted.

	Upgrade R&D Labor	Upgrade R&D M&S	Base Labor	Base M&S
A. Mekkaoui	200	0	50	10
Tools/license support	0	0	0	20
Submission	0	50	0	0
Test board fab	4	4	0	0

The FE-I3 readout chip now being used to build the present ATLAS pixel detector contains 3.5 million transistors in 0.25μm feature size CMOS technology and operates without significant degradation to ionizing doses of order 100MRad. The pixel size is 50μm x 400μm with approximately 1000 transistors per pixel, which are needed in order to implement low noise charge sensitive pulse amplification with automatic DC baseline subtraction, uniform threshold pulse discrimination, digital time stamping, and 8-bit time-over-threshold pulse height measurement [1]. While this chip comfortably meets all requirements for operation at LHC design luminosity, many features are not scalable and a hit rate increase of an order of magnitude or more would necessitate fundamental redesign of many circuits and possibly the overall architecture.

In FE-I3 the pixel is filled with circuitry. Either adding functionality to cope with higher rate, or reducing the pixel size to lower the single pixel rate while keeping the same

functionality would require (1) migration to a smaller feature technology, or (2) a very laborious hand-optimization of the entire artwork to squeeze down the footprint. Independently of design considerations, experience dictates that, given the timescale of the sLHC, consumer electronics market forces will probably impose a migration to a finer feature technology. The planned B-layer upgrade a few years ahead of the sLHC could provide a unique opportunity to "field test" a real 0.13um device if one can be produced on time. Initial studies have therefore focused on exploring the next available CMOS technology, which has 0.13μm feature size. A test chip incorporating the FE-I3 analog front end design plus some digital registers was prototyped in this new technology by the FE-I3 final design team in 2004. Testing of this prototype has been the main activity in this area in the first half of 2006.

The 2004 prototype mentioned above has been characterized on the bench and the results compared to simulation. The most salient feature is the increased threshold dispersion relative to the 0.25μm FE-I3. This is not a great surprise but it is a key item that must be addressed in a new amplifier design and understanding it is very important. IN addition to these tests the chip has been irradiated at the LBNL 88" cyclotron both for total dose studies and for SEU studies, using both protons and ions. A talk has been submitted and accepted to Valencia 06 and the results will be presented there. These tests form a good basis to resume significant design activity, which is now possible thanks to the new hire mentioned. A plan for preliminary design work in the remainder of 2006 is outlined below:

1. Simulate 2004 test chip to understand single channel basic analog performance and try to do a reliable noise analysis. Attempt to understand/reproduce the threshold dispersion in simulation.
2. Find the Cadence design directories for FE-I3 submission and for 2004 0.13u test chip
3. Simulate 0.25um amplifier to reproduce threshold dispersion of present FE-I3 chip
4. Arrange CERN visit to plan design work for new 0.13um amplifier, coordinate with other efforts, and learn about CERN 0.13um frame contract to be used for submission.
5. Detailed specification for new amplifier should be produced ahead of this meeting.
6. Concentrate on new design upon return to LBNL. By the end of FY06 hope to explore:
    - techniques to reduce our sensitivity to matching and reduce threshold dispersion
    - different charge measurement techniques (TOT, peak-sense,...)
    - basic configurations (zero-crossing vs present design)

WBS 4.1.4.4(Powering Schemes)

A switched capacitor, divide by four charge pump DC-DC converter test chip was laid out in the Austria Microsystesm (AMS)0.35 HV process and submitted in February 2006.

It was received back in May and has been tested (mostly by R. Ely and students) using two circuit boards laid out by Sami Hynynen, a Finnish exchange student. The characteristics of the transistor switches have been measured and agree, for the most part, with the models provided by AMS. However the overall performance was poor do to excessive leakage of some switches during the charge transfer phase. This problem has been identified and significant design revisions are necessary to make a new version that might be integrated into the prototype silicon strip stave. P. Denes is doing this design (at no cost to the Upgrade).

A power supply that will give good performance on a stave needs a regulator as well as a DC-DC converter. Ultimately both circuits can be laid out on the same chip but in order to facilitate the design of the converter we intend to prototype the two circuits in two separate submissions. The plan is to layout an improved version of the 'divide by four' converter with the goal of a submission in November for arrival in about January '07 and to design and layout a separate chip containing a pulse width modulated regulator for submission in February . Testing will be done by Ely + students. A second iteration is in our plans and for this and for the regulator design we are requesting upgrade support for IC design such that a near final version would be ready towards the end of FY07 or early FY08. The upgrade request for testing is for test board layout and fabrication and commercial components. The PCB layout is needed for a mezzanine board to fit the prototype stave.

In addition to the above design activity we are planning to determine the radiation hardness of the AMS process by exposing the present chip to 55 Mev protons at the 88 inch cyclotron. If the schedule of the 88 inch cyclotron allows, this test will begin in September, 2006. No additional funds will be necessary for these tests.

	Upgrade R&D Labor	Upgrade R&D M&S	Base Labor	Base M&S
IC design	70	0	0	0
PCB layout	6	0	0	0
Submissions (2)	0	40	0	0
Testing	4	10	15	0

Overall Budget

The overall budget is given below, including projected base support.
Ideally the base support would be higher, but most of our technical base support is reserved for finishing pixels in FY07.

	Upgrade R&D Labor	Upgrade R&D M&S	Base Labor	Base M&S
TOTALS	284	104	65	30

	Upgrade	Base

4.1.2.1	258	80
4.1.4.4	130	15
GRAND TOTAL	388	95

WBS 4.1.4.4.2
FY07 Power Distribution Proposal

Power Distribution

It is clear that for the inner detector new power distribution schemes that provide power to staves (or modules) at higher voltages and lower currents are needed to limit power losses in the supply cables and reduce cable mass. The power schemes currently being considered to replace standard parallel powering (PP) are serial power (SP) and DC-DC conversion (DCP) at the point of load. These schemes are illustrated in Figure 1.

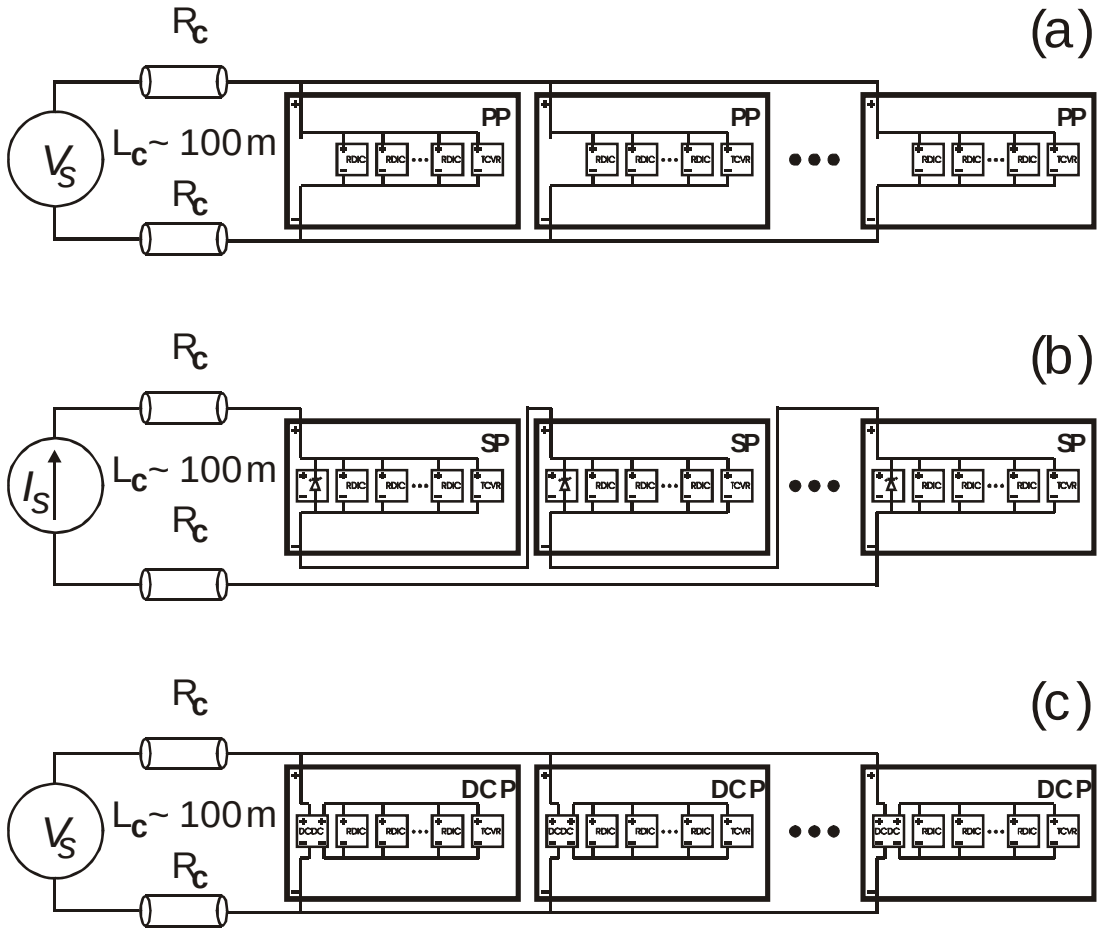


Figure 1. Electrical models of power connections of (a) Parallel/PP, (b) Serial Power/SP, and (c) DC-to DC/DCP staves.

Initial tests of serial powering have been very promising[1,2], although the concept remains unfamiliar to much of the silicon detector community. Many commercial DC-DC converter solutions have been developed for the telecommunications and other industries

that deliver high current and low voltages at the point of load. Both solutions show promise and difficulties for our application.

With either a serial or parallel solution, if multiple modules share the same voltages or currents, the vulnerability of a collection of modules to a single point failure is a crucial issue. To some extent, these are architectural questions, and to some extent are independent of architecture.

We have started to study both concepts from a system or architectural viewpoint, with emphasis on the following:

- Reliability

  For each topology we need to carefully consider how to isolate single point failures such as opens or shorts in the readout modules to prevent failure of the complete stave.

- Current/Voltage regulation

  While regulation of voltages or currents is implicit in each topology, there exist numerous variants of each. For example, it may be desirable to supplement the DC-DC converters with linear regulators to isolate the readout chips from the RF switching noise of the DC-DC converters.

- Noise and noise isolation

  Noise coupling is different in each architecture and needs to be understood. In the serial topology coupling between modules may be dominated by the shared current, while in the DC-DC converter scheme coupling may be dominated by the shared voltages. In addition, how the noise from an oscillating readout chip may best be isolated to prevent it from propagating through all the readout modules of a stave needs study.

- HV supply architecture

  Some consideration, particularly with the serial power topology, of how to bring high voltage (to the detector) and reference it properly to the readout modules is necessary. A traditional approach in a serial power configuration is shown in Figure 2a. This case requires multiple floating HV supplies. A possible alternative utilizing a single supply for multiple modules is shown in Figure 2b. In this approach not all detectors operate at the same voltage, but would be overdepleted by multiples of the shunt regulator voltage. However, some reduction in cable mass and simplification of HV power generation and distribution is obtained.

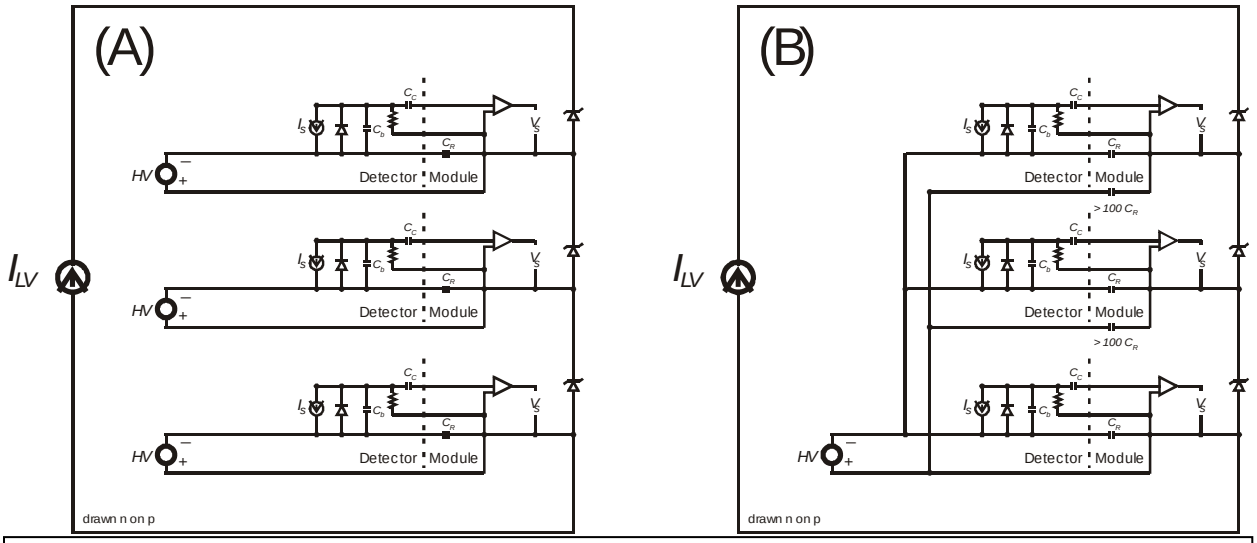


Figure 2. (A) conventional HV supply scheme; (B) minimal HV scheme with one supply per stave

We also have begun to look at a potential DC-DC conversion utilizing buck-boost conversion or variants thereof. The inner detector has a magnetic field of 2 Tesla. To work in such a strong field, the inductors in the buck converter topology must be nonmagnetic or air-core inductors. To keep the inductors small requires that the switching operate at frequencies above 1 MHz and possibly within the bandwidth of the readout preamplifiers. A number of multi-purpose test boards, each containing two ABCD chips will be available at BNL in mid July (Figure 3). Though the purpose of the board is primarily to assist in the new multi-module PXI based DAQ development, the board permits mounting of a daughter DC converter board to test noise response of the ABCD chip to various frequencies and architecture schemes under various front-end load capacitances. We plan to use this board initially as a test bed for various DC-DC architectures, and potentially for various shunt regulator architectures also. One final use for this board is to quantify the optimal ABCD response to electrons when utilizing the VTHN/VTHP pins.

We have started to perform a market search of existing shunt regulators, DC-DC converters, and high voltage FET switches for our studies and possible applications. We will perform radiation studies on selected devices at the BNL Solid State Gamma-ray Irradiation facility. Additionally, in collaboration with Yale[3] we are studying commercial examples of high frequency air-core DC-DC conversion for insight into possible variants of the simple buck converter configuration.

While we expect our level of activity on power distribution to significantly increase in FY07, we will be using part of our baseline support for this effort. We request from R&D funds the amount shown below, mostly to provide partial engineering support.

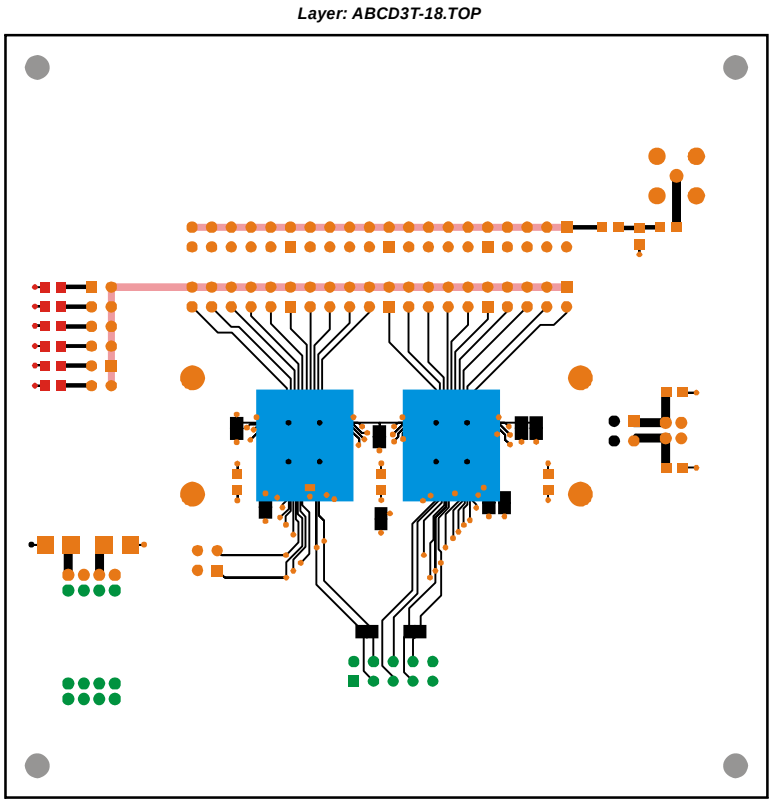


Figure 3. ABCD DAQ, Power, and Signal Polarity Testboard

BNL Personnel

Jim Kierstead, David Lynn, Don Makowiecki, Sergio Rescia

Collaborators

RAL	Marc Weber
LBNL	Carl Haber

Budget Request FY07

item		labor cost
1/4 Elect. Engineer		$50,000
Test Components		$5,000
Total		**$55,000**

References

[1] T. Stockmanns, P. Fischer, F. Hügging, I. Peric, Ö. Runolfsson, N. Wermes, **Serial powering of pixel modules**, Nucl. Instr. and Meth. A 511, 174-179 (2003).

[2] Marc Weber, Giulio Villani, Mika Lammentausta, **Serial powering for Silicon Strip Detectors at SLHC**, Proceedings of the 11th Workshop of Electronics for LHC and future Experiments.

[3] Satish Dhawan, private communications

FY07 System Design Proposal:

ID layout, Mechanical Integration, Barrel Support, Installation and Services Routing

Since we began preliminary studies on various inner detector layouts (e.g., projective vs. fixed length), a strawman baseline design has emerged, at least in the case of a stave (vs. modular) approach. This "fixed length" design features +/-2 meter long strip outer staves and +/- 1 meter inner short strip staves. Inside the strip barrels are two layers of pixels and an innermost "B" 3-d layer. We intend to further evolve this design by considering the interrelated issues of

- volume/routing of services
- coupling/independence of pixel and strips
- integration of barrels and disks
- assembly
- barrel support structure
- installation plan and ease of installation
- power and cooling
- moderator
- grounding schemes
- material budget

A coherent plan that addresses simultaneously these many facets at an early stage is desirable to further optimize the ID layout. This will require coordination with R&D groups devoted to these particular aspects. However, we have begun initial studies of some of these aspects and their impact on the layout. For example, using early estimates of stave power and allowable power loss in cables, as well as referencing cooling studies for the present SCT, a first sketch of the services volume supplying staves is shown in Figure 1. Diameters for the LV cables are shown for both 20% and 100% power loss (compared to total detector power) in 25 meters of low voltage cable for a typical power scheme, i.e. no serial power or DC-DC conversion. The conclusion is that local cable volume is manageable with any power distribution scheme. Figure 2 shows parts of our recent study of an assembly procedure for a fixed length geometry with integrated pixel.

We expect the fixed length strawman design to develop and change as work by the simulation group attempts to optimize the layout with regards to specific physics goals. We have positioned ourselves to study the mechanical aspects of such changes through modeling of the inner detector with CATIA. CATIA is a 3-D mechanical modeling package that we recently installed at BNL and is being adopted by Atlas. Atlas is currently in the process of converting their models from the obsolete Euclid software into CATIA.

As we are involved in a separate stave proposal, it's a natural extension to consider some mechanical aspects of the inner detector beyond modeling, specifically the design of the barrel support structure. We are currently developing finite element models in ANSYS to provide thermal and mechanical models of staves and the support structures. Figure 3 shows an initial simulation of a CDF style stave; understanding the requirements on stave kinematical supports will in part drive the barrel structure design, one example of which we show in Figure 4.

Figure 5 shows provides a comparison of the mounting scheme of Figure 4 to a Lorentz-angled rotated stave mounting. The un-rotated scheme leads to simpler kinematic supports as the radial and r-ϕ components are decoupled. However, input from detector and readout simulations are needed to determine whether it is a necessity to compensate for the larger Lorentz angle (~17º) expected for electron drift in p-type detectors.

One primary goal for the coming year is to have a complete 3-D model of one version of the inner detector. The model will include services, endcaps, and other major components so that the space and other constraints can be easily visualized and understood. Additionally, we will develop finite element analyses of barrel structures in an attempt to understood the stability-mass relationship. As the scope of this effort is large, we will be actively looking to collaborate with other institutions.

Manpower

BNL Personnel

Jason Farrel, Anatoli Gordeev, David Lissauer, David Lynn, Sue Norton, David Rahm Magareta Rehak, Yannis Semertzidis, John Sondericker

Collaborators

Rutherford Lab	Marc Weber
CERN	Steiner Stapnes, Andrew Catinaccio

Budget Request FY07

item		Materials	Labor
1/3 Designer			$39,000
1/3 Mechanical Engineer			$64,000
Design Tools		$4,000	
Total		**$107,000**	

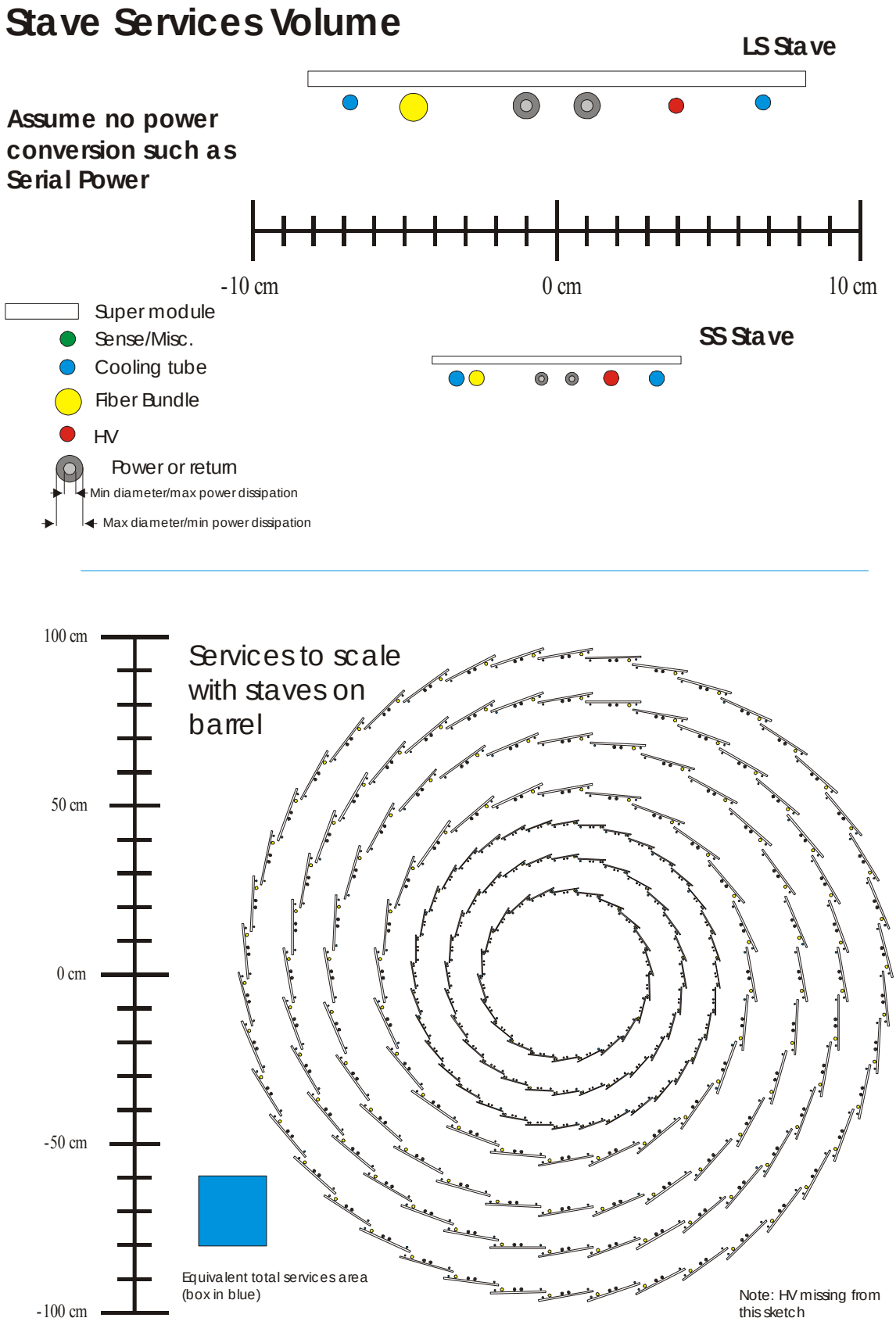


Figure 1. Stave Services Volume with Standard Powering Scheme

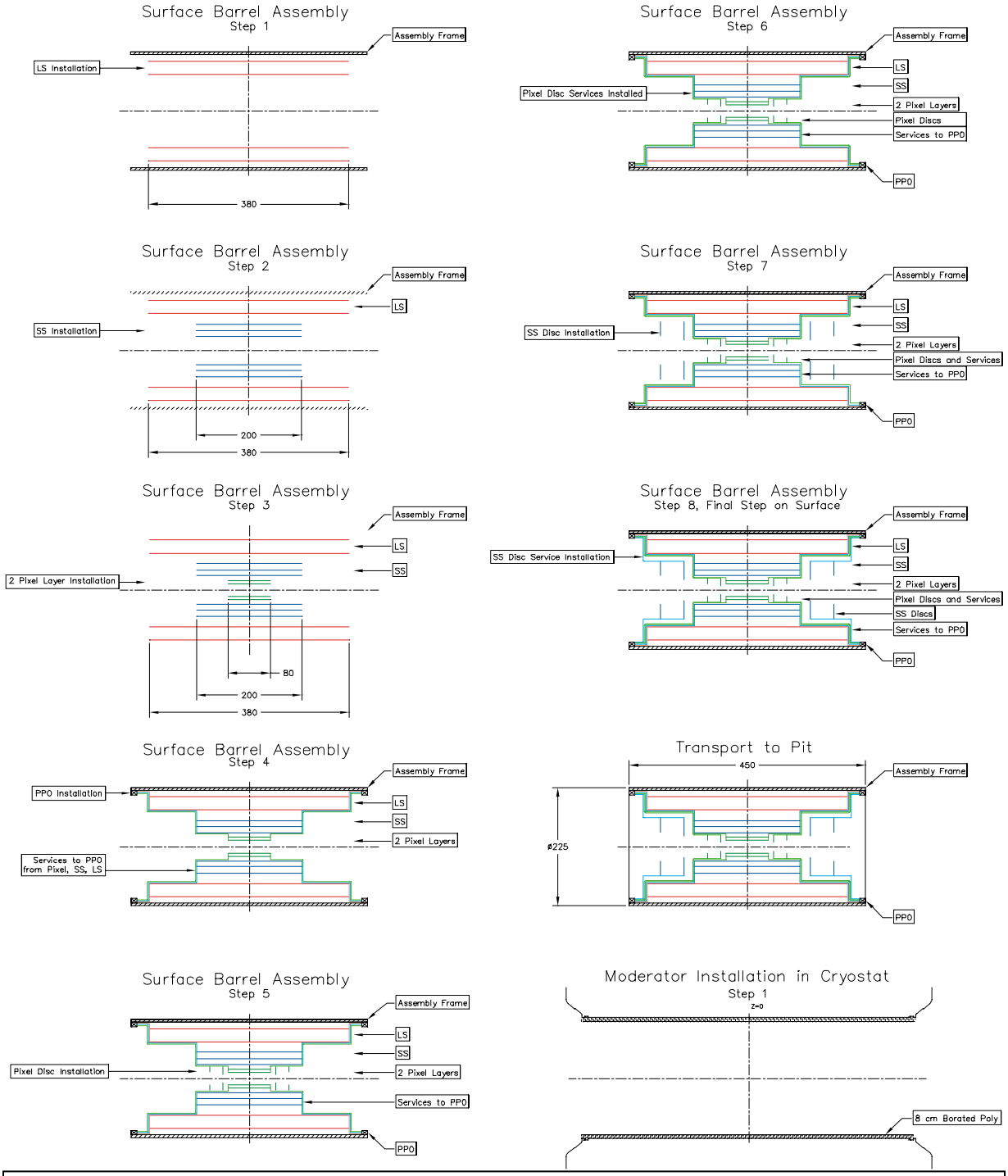


Figure 2. Possible assembly sequence for a fixed length barrel geometry with integrated pixel

I

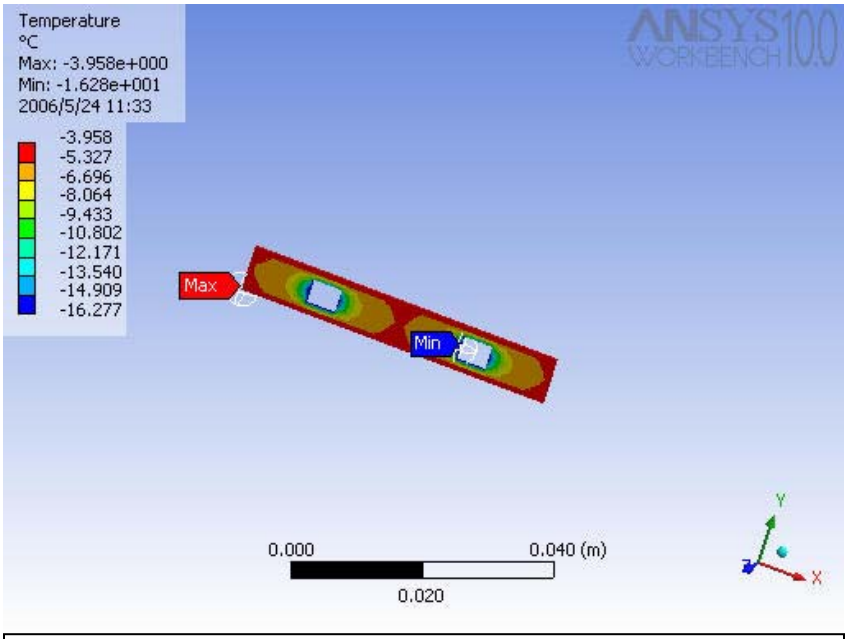


Figure 3. 0th order thermal finite element analysis of a CDF style stave

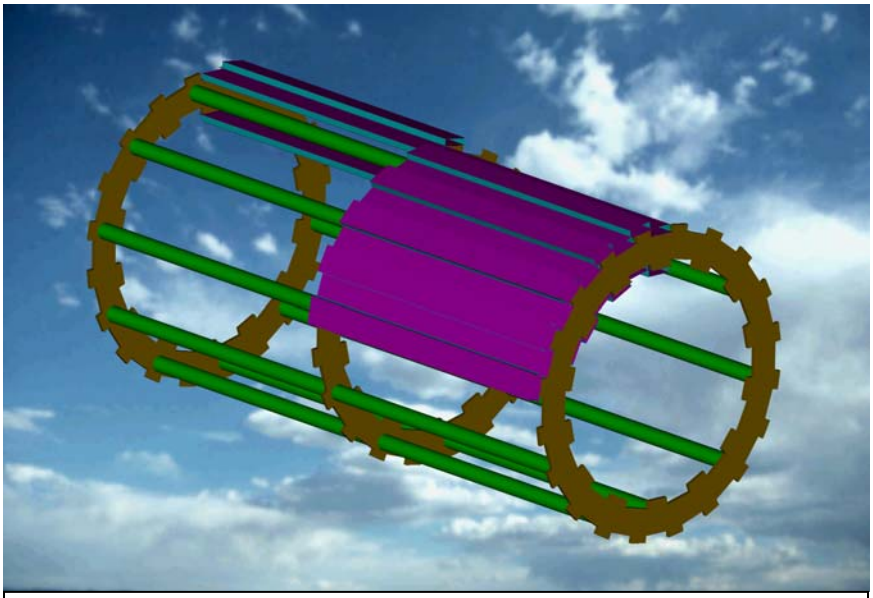


Figure 4. Early look at possible support for outer (2 meter long) staves.

ASSYMMETRICAL SENSORS POSITION

SYMMETRICAL SENSORS POSITION

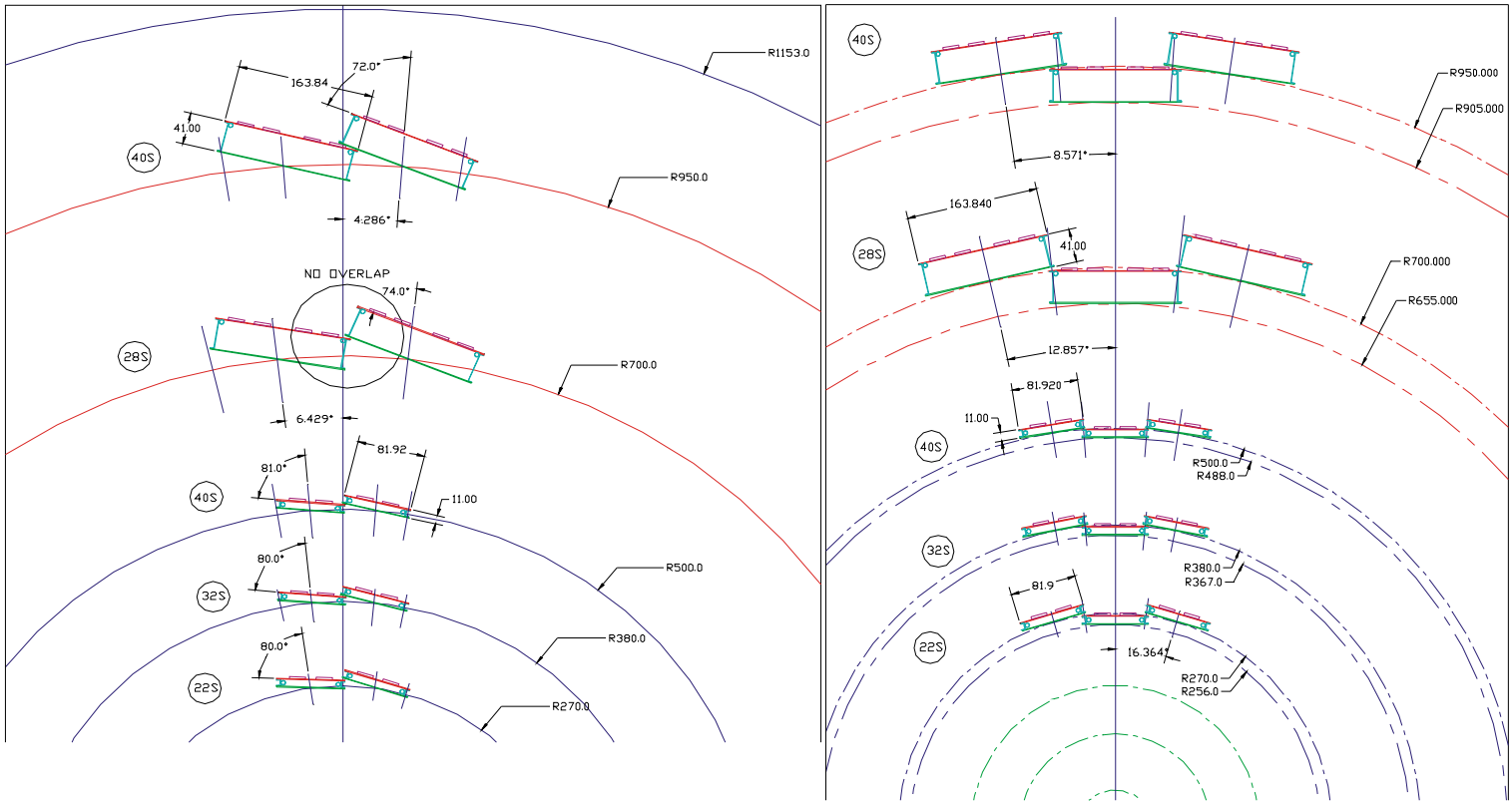


Figure 5. Comparison of Lorentz angle rotated and un-rotated mounting schemes

WBS 4.1.3.1.1, 4.1.3.1.2, 4.1.3.2.1, 4.1.3.4.1

Progress Report on Optical Link R&D for Inner Detector Upgrade

K.K. Gan, H.P. Kagan, and R.D. Kass
The Ohio State University

F. Rizatdinova
Oklahoma State University

P.L. Skubic, Rusty Boyd
University of Oklahoma

This is a progress report on the optical link R&D for the strip and pixel detector upgrade planned for SLHC. For FY06, we have investigated the feasibility of using the infrastructure of the current pixel optical link to transmit signals up to 1 Gb/s, a rate significantly higher than the current 80 Mb/s. The infrastructure studied includes micro twisted-pair cables, fusion spliced SIMM-GRIN fiber, and VCSEL and PIN diodes currently used in the pixel detector along with devices available from other vendors. We plan to irradiate the components to the SLHC dosage to test its radiation hardness. For FY07-8, we plan to upgrade the driver and receiver chips of the current pixel optical link to operate up to 1 Gb/s using the 0.13 μm process. The irradiation program will be continued, including the irradiation of the new driver and receiver chips.

Introduction

The SLHC is designed to increase the luminosity of the LHC by a factor of ten to 10^{35} $cm^{-2}s^{-1}$. The radiation level at the detector is expected to increase by a similar factor. We use the Non Ionizing Energy Loss (NIEL) scaling hypothesis to estimate the SLHC fluences [1-3] at the present pixel optical link location (PP0). The estimate is based on the assumption that the main radiation effect is surface damage in the CMOS devices due to ionizing radiation and bulk damage in the VCSEL and PIN with the displacement of atoms. After five years of operation at the SLHC, we expect the silicon component (e.g. ASIC and PIN) to be exposed to a maximum total fluence of 2.5 x 10^{15} 1-MeV n_{eq}/cm^2 [4]. The corresponding fluence for a GaAs component (e.g. VCSEL) is 1.4 x 10^{16} 1-MeV n_{eq}/cm^2.

The present SCT and pixel systems use receivers (DORICs) and drivers (VDCs) of similar architecture. The SCT chips were fabricated using bipolar integrated circuits (AMS 0.8 μm BICMOS). The pixel chips were modern versions fabricated with the deep submicron (0.25 μm) CMOS process of IBM. The VCSEL Driver Chip (VDC) converts the LVDS signal from a module into a single-ended signal appropriate to drive a VCSEL. The Digital Optical Receiver Integrated Circuit (DORIC) decodes a bi-phase mark

(BPM) encoded signal received at a PIN diode to extract a 40 MHz clock and command. An SCT optical module (harness) contains a DORIC and a dual-channel VDC coupled to an optical package with one PIN and two VCSELs. A pixel optical module (opto-board) contains two 4-channel VDCs and DORICs. The VDCs couple to an optical package with an 8-channel VCSEL array while the DORICs couple to a PIN array package. For the inner barrel (B) layer, two links are needed to transmit data off detector due to the higher hit occupancy. Each B-layer opto-board therefore contains two more 4-channel VDCs plus an additional optical package with a VCSEL array.

The design of the present pixel optical link has several nice features:

- Much reduced radiation level: Since the optical components are mounted on patch panels (PP0) instead of directly on the pixel modules, the radiation exposure is much reduced.
- Separation of modules and optical link production: The separation of the optical components from the modules decouples the production of the pixel modules and optical links, greatly simplifying the design and fabrication of both components.
- Removable and less fragile fiber ribbon: Each SCT optical harness contains one optical package with three single fibers permanently attached. In contrast, an optical package on a pixel opto-board couples to a removable 8-channel fiber ribbon terminated with an MT connector. A fiber ribbon is much less fragile than a single fiber.

The design therefore simplifies the fabrication, testing, and installation of the optical link. The plan of this R&D program is to study the feasibility of an upgrade based on the pixel architecture while taking advantage of the several years of R&D effort.

Data Transmission Speed

Driver Speed

A present SCT module transmits data at 40 Mb/s. The upgraded module is expected to have the same bandwidth. This is achieved by having a shorter module (~ 4 x shorter) at the inner radius to compensate for the higher occupancy. The pixel module will have ~ 3 x finer segmentation to maintain an acceptable occupancy. Consequently there will be more charge sharing and this is estimated to produce ~ 30% more hits. A pixel module for the present outer layers and disks transmits data at 80 Mb/s, using both edges of the 40 MHz clock. For the upgrade, we expect a bandwidth of 350 Mb/s (= [10/3] x 1.3 x 80 Mb/s). As in the present system, each module of the innermost layer could transmit data at twice the speed using two links.

Ideally, we would like the optical links of the upgraded pixel and strip systems to use as many common components as possible to reduce the cost in the development, procurement, and production. The different bandwidth requirements of the two systems present a particular challenge. One attractive upgrade scenario is for the upgraded strip tracker to use an architecture similar to the pixel system. This would require adding a serializer that serializes the data from 8 modules. This would be analogous to the pixel system with a module control chip (MCC) that serializes the data from 16 front-end (FE)

chips on a module. The strip serializer would then transmit data at 320 Mb/s. This is slightly slower than the 350 Mb/s needed for the pixel system but might prove adequate. Experience with ATLAS data in 2007 will clarify the bandwidth requirement. If this rate is proven to be inadequate, a strip serializer that serializes 16 modules would be needed to transmit data at 640 Mb/s per link.

The above pixel-based architecture will allow the development of a common opto-board that transmits data at either 320 or 640 Mb/s per link.

Receiver Speed

The present optical link receives a signal with a 40 MHz beam crossing clock that is bi-phase mark encoded with timing, trigger, and control (TTC) data. The beam crossing frequency of the SLHC is not yet determined. The question for the upgrade is whether TTC will be transmitted at the relatively low speed of ~ 40 MHz or at a much higher speed. The advantage for a low speed receiver is that a single event upset (SEU) in a PIN diode is unlikely to corrupt more than one bit. However, a higher speed TTC link might be needed to minimize dead time if frequent reconfiguration of the FE or serializer is necessary due to higher SEU rates. Experience with ATLAS data in 2007 will elucidate this question. Our educated guess is that a low speed link for the upgrade is adequate.

Space Constraints

The services for the upgraded silicon trackers must fit in the present space allocation. Consequently, the number of fiber ribbons should remain about the same even though the silicon trackers will have significantly more modules. Therefore the pixel-based architecture for the SCT with a serializer serving 8 modules would be a feasible space saving solution. For the pixel system, the space saving could be achieved by increasing the fiber count in a fiber ribbon from 8 to 12 channels with no significant increase in the fiber volume since most of the material in a ribbon is in the cladding. The present pixel link uses 6-7 channels in an 8-channel ribbon because a half stave contains 6-7 modules and a disk contains 6 modules. Therefore more savings can be achieved by using all channels in a ribbon with alternative stave and disk designs or signal routing scheme.

R&D Plans and Results

The proposed upgrade path will preserve much of the architecture of the present pixel electronics. This takes advantage the many years of development in the FE, MCC, and optical chips. The SCT upgrade based on the pixel architecture will satisfy the speed and space requirements with much simplified construction. To achieve the above upgrade scenario, R&D is needed to verify that the infrastructure can be upgraded to operate at the higher speed. The following is the R&D plan together with the results obtained so far. The plan complements other R&D efforts without duplication.

A crucial component of the R&D program is to construct a test system. A single-channel prototype version of the system has been constructed by The Ohio State University group. The prototype can transmit both electrical and optical signals over a large dynamic range, from tens of Mb/s to several Gb/s. The signal pattern is programmable, from

various repetitive patterns to pseudo random. The system allows for measurements of the rise/fall time, amplitude, duty cycle, clock jitter, and bit error rate of both electrical and optical signals. This prototype system is used to perform the measurements reported below. Duplicate systems have been distributed to Oklahoma and Oklahoma State Universities. The prototype systems will soon be replaced by a more advanced multi-channel system that is currently being fabricated. This advanced system will then be deployed in the irradiation.

Wire Link

The present pixel optical link uses a micro twisted pair of wires for transmitting LVDS signals between a module and its associated driver and receiver chips on an opto-board. It is crucial to find out soon whether high-speed signals can be transmitted with the low-mass cable since mounting optical components directly on a module have several undesirable consequences.

The Ohio State University group has investigated bandwidths of micro twisted pairs with various lengths, diameters, and numbers of turns per inch (TPI) as shown in Fig. 1. The lengths shown represent the longest and shortest wires in the current pixel detector. The current wire for the barrel pixel detector with a diameter of 100 μm (38 AWG) and 5 TPI has the fastest rise and fall times of the wires tested. Fig. 2 shows eye diagrams produced by transmission of 640 Mb/s and 1 Gb/s pseudo random data in the barrel wire. It is evident that the current barrel wire is adequate for transmitting signals at 640 Mb/s.

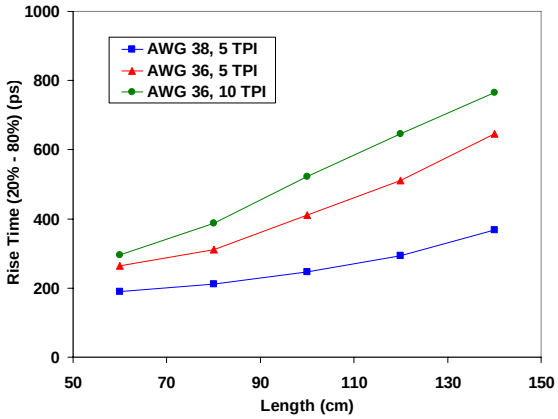
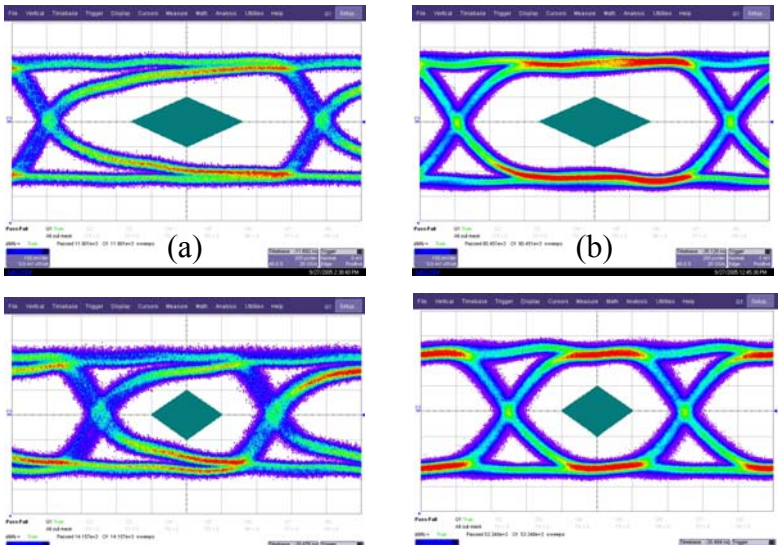


Figure 1. Bandwidth of the micro twisted pairs vs. wire length for wires of various diameters and number of turns per inch (TPI).



(c) (d)

Figure 2. Eye diagrams for (a) 640 Mb/s and (c) 1 Gb/s signals in a 1.4 m barrel wire. (b,d) show the corresponding signals with a 0.6 m barrel wire.

Fiber Link

There are three kinds of commercial fibers available with each having different bandwidths. Single mode fiber with a core diameter of ~6 μm has no modal dispersion and hence the highest bandwidth. The other two fibers, GRIN and SIMM, are multi-mode fibers with core diameters of 50 or 62.5 μm. The former has medium bandwidth and is radiation tolerant. The latter is lower bandwidth and has a radiation-hard pure silica core. Each present pixel optical link has 8 m of SIMM fiber ribbon spliced to 70 m of GRIN fiber ribbon.

It is critically important that we measure the bandwidth of a fusion spliced SIMM-GRIN ribbon with length similar to what is used in the pixel optical link. If the spliced ribbon cannot support a high-speed transmission, we need to start immediately on an R&D program for fabricating a new kind of opto-pack that couples to a single mode fiber ribbon since this requires a much more precise VCSEL to fiber alignment.

The Ohio State University group has measured the bandwidth of a fusion spliced fiber as shown in Fig. 3. It is evident that the fiber can adequately transmit signals up to at least 1 Gb/s and hence the transmission bandwidth of the wire link will be the limiting factor.

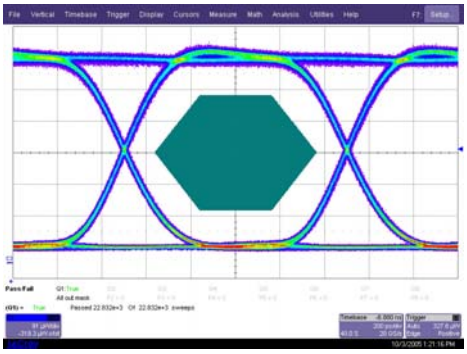


Figure 3. Eye diagram for 1 Gb/s pseudo random signals after 29 m of fusion spliced SIMM-GRIN fiber.

PIN

Commercial PIN arrays are fabricated using silicon, GaAs, or InGaAs. The silicon devices are radiation hard. We need to purchase silicon PINs and evaluate the following characteristics:

- rise and fall times vs. bias voltage before and after irradiation
- PIN responsivity vs. bias voltage before and after irradiation

In the R&D proposal, the consortium of three US universities plans to do the above characterization during the first year and hopefully identify one or two candidate arrays. We also need to measure the lifetime of the candidate arrays after irradiation. The Oklahoma groups will develop the protocol for the lifetime measurement via elevated temperature.

We have conducted a market survey and found that Truelight is the only vendor that currently fabricates silicon PIN arrays. This is the same vendor that supplies PIN arrays for the current pixel optical link. There are three vendors that supply GaAs PIN arrays. These could be used in off-detector electronics as the faster GaAs devices probably would not have the large baseline shift as observed in the Truelight arrays.

In our original R&D plan, the hope was that our Taiwanese colleagues would package the arrays. Unfortunately, Taiwan's commitment to the SLHC remains unresolved and consequently, Taiwan is currently not able to provide the packaging. Therefore we will use the optical package designed by The Ohio State University group. This new optical package has several nice features:

- use BeO as the substrate instead of FR-4 as in the Taiwan design. This provides efficient removal of the heat produced by the VCSEL arrays, the largest heat source in the optical link.
- more compact than the Taiwan design.
- connection to the VCSEL/PIN arrays via wire bonding instead of soldering. This allows easy replacement of an optical package and easy rerouting of signals to different VCSEL channels as frequently needed in an R&D program.

We have prototyped the concept using scrap alumina pieces from a previous project to verify the principle of the design. We decided to fabricate VCSEL optical packages instead of PIN packages due to the much more stringent alignment requirement. Four optical packages have been fabricated with passive VCSEL alignment. The coupled optical powers are excellent, with an average of 1.5 mW and a minimum of 1.2 mW. This has verified the principle of the design. For FY07, we propose to continue the development of the optical package. We expect three iterations with BeO as the substrate to achieve an optimum design.

VCSEL

Commercial VCSEL arrays will be acquired to evaluate:

- rise and fall times at various VCSEL currents before and after irradiation
- LIV curve before and after irradiation. The light (L) vs. drive current (I) curve will be of particular interest, i.e. what is the light output at 10 mA, the current default operating current. The voltage (V) vs. current (I) curve is needed for the driver design, i.e. what is the voltage needed to supply 10 and 20 mA of current in the VCSEL. The latter is considered to be the optimal current for efficient annealing based on previous irradiation experience with Mitel VCSELs in the SCT opto-link. Experience with Truelight VCSELs in the pixel opto-link showed

that annealing at lower current is adequate. The annealing current requirement in the higher radiation environment for various commercial devices will be evaluated.

The Ohio State University group has acquired packaged single-channel VCSELs from four vendors. Figure 4 shows the rise and fall time of the VCSELs. All VCSELs have similar characteristics. LIV curves of three VCSELs are shown in Fig. 5; one VCSEL cannot be characterized because it is packaged within a commercial small form factor transceiver. All VCSELs produce good optical power. However, the ULM VCSELs require significantly higher voltage to produce the same VCSEL current and may not be suitable for the SLHC application. We are awaiting delivery of a lower voltage VCSEL from ULM to evaluate its characteristics. Furthermore, we have acquired VCSEL arrays from the three vendors and plan to characterize them using our own packaging by July to select the candidate arrays for irradiation.

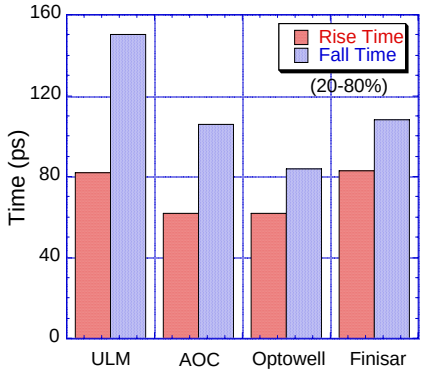


Figure 4. Rise and fall times of VCSELs from four vendors.

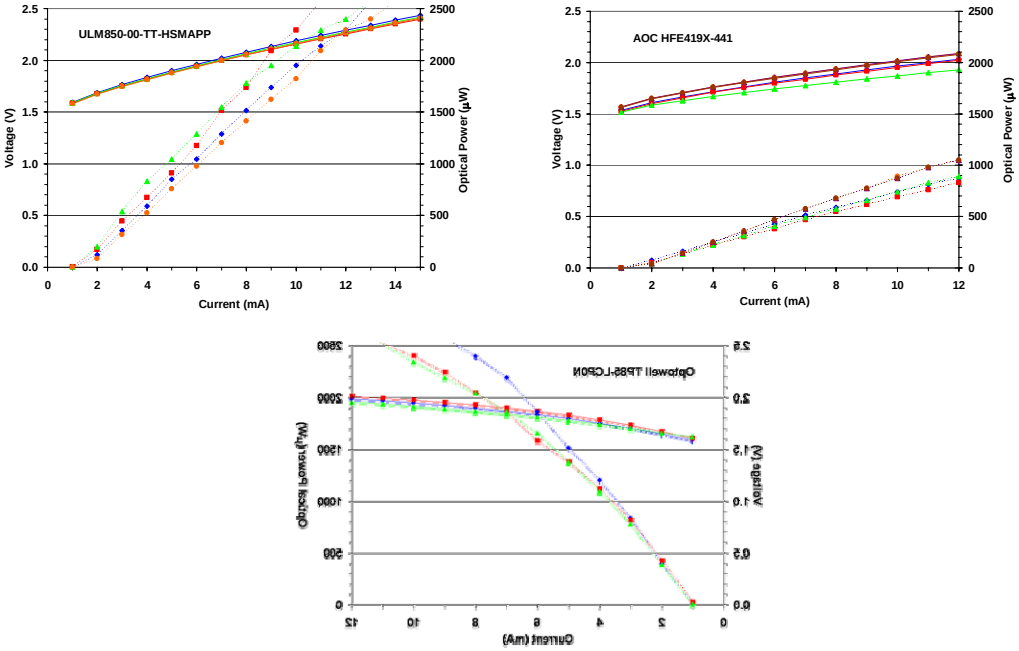


Figure 5. LIV curves of packaged VCSELs from three vendors.

Driver/Receiver

The VDC and DORIC of the present pixel opto-link need to be converted from the 0.25 μm layout to 0.13 μm. Unfortunately, the nominal operating voltage for the smaller feature size is 1.3 V and is inadequate to drive a VCSEL. The thick oxide option has a nominal supply voltage of 2.5 V and must be used in the driver design. Developing the chips using the same process as the pixel FE and MCC, which will most likely be based on the 0.13 μm technology, will allow submissions of some prototype and production chips in the same run for cost saving as in the present development of the pixel optical chips. We will start the conversion and simulation near the end of FY06 and submit the prototype chips for fabrication during the second and third years.

Irradiations

All optical components need to be irradiated to the SLHC dosage. Our irradiations will concentrate on using 24 GeV protons from the PS accelerator complex at CERN. The Ohio State University group has extensive experience with this irradiation facility from the development of the present pixel opto-link system. As noted above, the test system to be used during the irradiation is still under construction. We will test the setup in the laboratory before shipping to CERN. The following components will be irradiated:

- FY06: LHC production opto-boards with candidate PIN/VCSEL arrays and LHC receiver/driver chips
- FY07-8: SLHC opto-boards with candidate PIN/VCSEL arrays and SLHC receiver/driver chips

We will irradiate for several hours a day and spend the rest of the day annealing the VCSELs with high current. During the irradiation, we will measure the SEU vs. the PIN current. Our first irradiation is scheduled for August 2006.

Milestones and Budget

The milestones of the R&D program are summarized in Table I. We have met the first two milestones. The delay in identifying the VCSEL/PIN candidates is due to fact that we need to develop our own optical packages rather then using packages from Taiwan. The June irradiation date was based on an educated guess as the CERN irradiation schedule was not available at that time. The approved budget of the three institutions for FY06 together with the budget request for FY07-8 is shown in Table II.

Table I. Milestones of the R&D program.

Goal	Current	Actual
Wire link solution identified	May 06	May 06
Fiber link solution identified	May 06	May 06
VCSEL/PIN candidates identified	May 06	July 06
1st irradiation	June 06	August 06
1st chip prototype received	March 07	
2nd irradiation	June 07	
2nd chip prototype received	March 08	
3rd irradiation	June 08	

References

[1] I. Gregor, “Optical Links for the ATLAS Pixel Detector,” Ph.D. Thesis, University of Wuppertal (2001).

[2] A. Van Ginneken, “Nonionzing Energy Deposition in Silicon for Radiation Damage Studies,” FERMILAB-FN-0522, Oct. 1989.

[3] A. Chilingarov, J.S. Meyer, T. Sloan, “Radiation Damage due to NIEL in GaAs Particle Detectors,” Nucl. Instrum. Meth. A 395 (1997) 35.

[4] The fluences include a 50% headroom as a safety margin.

Table II. Approved budget of the three institutions for FY06 together with the request for FY07-8 in unit of thousands of dollars.

FY	06	07	08
Ohio State U.			
Technician (1/2 FTE)	22.1	22.8	23.4
Engineer (1/4 FTE)	18.1	18.9	19.5
Student	4.0	4.0	4.0
Cables/fibers	4.0	2.0	2.0
VCSEL/PIN	8.0	2.0	2.0
Chip Prototype		57.5	57.5
Equipment	15.0	12.5	8.0
PCB	3.0	3.0	3.0
BeO		6.0	3.0
M&S	9.0	8.0	7.0
Irradiation	8.0	6.0	6.0
Cadence	4.5	4.5	4.5
Irrad travel	3.0	3.0	3.0
Indirect cost	38.3	39.4	35.4
Sub total	137.0	189.5	178.3
Oklahoma State U.			
Graduate student	16.5	13.4	18.3
Technician (1/2 FTE)	19.2	20.3	21.4
Test system	10.0		
M&S	3.0		
Travel	3.0	3.0	3.0
Indirect cost	19.4	16.3	19.8
Sub total	71.1	53.0	62.5
Oklahoma U.			
EE Graduate student (1/2 FTE)	14.0	14.0	14.0
Equipment	10.1	10.1	
M&S	3.0	3.0	3.0
Travel	3.0	3.0	3.0
Indirect cost	8.8	8.8	8.8
Sub total	38.9	38.9	28.8
Total	247.0	287.9	279.4

WBS 4.1.3.2.2

Report on WBS 4.1.3.2.2 and Funding Request for FY 2007

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Dallas, Texas 75275

Progress Report

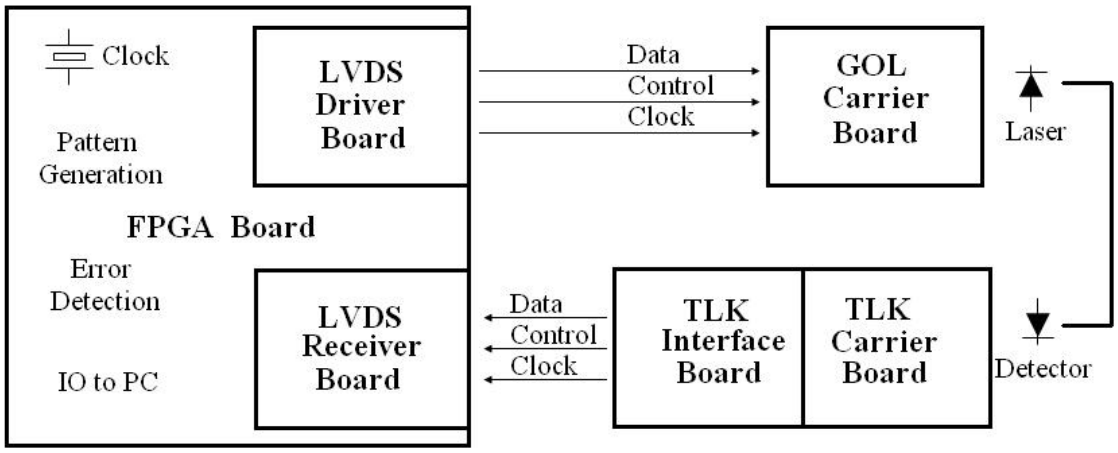
The purpose of this project is to evaluate the CERN Gigabit Optical Link (GOL) Transmitter chip made in 0.25 micron technology for the ATLAS inner detector readout upgrade. GOL combines serializer and laser driver functions on one chip. Issues that need to be paid attention to at system design level include: input timing between data and the reference clock; jitter transfer function of the serializer from the reference clock to the serial data stream; and system jitter tolerance of the reference clock with a specific receiver. We plan to carry out system level studies of this chip to understand the following: (a) the system's clock jitter tolerance with HDMP-1024 or TLK2501 as the receiver chip; (b) the jitter conversion from the reference clock to the serial data stream through the GOL; (c) the GOL driving characteristics with a VCSEL laser as well as DFB and FP lasers. We also plan to carry out irradiation tests on the GOL chip in a link system to study its resistance to total ionization dose and its radiation induced single event upset rate up to inner detector upgrade required level.

The work planned for FY 2006 is detailed in the proposal we sent in a year ago. Essentially we planned to construct the optical link system with GOL as its transmitter chip, providing testing points for verification of operating parameters during various tests. We also designed special PCB arrangement for irradiation tests to separate GOL chip being irradiated from other board components that should be protected from radiation.

During this work, we added two more requirements in our system design: (1) Power up scheme study. It was reported that GOL chip might fail to start-up correctly due to partial charge from circuits elsewhere in the system. CERN developed a special power-up chip (CR4T) to handle this problem. After extended discussions with GOL chip designer, we incorporated CR4T in our design with 3 power-up schemes to study each scheme's reliability; (2) we collaborate with the Oxford UK group (Cigdem Issever, Todd Huffman and Tony Weidberg) on the neutron irradiation of the GOL chip, and incorporated their requests into the PCB layout in such a way that the same board may also be used for the planned neutron tests by the Oxford group. One set of the boards have been sent to UK for their evaluation.

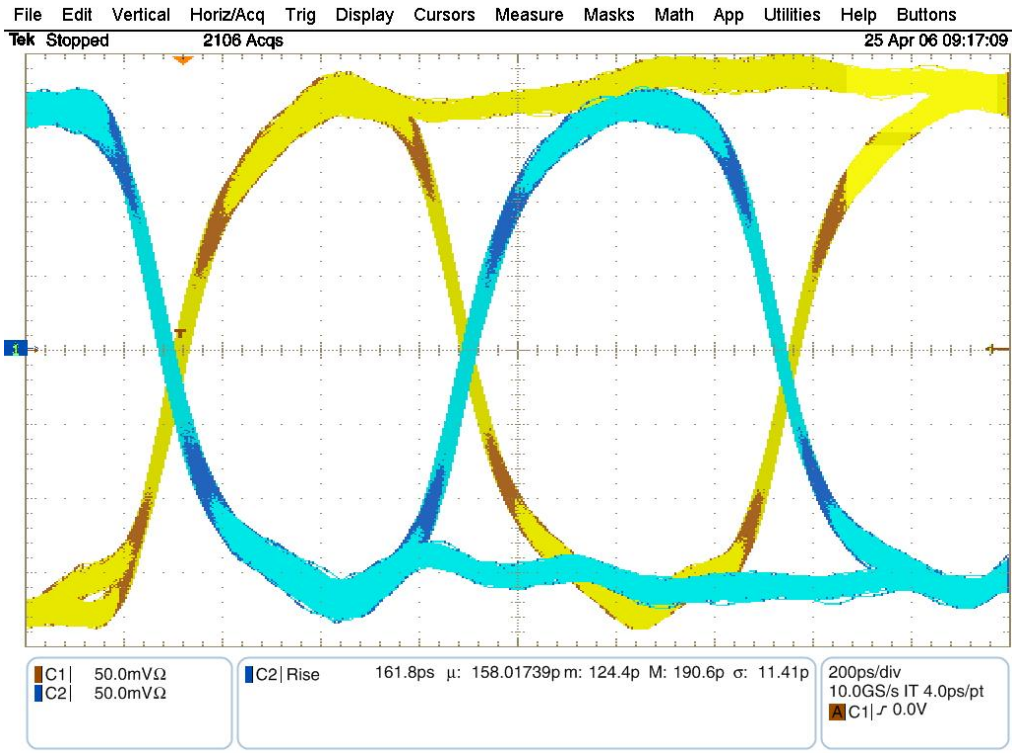
We started this work on borrowed support from SMU.

The system level design started in October 2005. The corresponding PCBs design was finalized in March 2006. Shown in the following figure is the block diagram of the system. All the boards are shown in the following pictures.

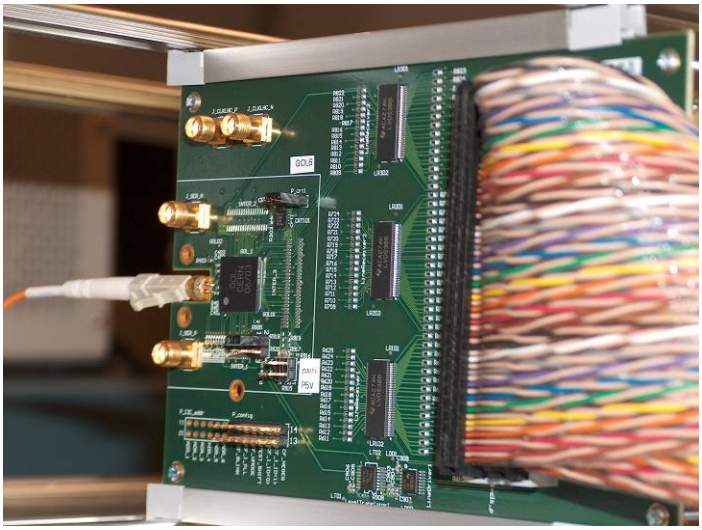


GOL test block diagram.

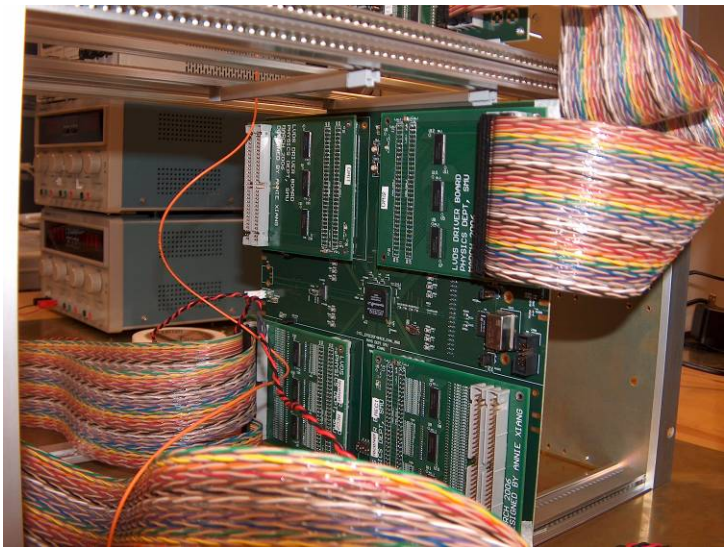
The system debugging is close to completion and we are preparing for characterization studies. The complete data link has passed proof-of-concept and pseudo-high speed tests. Shown below is an optical eye-diagram of serial data transmission at 1.6Gbps. Random pattern testing is underway and we will then continue onto jitter analysis and laser evaluation.



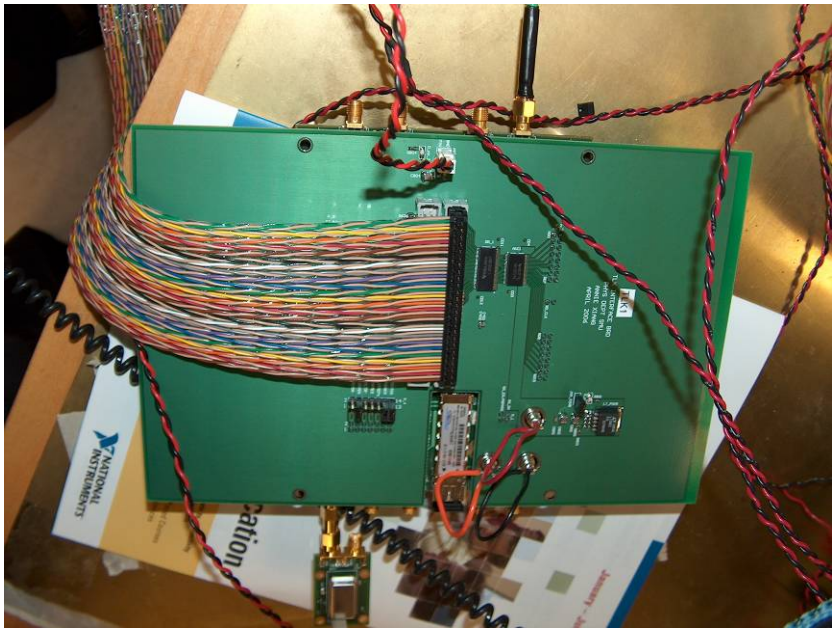
Optical eye-diagrams with GOL sending “alignment signals”



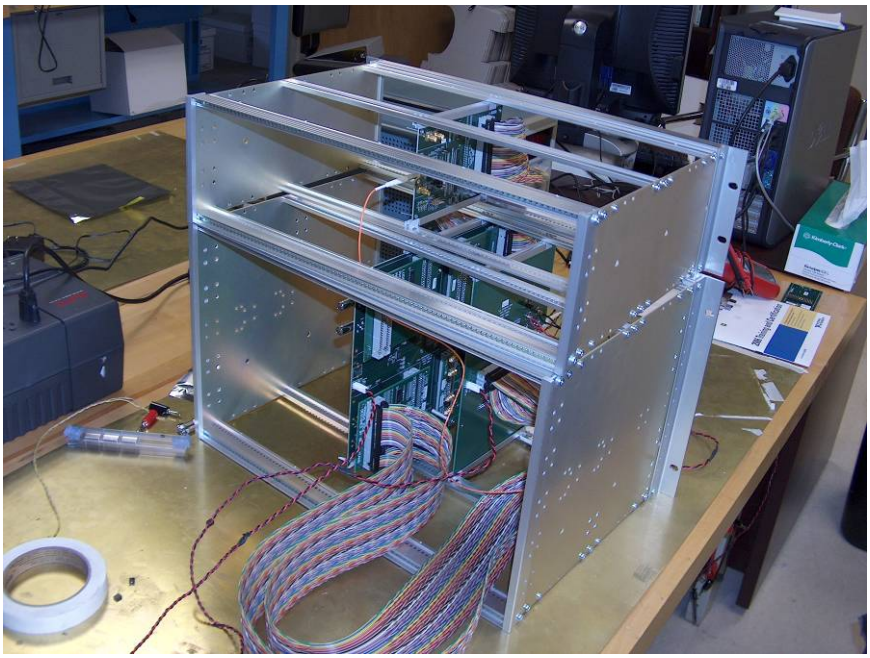
The GOL carrier board with VCSEL attached. Parallel data are sent in through twist pairs 2 meters away from a FPGA based pattern generator board. This to make sure that only the GOL chip will be exposed to radiation during an irradiation test.



The FPGA based pattern generator board with its signal driver and receiver boards. All signals are LVDS standard for long distance (2 meters) transmission. This system can be used for other in lab and radiation tests.



The adapter board for the optical receiver board. We use TI's TLK evaluation board as the receiver board. This evaluation board does not have LVDS signal interface and is not suitable for tests in radiation. The adapter board is built to solve this problem.



The whole system in the 3U VME crate (to be placed in the beam) and the 6U VME crate remaining outside the beam.

We plan to carry out the rest of lab tests during this summer and irradiation tests this fall, depending on the status of the R&D in the Link-on-Chip project for the LAr readout upgrade so that we can purchase longer beam time to do a careful study on the GOL chip.

Plan and Budget for FY 2007

As we stated in our proposal, the first year will be spent on the design and tests, the second year we plan to arrive at a complete link design, ready to be incorporated in the inner detector readout system. In this year's work, the system becomes more complicated than originally planned due to additional features requested by the Oxford group. Based on past experience, we would like to revise our budget request to increase support for more engineer's time and travel to collaborating institutes. We feel this increase is important to apply what we have learned and will be learning to the actual readout system.

FY07:

1. Final link system design.
   System design, schematics capturing and PCB layout. This work includes interactions with the inner detector readout group to define the technology to be used, and the part of work SMU can contribute.
   Jan.2007 – April.2007, work done at SMU
   We requested:
   1.5 months FTE, $6.3k, w/ 25% benefit, 45% oh ➔ $11.4k
   Revise to:
   4 months FTE, $17.3k, w/ 25% benefit, 45% oh ➔ $31.4k
   1.2 PCB fabrication.
   April 2007 – May 2007, work done by Eagle Circuits
   PCB fab. + assembly $8k (BGA mounting, 6 to 8 layer board)
   Components $2k
   Total w/ 45% overhead ➔ $14.5k
2. Lab tests on system performance including jitter, eye diagram and sensitivities and data analysis, reporting notes.
   May 2007 – October 2007, work done ay SMU
   We requested:
   3 months FTE, $12.5k, w/ 25% benefit, 45% oh ➔ $22.7k
   Revise to:
   4 months FTE, $17.3k, w/ 25% benefit, 45% oh ➔ $31.4k
3. Engineer's travel to collaboration meetings.
   We requested:
   2 trips at $1k, w/ 45% oh → $2.9k
   Revise to:
   4 trips at $1k, w/ 45% oh → $5.8k

So the total for FY07, $51.1k requested is now revised to be $83.1k, of which $62.8k is for manpower and $20.3k is for material and supplies.

19-June-2006

WBS 4.1.4.1.1
ATLAS Tracking at SLHC: Development of a Stave Readout Structure: FY2006 Report and FY2007 Plan

Lawrence Berkeley National Lab
Brookhaven National Lab
Hampton University
Yale University

This document describes the US ATLAS stave development plan for FY2007. The FY2006 effort is within budget. The basic stave construction and test efforts at LBNL are on schedule. We have not however moved some of activities out of LBNL as originally scheduled yet. This reflects a re-adjustment of priorities as the project has evolved. The plans for a follow-on effort (this document) reflect conclusions reached in FY2006 reflecting the Genoa Meeting and discussions with other non-US ATLAS colleagues. The plan is also informed by the concurrent proposal for stave development submitted to the ATLAS Upgrade Steering Group. That proposal supplements this report as well.

Completion of FY2006 milestones.

Here we give a status and update on the prior years milestones. The last column entries are status or new dates.

Phase 1 Milestones (completion dates given):

1.	full electrical specification and schematic for Phase 1 stave	10/04	done
2.	establishment of test stands at LBNL, BNL, and Hampton	11/04	done
3.	validation of test stand operation on test parts	12/04	done
4.	design and layout of Phase 1 hybrid	12/04	done
5.	fabrication of hybrid	03/05	done
6.	assembly and test of hybrid	04/05	done
7.	re-commission and tests with existing fixtures	03/05	done
8.	assembly of ATLAS staves	06/05	done
9.	initial test of ATLAS staves at LBNL	07/05	done
10.	transfer to and test of staves at BNL/Hampton	12/05	8/06
11.	irradiation studies of staves	2/06	12/06
12.	transfer of assembly methods to BNL	12/05	9/06

Conclusions from Genoa and ATLAS wide discussions

We left Genoa with a basic concept for an ATLAS tracker (outside the pixel region). The concept is shown in Figure 1. The tracker consists of only two types of staves, described below.

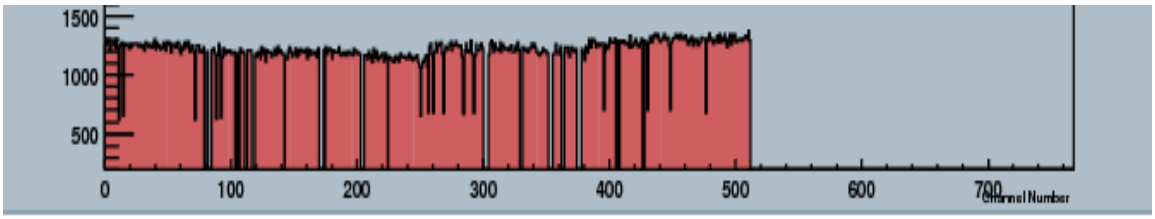
- Inner layer stave: This stave is (approx) 1 meter long. It carries (approx) 3 cm long "short-strip" detectors. These are tiled alternately on the two faces to give full coverage along the z-axis. Each stave holds (approx) 32 detectors, 16 on each side. The pitch is 80 microns and there are 768 or 896 strips per detector. The hybrids and fanouts are adjacent to the detectors. The scheme is shown in Figure 2.

- Outer layer stave: This stave is (approx) 2 meters long. It carries (approx) 10 cm long detectors in a stereo u-v configuration (like SCT). Each stave holds (approx) 20 detectors per side (a total of 40 detectors). There are small (3 mm) z gaps between each crystal. The hybrids and fanouts are glued on top of the crystals. The scheme is shown in Figure 2.

- Alternate powering (serial or DC-DC conversion) are seen as an integral aspect of future stave development. Evaluating these as part of the stave testing is of equal priority to the mechanical, assembly, and packaging aspects.

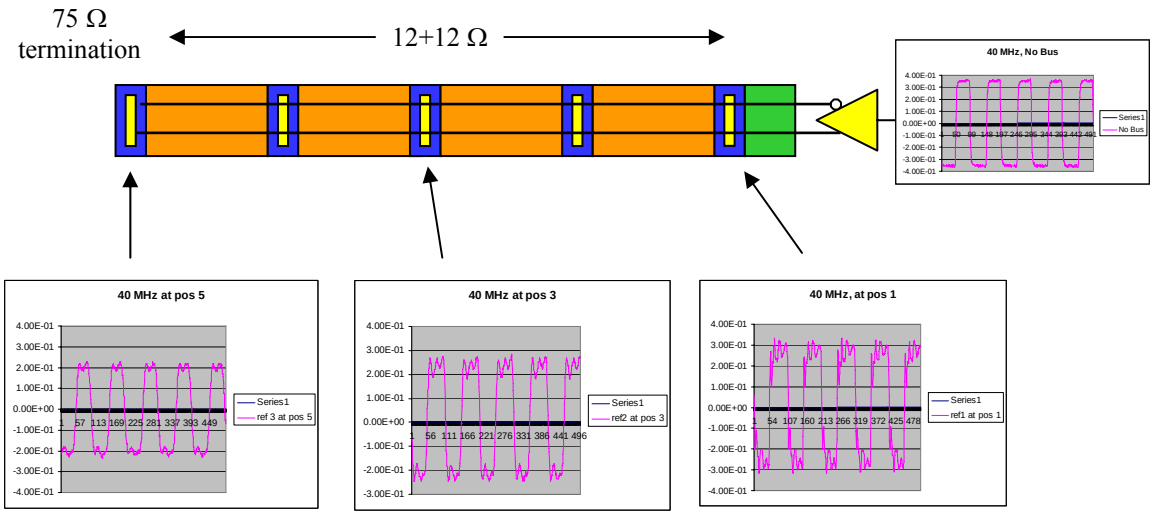
Review of Plan from FY2006 *with comments and accomplishments in italics*

Below we remark specifically on the items in the 2006 plan. Beyond these items, a number of modules were assembled and tested on and off the parallel powered stave. They worked as expected and showed, if anything, improved noise performance on the stave. In particular modules were operated concurrently with control, clock, and data flowing to and from other modules. We presume the engineered and compact ground and power configuration of the stave is a key aspect to this good performance. See figure below.



Hybrid + detector in 3rd position mounted on stave with concurrent operation of detector in position 1.

Studies of multi-drop LVDS clock distribution on the stave were also completed. See figure below.



LVDS signal integrity with significant DC bus cable resistance is still acceptable for timing and data transmission requirements

Abstracts describing all aspects of the project have been submitted to the 2006 IEEE NSS conference and the 2006 Hiroshima (Carmel) Silicon Detector conference.

The basic plan for FY2006 was:

1. Advance the stave design to study alternative powering schemes: As discussed in Genoa, a significant reduction in services is likely to come from a change in power distribution. Two basic schemes can be considered, serial powering or local DC-DC conversion. Serial powering has been studied at RAL using existing SCT modules with good results. Voltage conversion is the subject of an IC design effort at Berkeley. To incorporate these schemes into the stave will require a modification to the hybrid and stave bus cable as well as the development or procurement of the basic components.
   1.1. Development of serial powering components (LBNL): Serial powering can be implemented on the FY2005 stave with the addition of a new "power-interface" hybrid. This hybrid would be placed between the existing hybrid and the bus cable bond pads. The scheme is shown in Figure 4. This hybrid will be designed and fabricated in the FY2006 project.

   In FY2006 this effort became an active collaboration with RAL. The "power-interface" hybrid was designed collaboratively. RAL had it fabricated and it is scheduled to be tested in modules and stave in late June 2006 at LBNL. A serial powering bus cable was also designed and is currently in fabrication.

   1.2. Development of DC-DC converter circuit (LBNL): As stated, design effort is underway with separate funding. The viability of this approach will be reviewed. If viewed as promising a second power-interface hybrid could be developed as well. (We will explore the possibility that a single interface hybrid could be used for DC-DC and serial powering tests.)

The IC development effort did not proceed far enough to lead to a DC-DC "power-interface" hybrid. The serial version of the hybrid pin-out was designed to also be compatible with DC-DC conversion.

1.3. System level studies of serial and DC-DC powering (BNL): A number of critical issues need to be addressed using test boards and available components. Also fail-safe schemes need to be studied and evaluated. A system level design and specification will be derived.

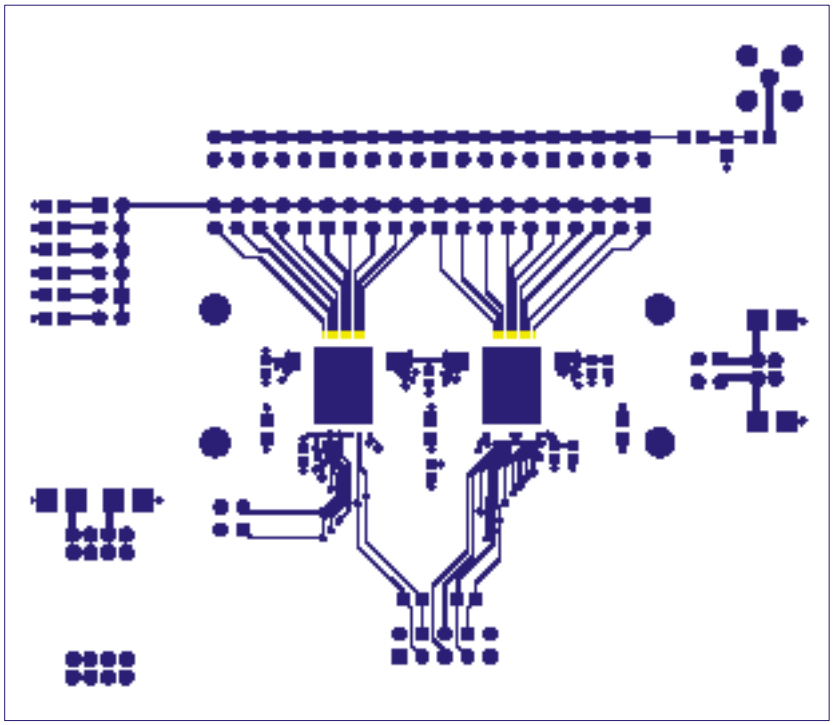
Some preliminary engineering work on this aspect has occurred.

2. Development of special control and readout electronics to test multi-module deadtimeless operation (BNL): The present SCT test electronics (MUSTARD-SLOC-CLOAC) are best suited for sequential testing of modules. We will explore the development of a multi-modular test board which is particularly suited for stave-like objects.

We have chosen a solution that utilizes a commercial module, the National Instruments PXI based 6151 wave generator/analyzer card to control and read out multiple hybrid modules. A single card is capable of controlling and simultaneously acquiring data from at least 14 modules, while two modules can simultaneously read out 30 modules. The system is further expandable in readout capability in multiplies of 16 modules.

Software development has begun at LBL, with further development taking place at BNL. LabView(LV) and C are the software platforms in use. A full set of control and acquisition routines have been written in LV and are in the process of being debugged. A breakout card has been configured to connect SCT hybrids and modules to 6151.

A simple card containing just two ABCD chips is being developed at BNL to facilitate the software development. It is envisioned these cards will be provided to other institutions to aid in their setting up a duplicate DAQ system. A preliminary, but almost final layout of one layer of the card is shown below.



Simple ABCD test card

3. Development of detectors (BNL): For the outer layer staves the existing CDF Run IIb detectors are well suited and still available. For the inner layer (SCT region) staves a new short strip detector is required. This would have (approx) 3 cm long strips. It might be fabricated in a p bulk process. The development and fabrication of a quantity of the short detectors would be undertaken.

The large quantity of detectors required (~100) ruled out in-house production at BNL. We obtained quotes to produce short strip detectors from both Hammamatsu and Sintef. As Sintef's quote was higher than expected, we chose to produce detectors via Hammamatsu. This choice has the added benefit in that the detector will be very similar to the present SCT detector, only shorter (about ½ the length). In order that the detectors are fully compatible with the ABCD chip, we will fabricate p on n-type detectors. The order has been placed and the detectors are expected in about six months. These detectors are an integral part of the 1 meter ATLAS stave test at the center of the 2007 workplan.

4. Stave mechanics (LBNL and BNL): The inner layer stave would be thin and (approx) 1 meter long. This is about 50% longer than the CDF stave so is probably not a major deviation. For the outer layers an (approx) 2 meter stave is close to optimum. The design of this object is certainly more complex technically. We propose to mount some engineering effort in this direction. We would initiate this by consulting with the Fermilab engineers who developed the CDF stave. This would be followed by appropriate fixture development and fabrications.

A considerable design and simulation effort has occurred in collaboration with Bill Miller at ITI, an outside consultant to the project. This effort is described further in an accompanying report. The effort has focused on the mechanics and cooling of a 1 meter long stave. A design has been found which shows minimal gravitational sag (<60 microns) and negligible thermal deformation (<10 microns). Fiber lay-ups and materials have been identified (4/1 fibers) and selected as well as a cooling tube and core configuration. The design is moving into engineering drawings and assembly fixture design.

Some effort has gone to consider also the 2 meter stave. The basic conclusion is that similar sag can be achieved with an intermediate support at 1 meter.

Preliminary work on developing stave design and measurement capability has begun at BNL. Initial thermal and mechanical finite element analysis has begun. As work on the CDF style stave is well advanced at LBL, BNL is looking into some alternative, though similar designs. Additionally, BNL will study the implications of a 2-d inner stave should later simulation demonstrate that 2-d information from the inner staves is necessary.

Budget (2006)

In the accompanying spread-sheet a budget for all the activities listed above is calculated. The estimates for LBNL and BNL are both $115K. The Hampton tasks are not specified but it is expected that Hampton will engage with either of the National Labs on some aspect of the testing and characterization of the devise. The Hampton cost is $20K.

A fraction of the money allocated remains un-committed. This is because RAL built the serial-power hybrid at no cost to us, the DC-DC effort did not reach the hybrid phase, and stave fixturing costs were less than anticipated. The excess funds can be used to support the FY2007 activity and front load the stave mechanical fixturing in the near term (summer 2006). This is all reflected in the new budget request (attached).

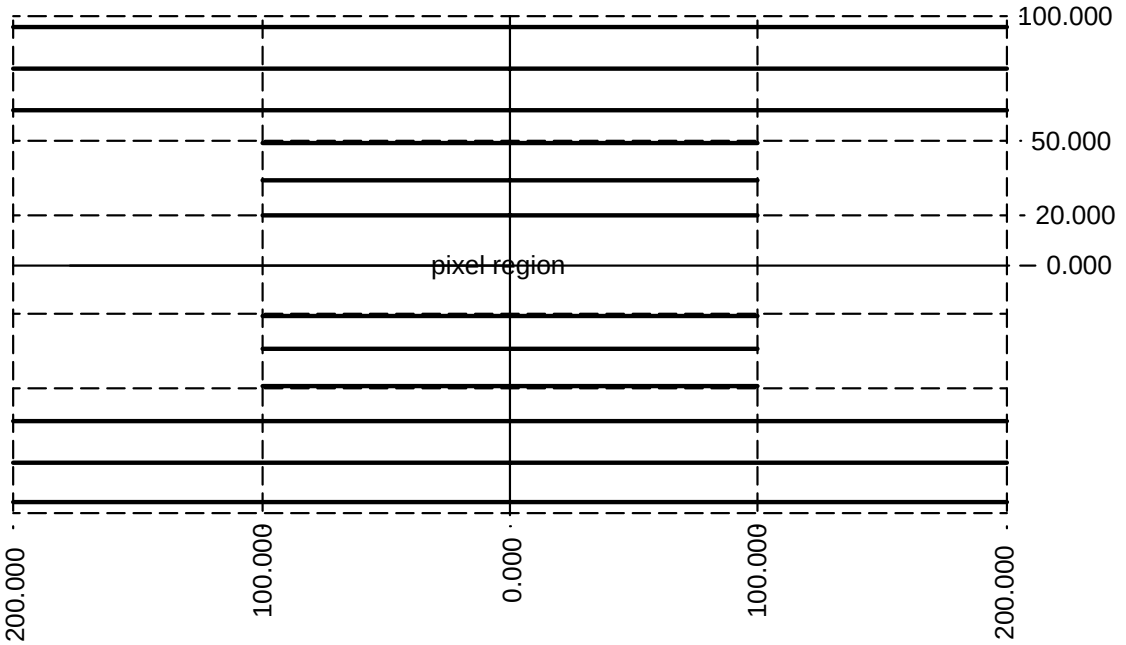


Figure 1: Overall barrel tracker layout shows intermediate and outer stave regions with a default of three stave layers in each region.

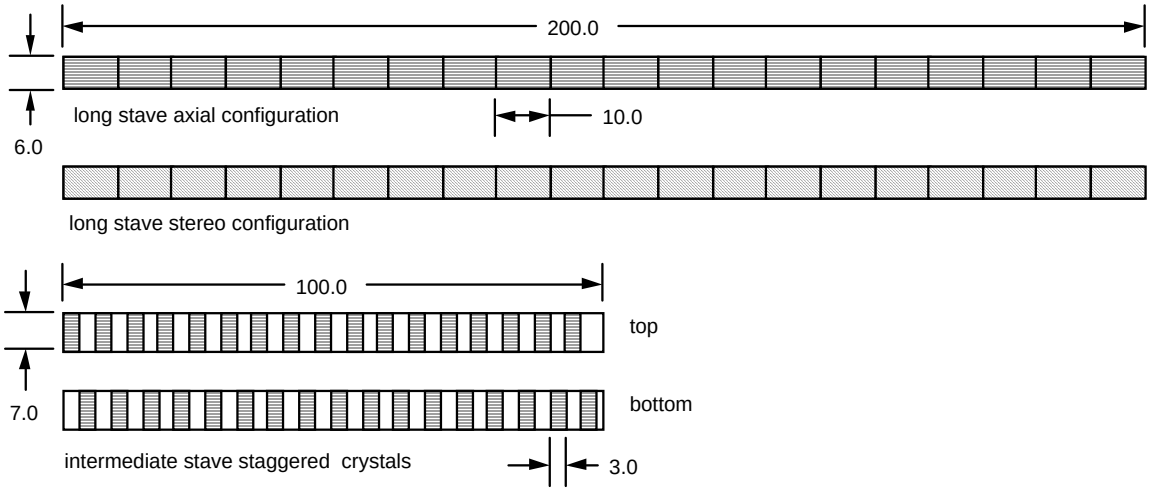


Figure 2: Concepts for long outer region stave (top) and intermediate region stave (lower). Hybrids are not show but are on silicon for long stave (as in test stave under study now) and adjacent to the silicon for the intermediate stave with gaps between crystals.

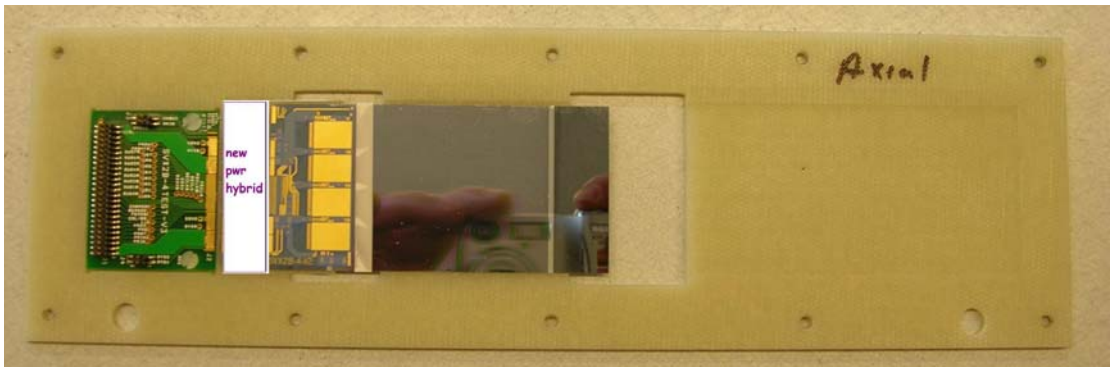


Figure 3: Scheme with new serial or DC-DC powering hybrid shown.

Report on Mechanical Activities

The description and plan for mechanical activities towards a 1 meter stave are in an accompanying report entitled:

ATLAS Upgrade
Stave Mechanical and Cooling Design Study

WBS 4.1.4.3

William O. Miller
Innovative Technologies International (iTi)
M. G. D. Gilchriese and C. Haber
Lawrence Berkeley National Laboratory

June 19, 2006

The budget for this activity is included below and in the report.

Plan for FY2007

The plan for FY2007 is to complete the FY2006 studies and build and test an ATLAS specific 1 meter stave.

1. Completion of FY2006 tasks
    a. Complete testing of serial powered "CDF style" stave. Most of this will occur in summer 2006
    b. Complete DC-DC converter chip and board, test on a "CDF style" stave
    c. Engineering studies on alternate powering reliability.
    d. Complete mechanical studies leading the 1 meter stave design.
    e. Complete software development around NI-6151 module in preparation for multi-module tests. Test this new system.
    f. Test and QA on detector order when it arrives from Hamamatsu.
2. Design and build electrical components for the 1 meter stave
    a. A six chip version of the ABCD hybrid, probably with integrated serial powering circuitry will be designed and built. A preliminary floor plan has already been made.
    b. A wider thin film fanout.
    c. Test fixtures, holders, and interface cards.
    d. A 1 meter version of the bus cable.
3. Design and build mechanical assembly and test fixtures for the 1 meter stave. (This is included in Bill Miller's plan and cost estimate.)
4. Design and build electrical assembly and test fixtures for the 1 meter stave.
    a. A fixture to test hybrids and detectors together
    b. A fixture to laminate the bus cable on the stave core
    c. A fixture to locate the hybrids on the stave
    d. A fixture to locate the detectors on the stave
    e. A fixture to hold the stave during wirebonding of hybrids and detectors
    f. A fixture to hold the stave during metrology and survey
    g. A test box including cooling and electrical feedthroughs.
    h. A storage and transport box.
5. Fabricate stave (mechanically) and survey (This is included in Bill Miller's plan)
6. Fabricate and test stave (electrically). Sufficient components will be on-hand to populate 3 staves.

End of FY2006 and FY2007 Schedule

Summer 2006:

- Assemble serial powering components and test on "CDF style" staves
- Continue DAQ software debug
- Continue mechanical design study
- Design 1 meter hybrid, fanout, and bus cable
- Design 1 meter stave mechanical assembly fixtures (Miller)
- Procure materials for 1 meter stave

Fall 2006

- Prepare and present papers at IEEE and Hiroshima meetings
- Fabricate 1 meter hybrid, fanout, bus cable, test fixtures
- Fabricate 1 meter stave mechanics and test.
- Design and fabricate electrical assembly fixtures for 1 meter stave
- Test DAQ for multimodules

Winter 2006-2007

- Test and QA on 3 cm detectors
- Assemble and test 1 meter stave hybrids and components
- Assembly and test 1 meter staves electrically
- Design work on 2 meter staves

Spring 2007

- Continue assembly and test of 1 meter staves
- Design work on 2 meter staves

Budget for FY2007
The totals are 170,246 (LBNL), 135,000 (BNL), 20,000 (Hampton), and 114,500 (Miller +LBNL mechanical effort) = $439,746

FY2007 development cost for ATLAS ID stave prototype 15-June-2006 Carl Haber
Phase 3
4.1.4.1.1
LBNL Section

	item	num	materials	total	hours	labor-cost	notes
1	**6 chip AC Hybrid**						
1.1	**substrate**						
1.1.1	BeO blanks	75	$25.00	$1,875			1
1.2	**thick film**						
1.2.1	CAD				150	$13,650	2
1.2.2	NRE	1	$6,000.00	$6,000			
1.2.3	printing	120	$600.00	$72,000			3
1.3	**fanouts**						
1.3.1	CAD				40	$3,640	2
1.3.2	mask	1	$1,500.00	$1,500			
1.3.3	fabrication	150	$125.00	$18,750			
1.3.4	dicing	150	$5.00	$750			
1.4	**components**						
1.4.1	discretes	1	$400.00	$400			
1.5	**assembly**						
1.5.1	surface mount	150	$75.00	$11,250			
1.5.2	bond chips	150	$75.00	$11,250			
1.5.3	misc assy,QC				25	$1,450	
1.6	**test**						
1.6.1	test PC adapter						
1.6.1.1	CAD				25	$2,275	2
1.6.1.2	fabrication	1	$3,000.00	$3,000			
1.6.2	misc fixtures				25	$1,900	
1.6.3	misc components	1	$1,500.00	$1,500			
1.7	**holders**	100	$50.00	$5,000			
2	**1 Meter Bus Cable**						
2.1	CAD				100	$9,100	
2.2	NRE	1	$500.00	$500			
2.3	parts	20	$400.00	$8,000			
3	**Interface card**						
3.1	CAD				25	$2,275	2
3.2	fabrication	1	$1,500.00	$1,500			
4	**Stave elect assbly**						
4.1	parts	1	$7,000.00	$7,000			
4.2	hybrid+det test fixt				25	$1,900	
4.3	cable lamination				25	$1,900	
4.4	stave mount fixt				80	$6,080	
4.5	stave bond fixt				80	$6,080	

4.6	test box				40	$3,040
4.7	storage box				25	$1,900
4.8	electrical assembly				160	$9,280
6	**Test box**	2	$700.00	$1,400		
7	**Student labor test**					$35,000
	total protoyping			$151,675		$99,470
	overhead		1.0600	$160,776		
	SUM			**$260,246**		
	est 2006 uncomm			**$90,000**		
	LBNL REQUEST			**$170,246**		

notes: 1. Substrates can contain more than one hybrid when printed
2. CAD includes work which can be applied to final design
3. Fabrication cost driven by quantity, ~factor 2 savings in production

rates	CAD rate 1	$91.00
	shops rate	$76.00
	junior tech	$58.00
	senior tech	$82.00

4.1.4.1.2 BNL Section

	item	num	materials	total	hours	labor-cost	notes
1	**Hamamatsu Short Strips**						
1.1	Order Remainder	1	$85,000.00	$85,000.0			
1.2	QA Testing	1	$5,000.00	$5,000.0			
2	**NewDaq Software Development**						
2.1	1/6 Engineering				320	$20,000	
3	**Stave Metreology**	1					
3.1	Optical system	1	$5,000.00	$5,000.0			
4	**2nd Stave Assembly**						
4,1	engineer	1			80	$5,000	
4.2	tech	1			160	$10,000	
4.3	fixtures	1	$5,000.00	$5,000.0			
Subtotal			$100,000.00	$100,000.0	560	$35,000.00	

TOTAL **BNL Request** **$135,000**

4.1.4.1.3 Hampton Section

1	cooling box		$5,000

2	daq modules			$5,000			
3	testing and fab effort					$10,000	
	subtotal			$10,000		$10,000	
	total			**$20,000**			

4.1.4.3							
Cooling Channels (Bill Miller Effort)							
4.1.4.3.1	**Stave materials**						
1.1	Pre preg	1	$17,500.00	$17,500			
1.2	Honeycomb	1	$4,000.00	$4,000			
4.1.4.3.2	**Stave design/eng**						
2.1	Engineering				300	$22,500	
2.2	Design effort				100	$3,500	
4.1.4.3.3	**Fixtures**						
3.1	Fixture fabrication	1	$25,000.00	$25,000			
4.1.4.3.4	**Assembly and test**						
4.1	Materials testing	1	$5,000.00	$5,000			
4.2	Assembly labor				390	$32,001	4
4.3	stability test fixture	1	$5,000.00	$5,000			
4.4	subtotals		$56,500.00	$56,500		$58,001	
TOTAL				**$114,500.50**			

rates	engineering	$75.00
	design	$35.00
notes	4. LBNL tech labor	

ATLAS Upgrade
Stave Mechanical and Cooling Design Study

WBS 4.1.4.3

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June 19, 2006

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FY 2006 Mechanical Engineering Tasks

The engineering plan for the ATLAS Upgrade Silicon Tracker separated into two natural phases, engineering analysis of the stave structure and prototype stave testing. During this fiscal year the focus was on structural analysis of the stave structure and thermal analysis of the embedded cooling system. Next year will focus on stave construction and testing. Our tasks planned for this year were:

- Prepare stave design layout for 1 meter length and width of 6.4cm
- Review material options for attaining structural stiffness (sag < 50 to 60 microns) using FEA modeling. Select composite materials best suited for the composite facing and the sandwich core material
- FEA model of the stave connection support to describe anticipated boundary restraint for the stave, i.e. to what extent the end close approaches a fixed support
- Using ATLAS evaporative cooling system as a baseline, establish what coolant temperature is required to provide a strip detector temperature of nominally -25ºC. Develop reasonable assurance that -30ºC inlet is not required to achieve the stated objective
- Using FEA model predict thermal strains for the stave structure, accounting for the effects of dissimilar CTE for the strip detector, hybrid, and composite materials. Predict strains for the operating chip heat loads and sub-cooling of the detector from room temperature to -25 ºC
- Calculate heat transfer coefficient for forced convective evaporative coolant in the stave embedded tubing
- Calculate pressure drop for the coolant passage within the stave proper (dual pass, entrance and exit both from one end of the stave)
- Review option of 2m stave length and propose an approach for longer and wider stave
- Develop plan for constructing stave prototype, detailing parts and design necessary fixtures

This effort was structured to lower the risk in the development stave prototype, an activity planned for FY2007. To accomplish this objective will require placing commitments for the long lead materials - composite pre-preg material and honeycomb for the sandwich core – by the September-October CY 2006 time frame.

Work Accomplished

2.1 Summary

The engineering effort has produced two stave designs; the principal design difference between the two concepts is the stave sandwich thickness. The first option, which has been analyzed more fully, has an overall thickness of approximately 6.1mm. For the first design a minimum inner separation between composite faces was chosen, nominally 4.6mm. A prototype tube of this size is not available, thus requiring procurement of a special coolant tube extrusion.

The second design option premise used an 8mm diameter aluminum tube to lower the cost of the prototype fabrication, since the extrusion stock is available. A slight reforming of this tube to flatten and improve thermal contact provides a separation between composite faces of 7.3mm (overall thickness of stave 8.8mm). The advantage of this design is a much stiffer stave. As a next step, we plan to bend the tube through a 180º arc without exceeding a 3.2cm radius of curvature. This will allow the tube to be placed optimally within the 6.4cm stave width.

A very slight difference in radiation length will exist between the two designs. Small increases are associated with increased honeycomb core height and coolant tube mass.

Gravity sag for the 8.8mm thick stave design, in the critical most horizontal position, appears to be well within our design goals.

The effective thermal performance of both tubes is quite similar. The smaller diameter tube has a lower convective film coefficient, but a higher heat flux than the larger tube cross-section. Effectively, the differences in convective film coefficients and tube surface heat flux balance out. In both tubes the low mass flow rate required to cool the 108W electronic chip load yields a very low two-phase flow velocity throughout the channel. This results in a predicted 3 to 4ºC temperature gradient for the forced convective cooling condition (evaporation) in either case.

We have selected all materials and material thicknesses of the various stave elements. K13D2U, a very high modulus, highly conductive graphite fiber oriented in 4/1 orientation has been selected for the sandwich facing. Material properties are based on a 60% fiber fraction. At this fiber fraction, the longitudinal tensile modulus, important to opposing gravity sag, is nearly twice that of steel. In spite of the fact that the longitudinal CTE in this laminate is very negative and not particularly well matched to the wafers and hybrids, thermal distortion for the 50ºC temperature change[1] is quite acceptable. Out-of-plane distortion of the silicon strip detectors is moderated by the near symmetry of the assembled unit.

A review of the 2m option was made. To limit gravity sag over this large span would require a large separation between stave sandwich facings. This potential solution complicates significantly the effective placement of a cooling tube. Our present approach is to provide a mid-span support, limiting the un-supported length to 1m. This essentially provides a compatible geometry for all staves, long or short, regardless whether the stave width is 6.4cm or 12cm.

2.2 Current Activities

Our current effort centers on identifying fixture needs to fabricate stave components and resolve assembly issues for a stave constructed from a stock cooling tube extrusion. The solid model under construction is shown in Figure 4. Precision pins are used at each end to support and align the stave in the over tracking assembly. Tooling concepts are being formulated for this 1st article; tooling design will provide precision alignment of the two stave ends, bonding the sandwich structure in steps to permit proper placement of the

[1] Sub-cooling the detector from room temperature to -25ºC.

cooling tube and end caps. A preliminary plan for accomplishing these tasks is under review.

Figure 5 illustrates the nominal 1m stave assembly that will be constructed as a first article.

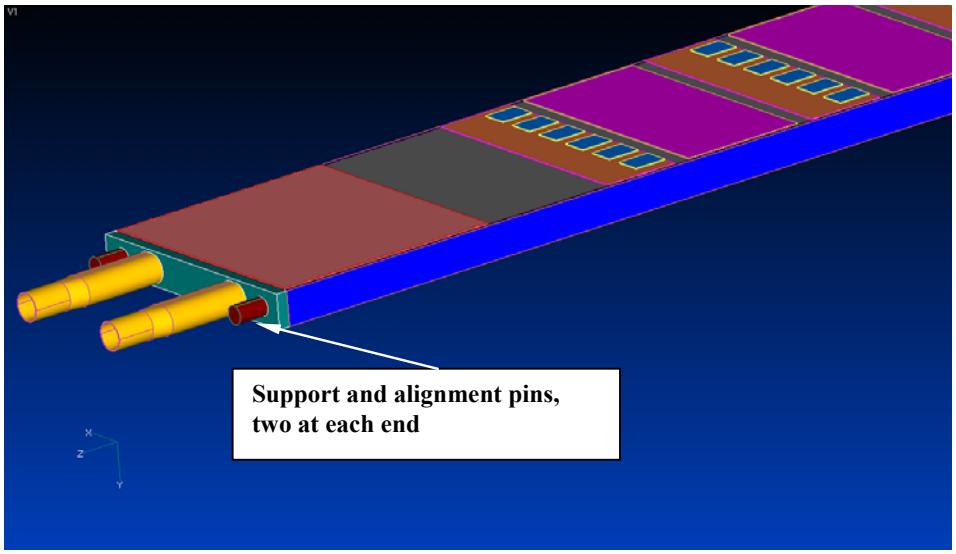


Figure 4: Solid model rendering of a stave constructed using an 8mm diameter aluminum tube that has been reformed to enhance thermal transport area.

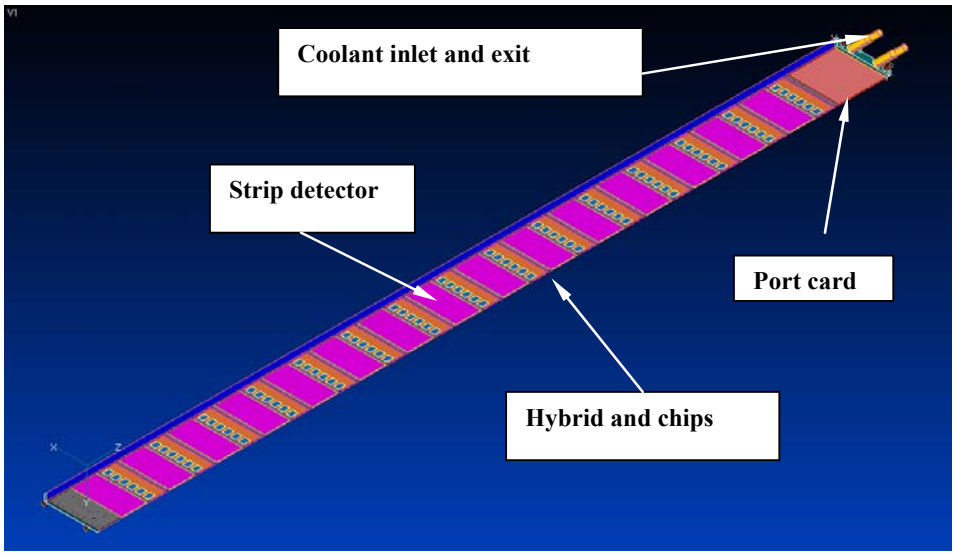


Figure 5: View of overall stave depicting strip detectors, hybrids and chips. The assembly comprises 15 strip detectors with a length of with a length of 993.5mm exclusive of the end caps and pin extension.

2.3 Overview of Specific Results

We present here a brief overview of some of the modeling that has been completed, which is input to the detailed design of the 1m stave prototype and the associated tooling. As described, the inner stave will be (typically) 1 meter and the outer stave (typically) 2 meters long. These staves will be supported by discs at some (minimum) number of locations e.g. about 1m apart. The gravitational sag and stability of the stave must be controlled as determined by performance and interference specifications. Using mechanical design and FEA methods the geometrical and physical (sag, resonance frequency, thermal properties) parameters of staves models were studied and determined. These results will be input to the design of full-scale, 1m, stave prototype.

2.3.1 Gravity Sag and Core Shear Properties

Detailed mechanical and thermal modeling of the stave structures and their connections to supporting bulkheads are already underway. The initial work has concentrated on modeling of the short stave, approximately 1 m long. The model includes all of the components of the stave – detectors, hybrids, electronics, bus cable, composite supports, cooling tubes, and closeouts. Studies of gravitational deflections (sag) are underway with various assumptions on the geometry and supporting boundary conditions. An example of a finite-element model of the maximum gravitational deflection for a 96 cm long stave is shown in Figure 6 . We propose to control gravity sag by preferentially orienting most of the stave composite fibers along the stave axis. For the illustrated solution, 4 times as many fibers are placed in the longitudinal direction as in the lateral, achieving tensile modulus greater than steel.

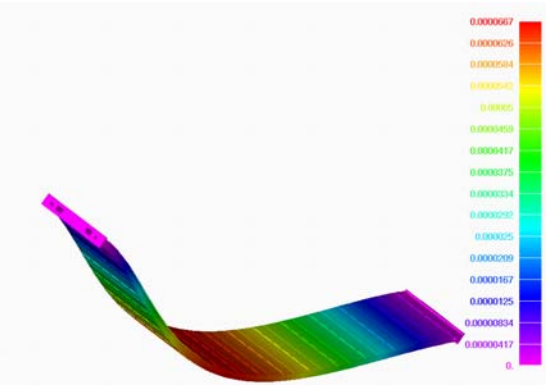


Figure 6: NASTRAN solution for stave gravity sag with aluminum cooling tubes. Distortion scale is in meters, with peak resultant distortion of 66.7µm; essentially all deflection is in the Y-direction, normal to the stave.

Honeycomb and carbon foam were evaluated as core material options as part of the FEA effort. From the standpoint of minimizing installed mass, there is an optimum core shear modulus to satisfy sandwich stiffness. Beyond a certain value, there is a diminishing return with respect to increasing core shear modulus for the purpose of reducing gravity sag. In absence of a cooling tube, the design problem becomes a rather simple. However in the stave case, the cooling tube divides the core into three separate

compartments, one central region and two outer regions. Most of the space for bonding core material is contained in the central region.

Throughout the initial FEA study, the cooling tube structurally interacted with the stave composite faces, contributing to core shear. Table 1 summarizes these results, in terms of two core materials, core thickness and two core heights. To assess the contribution that core material contributes to radiation length, an "equivalent thickness" was calculated. For this value the core material was assumed to be spread over the 6.4cm width of the stave.

Regardless of the core material, increasing core shear modulus with the cooling tube coupled structurally did not produce the desired effect; predicted sag increased slightly. It appears that the added core mass increased was responsible.

Table 1: Summary of FE Solutions Crediting Two Contributions to Core Shear Stiffness, Aluminum Tube in Conjunction with Indicated Core Options.

Carbon Foam Core Shear Modulus (MPa)	Foam Density (kg/m^3)	Stave Central Deflection (1G loading)	Foam Radiation Length (%)	Equivalent Foam Radiation Length (mm)
		Half Length Model		
		Separation between facings -5.88mm (equivalent t=4.48mm)		
26.8	**66**	**62.1**	**.069**	**6470**
34.4	**110**	**63.9**	**.115**	**3882**
229.7	**210**	**65.1**	**.221**	**2033**
		Full Length Model (96cm)		
		Separation between facings -4.61mm (equivalent t=3.15mm)		
26.8	**66**	**53.7**	**.049**	**6470**
34.4	**110**	**54.7**	**.081**	**3882**
229.7	**210**	**54.8**	**.155**	**2033**

Honeycomb Core Shear Modulus (MPa)	HC Density (kg/m3)	Stave Central Deflection (1G loading)	Foam Radiation Length (%)	Equivalent HC Radiation Length (mm)
		Half Length Model		
		Separation between facings -5.88mm (equivalent t=4.48mm)		
626/337 (resin)	**56**	**58.7**	**0.059**	**7611**
1551/710 (CC)	**160**	**61.6**	**0.168**	**2669**
		Full Length Model (96cm)		
		Separation between facings -4.61mm (equivalent t=3.15mm)		
626/337 (Resin)	**56**	**50.1**	**0.046**	**7611**
1551/710 (CC)	**160**	**51.7**	**0.168**	**2669**

A solution was made for the 1m length stave (4.61mm separation) with honeycomb core (626/337 resin) where the tensile modulus of the aluminum cooling was set essentially to zero. This solution uncouples the cooling tube structurally; a condition that a compliant, thermally conductive adhesive that joins the cooling tube may produce. Sag measurements on the stave prototype will assess to what extent this decoupled state exists; our prior experience has shown that the ATLAS Pixel thermostructures do experience structural coupling to some extent, albeit not very well documented. For this stave solution the gravity sag became 57.3μm (as opposed to 50.1μm). At this juncture, we concluded it best to proceed with the honeycomb option, since the carbon foam

density needed to provide this level of shear modulus is quite dense, resulting in an undesirable radiation length penalty.

2.3.2 Gravity Sag and Stave Pin Support Design

Each stave will engage the primary support disks with pins, two at each end. A thin stave profile limits the diameter of the pins to some extent, although some flexibility can be provided by making the end caps larger. Stave end caps slip in between the two composite facings, providing a ledge for bonding. Precision receiver holes are provided in the end caps for the small diameter solid pins. At the present, aluminum has been chosen for the end caps and steel for the pins. Since radiation length does not favor steel, the pins were kept small. FEA solutions for the 6.1mm thick stave (4.61mm separation) did include an assessment of the effect of beryllium parts and two distinct pin diameters. Solutions were made for 0.125in, 0.173in, and 0.25in diameter, with 0.173in diameter being choice for most of the solutions when other structural parameters were varied.

For 4.39mm diameter pins and aluminum end caps the gravity sag is 50.1μm (honeycomb core), as compared to 44.9μm, an 11.6% improvement. The gain provided by the higher modulus elasticity of beryllium, 45Msi versus 10Msi for aluminum, does not offset the hazards incurred through its use.

As we progress into the detailed design of the stave with the 8mm diameter cooling tube the end cap and pin geometry will undergo some change. One option considered briefly was to make the end cap from composite material, providing a closer CTE match to the facings and a lower radiation. Steel will be retained for the pins, but it may be possible to use a hollow pin instead of solid.

2.3.3 Pin End Support Boundary Conditions

In practice the pins at the stave ends fit into precision receivers, following a kinematical sense. Two pins at opposite ends and in line will slide into precision holes. This boundary condition fixes the stave normal to its axis and azimuthally for any orientation. The second pin at either end must slide into a slot so as not to over constrain an in-plane thermal dimensional change. A restraint in Z (stave axial direction) is required for static stability in the FE model. A number of solutions were made first using Z restraint at one end for both pins. Had the opposite pins been fixed in Z also, the condition would have simulated in-plane traction restraint, similar to fixed-end beam conditions. Later, to make the sag symmetrical about the stave midpoint, nodes at mid-span were fixed. The result was a slight difference (increase) in sag, not entirely unexpected.

With reference to Table 1, the Z-restraint for the pins was both fixed at one end. Removing this restraint and fixing nodes (Z) at mid-span of the stave increased the sag 11%, not significantly but noticeably. For example, the solution for carbon foam, 53.7μm increased to 59.4μm.

We are sensitive to the fact that our solutions are influenced to some degree by the uncertainty of the pin boundary conditions. However, it is felt that the method of allowing freedom of the pins to slide provides some contingency against aspects

presently unknown. During installation, one pin maybe clamped[2] to set the Z-axis, but clamping both pins at one end is not acceptable for kinematic reasons.

2.3.4 Cooling of 1m Stave

Studies of distortions that result from mismatch in thermal properties of the various materials comprising a stave have been initiated using a 32cm stave section. Cooling the assembly from room temperature to -25ºC is used to quantify this effect. The results indicate that distortions are within an acceptable range, largely due to the stave detector elements being mounted on both sides, albeit with a shift to provide the desired strip coverage. A distortion pattern tracking the above and below alternating strip and hybrid placement is evident in Figure 7.

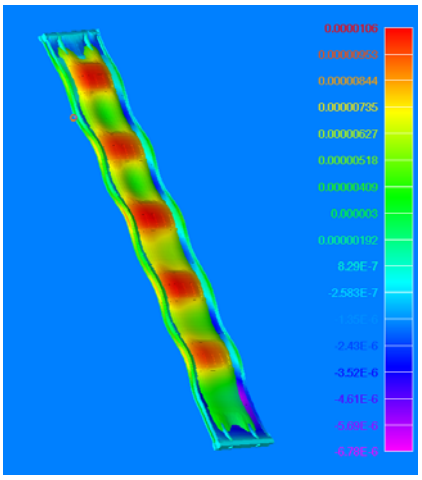


Figure 7: Thermal strain solution for 50ºC temperature change (room temperature to -25ºC), with aluminum cooling tube. Alternating detectors above and below on the stave produces a low amplitude cyclic pattern (10.6microns). Stave composite facings are constructed with 4 to 1 fiber orientation.

Stave cooling is accomplished by a dual pass evaporative cooling circuit, located between the stave composite facings. Cooling entrance and exit for the 96cm stave model occurs at one end, forming a long U-shaped passage between the stave composite facing. Preliminary thermal solutions have been made for both aluminum and PEEK coolant tube materials using the short 32cm stave section (Figure 8). Enhancing the lower thermal conductivity PEEK[3] material with carbon-fibers produces acceptable thermal performance, although an aluminum tube provides the best performance by a noticeable amount. The difference in peak chip temperature between the two materials is ~4 ºC, with nearly the same difference in strip detector temperature. In each case, the coolant reference temperature is -25ºC but there is no temperature gradient along the direction of the coolant flow in this model. The temperature difference between the reference temperature and the silicon detectors is less than about 3°C (5°C) for the aluminum (carbon-filled PEEK) coolant tubes. Sag is substantially lower with aluminum tubes.

[2] May be difficult.
[3] Unfilled PEEK produces a significant thermal gradient

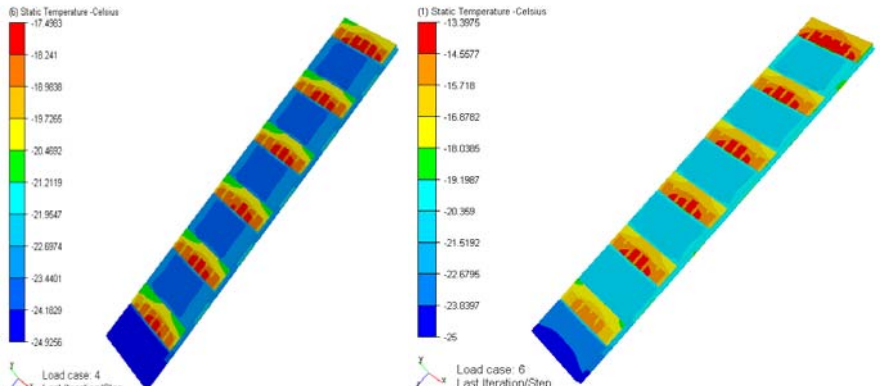


Figure 8: Comparison between Aluminum and carbon-fiber filled PEEK cooling tubes using the 32cm long stave model. Each chip is dissipating 0.5W. Chips are mounted on a BeO hybrid

2.3.5 Two Meter Stave Length

An assessment of a 2m stave, supported at its two extreme ends with fixed end conditions, was made using a classical analytical method and shear modulus properties extracted from the 1m stave analysis. The analytic method solves for shear and bending deflections separately. The assumed fixed end conditions, not at all kinematic, limits the gravity sag to roughly 90μm for a core height of 20mm. One may recall for a kinematically mounted 1m stave, the gravity sag was <60μm with a core height of 4.6mm, and the 7.33mm height being <<60 μm.

It is conceivable to pose an internal core configuration for a 20mm core height that limits shear deflection. The problem becomes integration of the cooling tube. It is no longer possible to cool both surfaces of the stave with a single cooling tube. No ready solution solves this complication without additional tubing or internal heat collectors to route the dissipated electronic heat to a centrally mounted tube. We propose a more direct solution to be providing a mid-span support for the 2m stave. This decision provides the obvious benefit of making the stave structural geometry universal for both short and long staves.

One 2m stave configuration under study is 12cm wide, as opposed to the 6.4cm wide version for which thermal studies have been substantially completed. At this time we do not seem any obstacle to the simple two-pass cooling embedded cooling tube working for both stave widths.

Proposed Plan for Mechanical Study FY2007

The activities planned for the coming fiscal year are:

- Fabricate tooling fixtures needed to assemble a 1m by 6.4cm width stave
- Procure raw materials for the stave structure, pre-preg, honeycomb, etc.
- Consolidate K13D2U/Cyanate ester laminate with 4/1 fiber orientation
- Conduct material specimen testing to verify laminate fiber fraction and tensile modulus properties
- Conduct thermal diffusivity measurements of facing material to confirm thermal conductivity through the laminate wall
- Measure transverse (in-plane) laminate thermal properties
- Prepare assembly procedure for bonding and curing stave structure

- Bond and assemble 3 staves, one for mechanical testing (4 point bend test to determine sandwich shear properties)
- Assemble cold box facility for thermal stability testing (-25ºC)
- Conduct thermal stability tests measuring out-of-plane distortion with LBNL TV Holography equipment or optical measurements
- Measure gravity sag using coordinate measuring equipment

Budget

The budget for engineering design, materials, fixture fabrication and labor (skilled mechanical technician familiar with composite fabrication) is given below. The tooling design will by done by iTi, with the collaboration of a senior technician from LBNL that has extensive experience in the fabrication of composite structures for ATLAS. It is not yet decided if the fixtures will be fabricated commercially (under the direction of iTi) or at LBNL. LBNL will procure the prepreg, honeycomb and other materials. Material testing will be done commercially. Fabrication of the stave components will be done at LBNL and utilize equipment there – automated cutting and an autoclave. Finally assembly of the stave prototypes will be done at LBNL. It is anticipated that LBNL will provide additional senior technical labor (0.3 FTE, S. Dardin and M. Cepeda or J. Wirth) supported by base program funds for the implementation of fixtures, assembly of the stave components and staves and preparation of fixtures for stability measurements. LBNL will provide measurement capability (TV holography, optical measuring machines and CMM).

Pre-Preg (K13D2U 10bs plus set up) Bryte Technologies……..$17,500

Honeycomb (UCF-119-3/16-3.5, ~3 staves)…….$ 4000

Consulting (iTi): Senior Engineer…….300hrs @$75/hr……$22,500

Designer…….100hrs @$35/hr……$ 3,500

Fixture Fabrication: 4 precision bonding fixtures…….$25,000

Material specimen testing……..$ 5,000

LBNL Tech Labor to assemble fixtures and make staves…….…$32,000

Fixtures for stability measurements.....$ 5,000

TOTAL $114,500

FY2007 development cost for ATLAS ID stave prototype 15-June-2006 Carl Haber							
Phase 3							
4.1.4.1.1							
LBNL Section							
	item	**num**	**materials**	**total**	**hours**	**labor-cost**	**notes**
1	**6 chip AC Hybrid**						
1.1	**substrate**						
1.1.1	BeO blanks	75	$25.00	$1,875			1
1.2	**thick film**						
1.2.1	CAD				150	$13,650	2
1.2.2	NRE	1	$6,000.00	$6,000			
1.2.3	printing	120	$600.00	$72,000			3
1.3	**fanouts**						
1.3.1	CAD				40	$3,640	2
1.3.2	mask	1	$1,500.00	$1,500			
1.3.3	fabrication	150	$125.00	$18,750			
1.3.4	dicing	150	$5.00	$750			
1.4	**components**						
1.4.1	discretes	1	$400.00	$400			
1.5	**assembly**						
1.5.1	surface mount	150	$75.00	$11,250			
1.5.2	bond chips	150	$75.00	$11,250			
1.5.3	misc assy,QC				25	$1,450	
1.6	**test**						
1.6.1	test PC adapter						
1.6.1.1	CAD				25	$2,275	2
1.6.1.2	fabrication	1	$3,000.00	$3,000			
1.6.2	misc fixtures				25	$1,900	
1.6.3	misc components	1	$1,500.00	$1,500			
1.7	**holders**	100	$50.00	$5,000			
2	**1 Meter Bus Cable**						
2.1	CAD				100	$9,100	
2.2	NRE	1	$500.00	$500			
2.3	parts	20	$400.00	$8,000			
3	**Interface card**						
3.1	CAD				25	$2,275	2
3.2	fabrication	1	$1,500.00	$1,500			
4	**Stave elect assbly**						
4.1	parts	1	$7,000.00	$7,000			
4.2	hybrid+det test fixt				25	$1,900	
4.3	cable lamination				25	$1,900	
4.4	stave mount fixt				80	$6,080	
4.5	stave bond fixt				80	$6,080	
4.6	test box				40	$3,040	
4.7	storage box				25	$1,900	

4.8	electrical assembly				160	$9,280	
6	**Test box**	2	$700.00	$1,400			
7	**Student labor test**					$35,000	
	total protoyping			$151,675		$99,470	
	overhead		1.0600	$160,776			
	SUM			**$260,246**			
	est 2006 uncomm			**$90,000**			
	LBNL REQUEST			**$170,246**			
notes:	1. Substrates can contain more than one hybrid when printed						
	2. CAD includes work which can be applied to final design						
	3. Fabrication cost driven by quantity, ~factor 2 savings in production						
	CAD rate 1		$91.00				
	shops rate		$76.00				
	junior tech		$58.00				
	senior tech		$82.00				
4.1.4.1.2							
BNL Section							
	item	**num**	**materials**	**total**	**hours**	**labor-cost**	**notes**
1	**Hamamatsu Short Strips**						
1.1	Order Remainder	1	$85,000.00	$85,000.0			
1.2	QA Testing	1	$5,000.00	$5,000.0			
2	**NewDaq Software Development**						
2.1	1/6 Engineering				320	$20,000	
3	**Stave Metreology**	1					
3.1	Optical system	1	$5,000.00	$5,000.0			
4	**2nd Stave Assembly**						
4,1	engineer	1			80	$5,000	
4.2	tech	1			160	$10,000	
4.3	fixtures	1	$5,000.00	$5,000.0			
Subtotal			$100,000.00	$100,000.0	560	$35,000.00	
TOTAL	**BNL Request**			**$135,000**			
4.1.4.1.3							
Hampton Section							
1	cooling box			$5,000			
2	daq modules			$5,000			
3	testing and fab effort					$10,000	
	subtotal			$10,000		$10,000	

	total			**$20,000**			
4.1.4.3							
Cooling Channels (Bill Miller Effort)							
4.1.4.3.1	**Stave materials**						
1.1	Pre preg	1	$17,500.00	$17,500			
1.2	Honeycomb	1	$4,000.00	$4,000			
4.1.4.3.2	**Stave design/eng**						
2.1	Engineering				300	$22,500	
2.2	Design effort				100	$3,500	
4.1.4.3.3	**Fixtures**						
3.1	Fixture fabrication	1	$25,000.00	$25,000			
4.1.4.3.4	**Assembly and test**						
4.1	Materials testing	1	$5,000.00	$5,000			
4.2	Assembly labor				390	$32,001	4
4.3	stability test fixture	1	$5,000.00	$5,000			
4.4	subtotals		$56,500.00	$56,500		$58,001	
TOTAL				**$114,500.50**			
	engineering		$75.00				
	design		$35.00				
notes	4. LBNL tech labor						

WBS 4.3

US-Atlas LAr Calorimeter Upgrade R&D for FY07 and Status Report for FY06

The US-Atlas LARG Group

1. Overview

Here enclosed are the proposal of activities and fund request for FY07 of the U.S. ATLAS Liquid Argon calorimeter R&D in view of a possible high luminosity LHC upgrade. The proposal follows a similar document [1] and R&D plan submitted last fiscal year and carried out by a collaboration between the following U.S. institutions:

- Southern Methodist University, Dallas, TX
- Columbia University – Nevis Lab, New York, NY
- Pittsburgh University, Pittsburgh, PA
- State University of New York at Stony Brook, Stony Brook, NY
- University of Arizona, Tucson, AZ
- Brookhaven National Laboratory, Upton, NY

These institutions collaborated successfully in the past several years in the construction of the ATLAS Liquid Argon (LAr) detectors and of their readout-electronics, as well as in the installation and commissioning phase that is currently ongoing. They proved to have successfully established good communication, collaborative spirit, and responsibility sharing among them and they are expected to develop the same sort of effort for this R&D program. In addition to the US groups we are collaborating with non US groups on different aspects of the R&D. In particular we have close collaborations with Milano, Orsay, and Annecy, Triumf and other Canadians universities among others.

During FY06 the US-Atlas LAr collaboration has grown thanks to several new collaborators joining the R&D efforts and being interested to some of the already existing R&D plans:

- University of Arizona: 1 faculty and 1 engineer joined the existing LAr group in Arizona and expressed interest on the next generation ROD development. (WBS 4.3.4)
- University of Pennsylvania joined the LAr R&D effort with 4 scientists who expressed interested in developing analog Front-End in SiGe technology (WBS 4.3.2.2)

The individual proposals included in this document address several issues for LAr calorimetry related to an increase in luminosity by a factor 10 over the present design luminosity (10^{34} $cm^{-2}s^{-1}$). CERN management is planning to upgrade the LHC collider on a time-scale of 2013-2014 (ready for commissioning) and recommended that the experiments start organizing for this. Within ATLAS, a High Luminosity Steering Group has been operating since June 2004 with the purpose of defining goals, guidelines, and layout of a work plan for all the subsystems.

Although the details of machine upgrades will probably not be finalized before 2007 it has been generally acknowledged that R&D activities needed to start as soon as possible given the long lead time (>5 yrs) required by several elements.

A possible timeline is summarized in the following table:

Table 1: LAr R&D Upgrade Roadmap

R&D activities	2006-2009
Final Design decision	2010
System Tests	2009-2011
Production	2011-2013
Installation	2014

The LAr Calorimeters will be affected by a higher luminosity environment in different ways, classified in two main categories, related either to the operation of the detectors [2] or to the performances and characteristics of the readout electronics [3]:

- *Detector issues:*
  - Increased radiation leading to possible break down of the charge collection in LAr (particularly severe in the end-cap region for high values of the pseudo-rapidity η).
  - Radiation induced poisoning and layer build-up effects on the readout electrodes that would reduce the charge collection efficiency and ultimately the detector performance.
  - Direct activation of the LAr that would increase the calorimeter noise level (compared to the electronics noise) and would have possible implications for safety in case of leaks.
  - High Voltage (HV) degradation depending on the HV distribution uniformity among the different calorimeter sections and on the average DC current draw due to the higher ionization rate in the active gaps. It may require new HV power supplies as well as a redesign of the HV protection resistors and feedthrough filter circuits.
  - Beam heating of LAr: the problem would be particularly severe in the Forward Calorimeters (FCAL). At the upgraded luminosity the heat dissipation would be 400 Watts in the FCAL detectors. Preliminary calculations foresee an 11^{o}C difference between beam on and off at an operating pressure where the difference between the freezing and boiling temperature is 9^{o}C. Operating the detector in such conditions would be extremely difficult if not impossible.

- *Readout Electronics issues:*
  The current readout is based on a complex architecture with 13 different technology ICs (COTS, and DMILL, DMS and AMS ASICs) and a total of 20 different voltage regulators. A block diagram of the readout is depicted in Fig. 1.

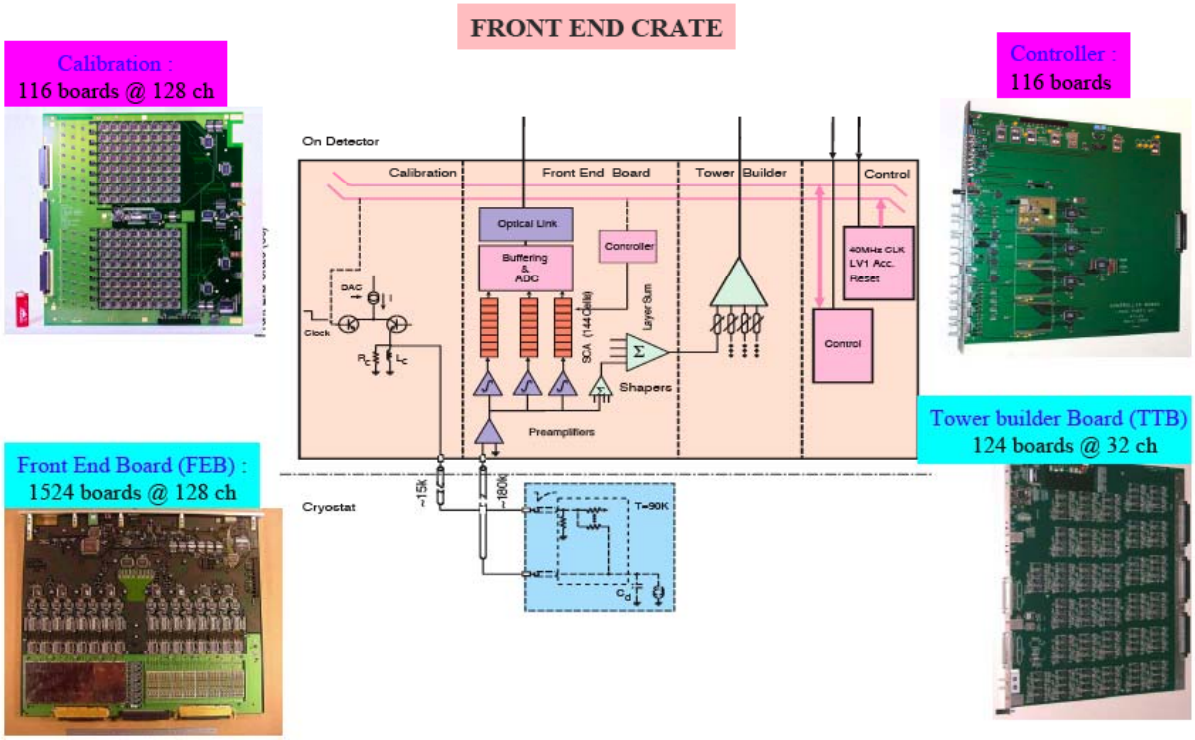


Figure 1: Current LAr Calorimeter readout architecture

- Each component has been qualified for 10 years operation at nominal LHC luminosity with safety factors of 35/10/10 for total ionization dose (TID), non-ionization energy losses (NIEL) and single-event effects (SEE). Some components started to show some degradation at high end implying that they will probably not qualify for 10 years operations at $10^{35}cm^{-2}s^{-1}$.
- In-situ radiation monitoring will be important to determine how large the safety margins are.
- Reliability/Lifetime of the components are also not well known. There are some worries about DMILL and DSM ICs for which some extended lifetime tests are already planned with the current pre-production series readout boards.
- Most components (in particular DMILL ASICs) cannot be replaced if they start failing. Furthermore, it would be difficult if not impossible to upgrade only a few components in the current system given the evolution of technologies, changes in the required voltages etc.

The need of an upgraded readout implies a redesign of the front-end boards, the power supply system, the back-end electronics and the level-1 (L1) trigger interface. Thus all boards in the front-end crates (calibration, tower builder and controller boards) would have to be redesigned. It is mandatory however that any upgrade of the LAr readout electronics will be as adiabatic as possible: in particular no change in the infrastructures (pedestals, crates, base-planes and interface to the cooling system).
To limit all the different options, this collaboration decided to adopt as the baseline for an upgraded layout the architecture depicted in Fig. 2: preamplifier, shaper and gain selection mechanism possibly integrated in a single ASIC, and high bandwidth optical links to transmit the digitized signals to the back-end modules reconstructing the energy deposited in each readout cell. Layer sums from each Front-End board would also be digitized locally and sent out to the L1-interface through optical links.

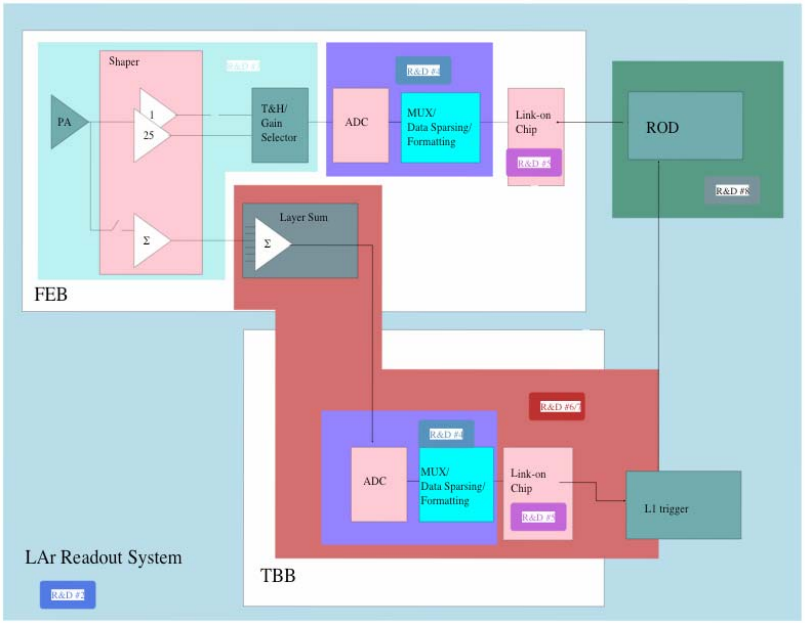


Figure 2: Proposed baseline architecture for the LAr calorimeter readout upgrade

Alternative readout architectures can not be excluded at this stage and should be considered in particular in the event of future technology breakthroughs (and it is for this reason that the roadmap in table 1 indicates FY10 as a target to freeze the architecture design). Indeed a possible alternative to transmit the L1-trigger information has been considered where the ROD modules will also form digital sums and send them to the L1 processor farm.

2. Summary of the R&D status, proposals and requests

Hereafter the status of the LAr R&D activities will be shortly reviewed together with summary tables for the FY07 funding requests.
The R&D activities proposed represent the interests expressed by the collaboration. They address uniquely and coherently several of the issues presented in the Overview Section. The report and the FY07 requests are deeply based on a "baseline"- document submitted last summer [1] to the US-Atlas management and approved limitedly to the FY06 activities. Adjustments to such a baseline have been taken into account and included in the plan during the past year for the reasons and with the methods that will be described extensively in each proposal.

1st U.S. Atlas workshop on LAr R&D Upgrades
The US-LAr collaboration held a first workshop on the upgrade R&D at SMU, Dallas on March 30th and 31st. Agenda, topics of discussions and individual presentations are available at the following URL: http://agenda.cern.ch/fullAgenda.php?ida=a06978.
The workshop has been organized into two sessions: the first one reporting the progresses on each individual activity, aimed at verifying the status of the R&D programs, the overall coherency of the developments as a system and a preliminary discussion of the interfaces among the different components. A second session was of general discussion and future organization and strategy within the US-Atlas and within Atlas-LARG collaborations. A discrete attendance by US institutions and universities as well as by few European colleagues allowed to strengthen the fruitful relationship among the existing collaborators and allowed few more people to express their interests in participating to the developments.

New ideas and possibilities have been exchanged and considered for next FY plans.

Status of the R&D activities

Availability of the funds in FY06 came to most institutions involved significantly late (Mar to May 06) in some cases. Nevertheless all the activities started successfully their programs, and achieved preliminary results, of some relevance in few cases.
This was possible in some cases by anticipating the activity needs through other funded grants and are in a need of returning whatever has been borrowed.
In other cases activities and milestones were reprioritized and reassigned to adjust dynamically for the late availability: an example is 4.3.2.3 where some radiation testing has being delayed by a few months while higher priority was given to the design of the "full-slice" board to test dataflow issues. In other cases recent technology advancements encouraged us to review or enlarge the scope of the R&D plans: an example can be found in 4.3.4 where recent progresses in communication systems (e.g. ATCA communication system) would boost the performances of the signal processing in the ROD and DAQ systems.
While the homogeneity and uniformity of the advances in each activity can't be entirely assessed as of today it we are convinced that the pace and the achievements reached so far are fully consistent with the goals and milestones proposed in last year's "baseline"-document. We don't believe that delays in fund assignments have impeded or impacted significantly the R&D project nor justify carryovers of FY06 funds in FY07. We would rather consider what WBS activity can be temporarily suspended to prioritize programs and better allocate limited resources and manpower.

Collaboration with non-US institutions

For some of the activities collaborations with non-U.S. institutions will be developed in the next few years and these will be specifically mentioned for those cases where such an interest has been already expressed. While is generally acknowledged that our collaborators in Europe are not ready yet to commit financially to a dedicated R&D program for the LAr upgrade is certainly true that:

i. Attendance at the Dallas workshop by few of our key collaborators in Europe is a proof of their interests to follow closely our activities. At the workshop representative of IN2P3, MPI-Germany and CERN were actually present and expressed interests to form up working groups within the existing Atlas-LARG collaboration and participate actively. IN2P3 has a nation-wide pool of engineers seriously involved in ILC R&D who is also interested or partly interested to join R&D projects for s-LHC

ii. In some respects ours is a leading effort that motivates others to get prepared and start internal discussion and organizational plans. An example of this is the recent 1-day workshop (6/07/06) within Atlas-France with 2 contribution on LAr upgrades where lots of references were made to efforts described in this document

iii. IN2P3 at LAL-Orsay, CNM-Barcelona are joining an Atlas-wide collaboration across the LARG and ID subsystems aimed at the development and characterization of SiGe ASICS in different processes and topologies.

iv. There is an international active collaboration among Atlas-LARG institutions aiming at establishing limits on the operation of the Atlas EndCap and Forward calorimeter at the sLHC. Their R&D program is being funded mainly through the CERN-INTAS structure and several institutions (i.e. BINP, IHEP, JINR from Russia, Univ. of Arizona in the US, Mainz, MPI-Munich, Wuppertal from Germany) are involved.

Organization of the Document and FY07 Summary Requests

The proposal is structured in sections each corresponding to the WBS organized last year. Each section will include a brief report on the activities accomplished in FY06 followed by a specific

request for FY07. Wherever is the case differences from the original plan - as proposed in the baseline document submitted last year – will be detailed. Only WBS with fund requests will be reported.

The following two tables summarize the requests for FY07. Table 2 specifies the requests by WBS (level 3 and 4) with cost breakdown between material, resources and manpower allocation, while Table 3 summarizes the total requests of funds by Institutions or Organization. Table 2 reports also the differences between the FY07 requests as originally laid out in the 2005 "baseline"-document – here briefly reviewed and summarized:

- WBS 4.3.2.2: funding requests have been reorganized and redistributed among different collaborators. In the baseline document there were no requests for radiation testing which has been now considered necessary.

- WBS 4.3.2.3: it is acknowledged by the collaboration that the development of a rad-hard ADC has a non-negligible risk factor. Higher priority and better engineering support should be provided to address and this issue.

- WBS 4.3.2.4: Justification of the request increase with respect to the "baseline"-document relies on a more detailed understanding of the engineering needs to design, develop and test the LoC chip. First radiation test on the SoS technology points out the necessity of better understanding of the radiation induced side leakage current and researches for ways to mitigate this effect. The plan is to adapt the enclosed layout transistors (ELT) technique that has been proved to be effective in eliminating this leakage current in 0.25 micron bulk CMOS technologies. More studies will be needed to understand how to simulate the ELT in the standard Cadence tool.

- WBS 4.3.3.1: we would like to investigate an alternative solution to the L1-trigger that falls more naturally within 4.3.4. For this reason the original request for FY07 has been put on hold and partly transferred to 4.3.4.

- WBS 4.3.3.2: an internal decision was made to hold the requests for FY07 because we feel would impact resources and manpower allocated for WBS 4.3.2.2:.

- WBS 4.3.4: the possibility of implementing the ROD system using the "AdvancedTCA" architecture, that is assuming in the last couple of year a role of new *de-facto* standard in the Tele-Communication and Embedding Computing system, would allow for fast ROD to ROD communication eliminating the limitations intrinsic to the VME based systems. This would let also study the feasibility of implementing L1-trigger sums information at the ROD level – if the latency budget will allow for.

References

[1] The US-Atlas LAr Coll.: *US-Atlas Liquid Argon Calorimeter Upgrade R&D for FY06*-FY08, proposal submitted July 2006.

Table 2: Budget Request Summary by Activities

WBS	Description	Inst.	Resources FY 07 as From Baseline Proposal of last year			Resources FY 07 - Updated Request			
			Material	Manpower	**TOTAL**	Material	Manpower	FTE Descr.	**TOTAL**
4.3	**Liquid Argon Upgrade R&D**				**1040.20**				**1237.50**
4.3.1	**Layer Buildup due to radiation**	Arizona	46.00	39.00	**85.00**	37.00	48.00	Tech	**85.00**
4.3.2	**Readout Electronics**								
4.3.2.1	Study of System Architecture	BNL	0.00	0.00	**0.00**	0.00	0.00		**0.00**
4.3.2.2	Analog Front-End in SiGe	BNL	85.00	100.00	**185.00**	95.00	100.00	0.5 Tech + 0.25 Eng.	**195.00**
		SUNYSB				19.00	6.00	0.1EE	**25.00**
		UPENN				13.00	47.00	0.2EE + 0.5Stud	**60.00**
4.3.2.3	Digital Readout System	Nevis	100.00	188.00	**288.00**	70.00	262.00	1.5 Tech + 1 Eng	**332.00**
4.3.2.4	Optical Data Link	SMU	68.20	89.00	**157.20**	78.40	155.90	0.8 Eng + 2.4 Stud.	**234.30**
4.3.3	**L1 Trigger**								
4.3.3.1	L1 Trigger Interface	BNL	35.00	0.00	**35.00**	0.00	0.00	0	**0.00**
4.3.3.2	Analog Optical Link for L1 Trigger	BNL	30.00	0.00	**30.00**	0.00	0.00		**0.00**
4.3.4	**ROD**	BNL	70.00	40.00	**110.00**	77.10	48.00	0.35Eng	**125.10**
		Arizona				18.50	12.60		**31.10**
4.3.5	**Radiation Hard LVPS**	BNL	60.00	90.00	**150.00**	60.00	90.00	0.75 Tech	**150.00**

Table 3: Budget Request Summary by Institution

Institution	***Baseline proposal***	***Updated Proposal***
Arizona	85	113.50
BNL	510	470.10
Nevis Lab	288	332.00
Penn.	0	60.00
Pittsburgh	0	0
SMU	157.2	234.30
SUNYSB	0	25.00
TOTAL	1,040.20	1,237.50

4.3.1. Studies of LAr detectors in high radiation environment

WBS: 4.3.1

Proposal to US ATLAS for LHC Upgrade R&D for FY07 Liquid Argon Calorimetry Behavior of Liquid Argon Gaps at High Ionization Rates

John Rutherfoord
With Leif Shaver, Michael Shupe, and Robert Walker
University of Arizona

Abstract

This is a funding proposal for FY07 to support LHC Luminosity Upgrade R&D on liquid argon electrodes. We are addressing the question "What are the limitations of liquid argon calorimetry in high ionization rate environments?" We start with a report on our progress, which, while considerable, is not entirely in line with last year's proposal. We then outline our proposed investigations for the next year. And we end with a budget estimate.

Results during FY06

As we were writing last year's upgrade R&D proposal we had just started a "run" with three electrodes nearly identical to those in the ATLAS FCal1 module, i.e. "tubular" electrodes with 250 μm gaps. But all are only 15 cm in length in contrast to the 45 cm length of the ATLAS electrodes. Also two of these three electrodes have rods made up of several sections. Inside of one section a cylindrical cavity had been bored leaving a 250 μm wall. A thin metallic foil with the beta emitter Strontium 90 deposited on one side was rolled into a cylinder to match the cavity. This 10 mm long foil was then slipped into the cavity and another length of solid rod with a short plug was soldered into the mouth of the cavity to seal the source inside. Together these made one longer rod. The tendency of the springy foil to "unroll" keeps the foil pressing against the walls of the cavity with the source coated on the outside surface. These two electrode rods were produced to our specifications by a nuclear power laboratory in Obninsk, Russia. (Thanks go to our ATLAS/Dubna collaborator Victor Kukhtin for identifying this contact for us.) One electrode has a 50 mCi source embedded inside while the other has a 2 mCi source to act as a control. For further control a third electrode with no cavity or source was constructed otherwise identical to the first two.

Fig 1. The blue foil is coated on the outside with a ^{90}Sr beta emitter. It is then inserted into a cavity in an FCal electrode rod. The cavity is then sealed with a solid rod with a short plug. The assembly is inserted into a tube with a PEEK insulator.

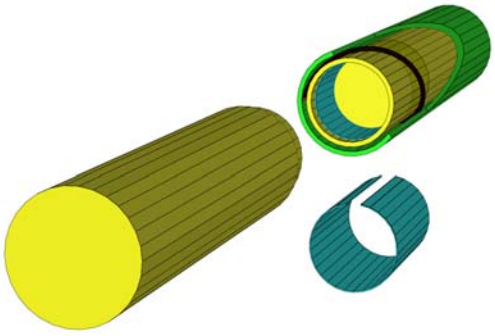


Figure 1 is a drawing of the source housing with the two-rod sections, which fit together to make up part of an FCal1 electrode. Figure 2 is a photograph of the parts.

Fig. 2. Photograph of the parts of one electrode rod. The rolled source foil is in the middle, the rod section with the cavity above it and the rod section with the plug below it. At the top and bottom are rod extensions that screw into the sealed source section to make a full length 15 cm rod. The full length is to help minimize personnel exposure.

The 50 mCi beta source gives an ionization rate in the liquid argon surrounding it of roughly equivalent to that expected in an FCal1 electrode at a depth of EM shower max at η= 4.7 at the LHC design luminosity of $\mathcal{L} = 10^{34}$ cm^{-2} s^{-1}. Because the source foil is 10 mm long, this high ionization rate region of the calorimeter covers an equivalent volume of about 0.5 cm^3 of the FCal1.

The three electrodes are housed inside a cube of copper with 15 cm sides shown in Figure 3. The radiation leaking out of this container is minimal. The electrodes were constructed from behind a thick Pb-glass block window and a large number of Pb bricks surrounding this window. Special tools allowed hands to be kept remote from the sources. Survey meters and film badges indicated personnel doses well below allowed levels.

The copper cube was suspended from the cryostat top plate and the electrodes were wired up so that they could be separately read out. The copper cube and tubes were held at HV while the rods were connected to ammeters with low impedance to ground. DC currents are read out.

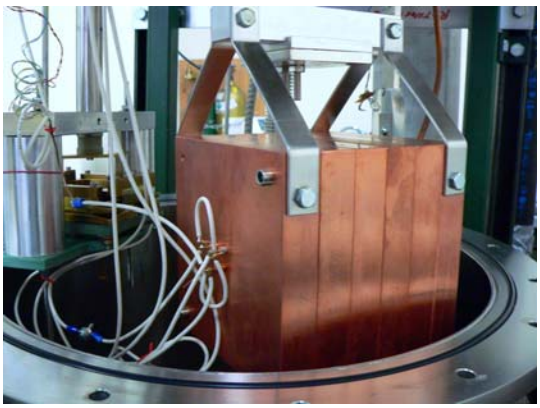


Fig. 3. The electrodes are inserted into a 15 cm Cu cube for personnel shielding.

We then filled the cryostat with liquid argon and started taking standard data. Our standard data-taking procedure is automated such that a computer-controlled number of current readings are taken at a computer-settable voltage. Then the voltage is stepped up and another set of readings is taken. A typical number of readings at each voltage is 25. The voltage is stepped up from zero to 1 kV. Note that 1 kV is 4 times the nominal operating potential for such a liquid argon gap. Liquid nitrogen dewars were exchanged every 30 to 40 hours.

This “run” started in late March 2005 and went well. We decided to see how long we could run, attacking one of the goals we had set ourselves. We expected some small mishap to stop the run but when that didn’t happen we continued far beyond our original guesses. We decided to stop just before the Christmas break because we would not have been able to get liquid nitrogen while the University was shut down. The length of this “run” was about 2.3×10^7 seconds which is equivalent to 2.3 LHC run years.

The PEEK insulating fiber is perhaps the material most likely to fail in the high ionization environment. So at the end of the run after we had disassembled the 50-mCi electrode we closely examined the fiber. It was not too hard to see a darkened length of fiber where it passed the 10 mm length of the ^{90}Sr foil. We photographed the fiber and taped it in the logbook labeling the location of the darkened region. After several months it would have been hard to locate the darkened region without the label. It appears that the PEEK was annealing itself. Also we saw no signs of mechanical weakening.

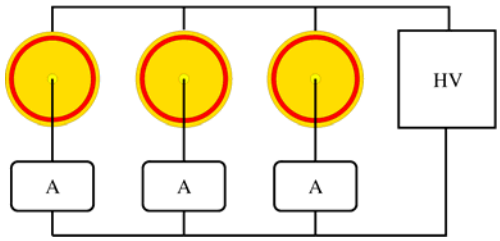


Fig. 4. The current from each electrode is read out by an ammeter for a wide range of applied high voltages.

Perhaps the most important result of this long run is that we saw the "layer buildup effect" in small gaps for the first time and, disappointingly, we didn't see any indication that the effect was saturating. At a fixed potential the current continued to degrade with time, showing no leveling off. At the nominal potential of 250 V the current from the 50 mCi electrode degraded by about 5% over the "run". Somewhat surprisingly, the 2-mCi electrode showed a very large initial drop in current, about 30%, at fixed potential followed by a slow decay for the rest of the "run", consistent with the ^{90}Sr half-life of 29 years. Three times during the long run the liquid level fell below the electrode causing a rise in current.

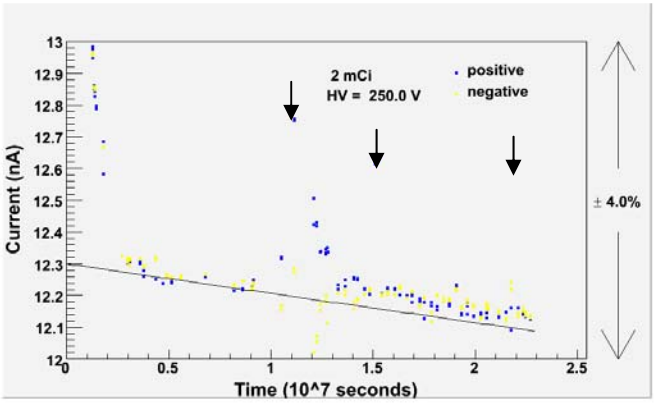


Fig. 5. Current at nominal HV vs. time for the 2 mCi electrode. The curve shows the exponential decay for the Strontium half life of 29 yrs. Arrows mark where the argon liquid level fell below the electrode.

The oxygen analyzer showed the contamina changing typically when we replaced the A during this long run.

After the Christmas break we took apart a section of the plumbing to install a flow meter and valves so that we could use the getter which had been given to us by our Brookhaven colleagues. We had also purchased a new canister but waited to install it until we exercised the system with the getter in the system.

We first did a short "run" without opening the system to the getter to see if we got data similar to what we got during the long "run". The current from the 50-mCi source was a bit lower than the final current we recorded during the long "run". This surprised us a bit so, after puzzling over it for a while, we guessed that it was because the outside surface of the rod containing the 50-mCi source was tarnishing at the location of the foil, presumably catalyzed in air by the radiation. So we polished the rod in our assembly jig and tried again. Still the current was lower than during the long "run". We then tried the Brookhaven getter with the old canister and got oxygen contamination levels below 0.1 ppm, a significant improvement from any reading we've had in the past. Here the current was even lower than during the long "run". Next we installed the new

canister and filled again. We are currently in this latest run. Up until now the oxygen contamination is about the same as with the old Brookhaven canister. Perhaps the old canister wasn't as depleted as Dave Rahm had suspected. Because we had suspected a much lower contamination level we next explored the possibility of recirculating the argon in the cryostat to continuously filter contaminants. We are now looking into purchasing a pump. The 50-mCi electrode is giving an even lower current than during the long "run".

We should also report that we had a radiation incident while polishing the 2-mCi source. The plug, which is soldered into the mouth of the cavity, broke loose under the stress of the polishing. Without leaving the room we phoned our Radiation Control Office. They arrived within 20 minutes with sensitive survey meters, decontaminated the assembly jig as much as possible (with adhesive tape) and then took it with them (sealed in a plastic bag), along with some of our customized tooling, to do a more complete job. They checked to make sure we hadn't gotten any of the Strontium on ourselves or anywhere else in the lab. Luckily it was completely contained within the well of the assembly jig. As a result of this incident we conceived of a better design for the source housing and have submitted drawings to our machine shop for fabrication. We have also contacted the Obninsk lab to see if they can construct another 2-mCi source for us. The first 50-mCi source was very expensive ($15k) but after Obninsk perfected their procedure, additional sources are quite in line with prices for stock sources from US firms. (The problem is that US firms aren't interested in producing custom designed sources so we will be forced to deal with Obninsk for future custom sources.)

Once the 2-mCi source broke open a possible explanation for the strange evolution of the current readings at fixed voltage presented itself. Betas originating on the outer surface of the foil (they all originate there) then penetrate the cavity wall and enter the liquid argon in the electrode gap, producing ionization current that we measure. But other betas head in the direction of the foil, penetrate the foil, cross the evacuated cavity, penetrate the foil again, then penetrate the wall of the cavity, and enter the liquid argon in the gap. There are fewer of such betas with sufficient kinetic energy to penetrate the additional material of twice the foil slant-thickness. If the source was leaking liquid argon very slowly into the cavity during the long "run", then those betas which were headed towards the cavity (rather than in the direction of the wall of the cavity) would have met more material (the liquid argon) before penetrating the 60 μm thick zinc foil again, then next the cavity wall, before ionizing the liquid argon in the gap. The initial drop in current seen from the 2-mCi electrode is in semi-quantitative agreement with this hypothesis. After about 0.3×10^7 seconds the cavity filled with liquid argon so no further drop in current was observed, other than that expected due to the depletion of the Strontium due to its 29 year half-life. We are starting detailed EGS simulations to test this hypothesis quantitatively.

Our most recent data suggests that the 50-mCi source is also leaking. It now seems likely that the 50-mCi source was slowly leaking during the long run in 2005. While we have definitely observed the "Layer Effect" at low voltages, it now seems possible that the continued drop in current at the nominal operating voltage wasn't due to the Layer Effect after all. Our conclusion that the Layer Effect doesn't saturate is now in doubt.

FY06 Goals accomplished

What we have called the "Layer Effect" is manifested by two phenomena: 1) At low voltages we see that at constant voltage the current drops with a time-constant of many minutes. 2) At higher voltage the current is constant but is lower after the layer builds up that before the layer builds up. In earlier studies with parallel plate electrodes with remotely adjustable gap we opened up the gap to 4 mm to build up the layer over many hours to a day and then closed down the gap to 0.5 to 1.0 mm to observe the manifestations of the Layer Effect. (The parallel plate electrodes are hard to adjust to less than 0.5 mm with any precision.) One goal of the long run was to study the Layer Effect with a fixed small gap of 0.25 mm. Does the layer build up only with larger gaps and higher voltage, or does it build up also with small gaps, albeit over longer periods of time?

We are well along the path we outlined last year of reducing the level of contaminants in the liquid argon. And we have had a long run with realistic electrodes that we proposed for FY05. We had also proposed a long run to see if the Layer Effect saturates. At first sight this was a failure due to leaking electrodes. But my present best guess is that we actually had a serendipitous success. For both the 2-mCi source and the 50-mCi source in our most recent data we now see a constant current at nominal voltage. No longer is the current degrading over many days. We interpret this to mean that the cavities in both electrodes have filled with liquid argon. (Of course this was already the case for the 2-mCi source during the long run.) One would guess that the ratio of current before leaking to current when the cavities are full would be the same for the two sources. But this ratio is smaller for the 50-mCi source. The likely reason is that bulk recombination is significant in the 50-mCi electrode gap before leaking starts and less so when the cavity fills. Bulk recombination is always negligible in the 2-mCi electrode gap. From the ratio of ratios we may have a sensitive measure of the bulk recombination rate constant. It will take quite a bit of Monte Carlo work to confirm this guess and extract a value for this rate constant.

Never before did we have a method to change the ionization rate and, with luck, we won't have such a possibility ever again (since it involves destruction of a valuable source). But this data we've taken as the present sources filled with liquid argon have given us valuable data that might yield results we would have only had with much more effort and much more indirectly.

For the immediate future we propose to continue our attempts to reach purity levels well below 100 ppb. (We are now at 80 ppb with the BNL getter, as measured by one of our two oxygen analyzers. The other, newer analyzer takes many days to settle down and is still converging on a reading.) We will probably install a recirculation system. After that we will try the getter and the ICARUS oxysorb filter in series. To see the effect of the improved purity we need sources. We can either go back to our parallel plate electrodes and "button" beta sources or use replacement FCal-style electrodes. We have designed a new, far more robust rod/cavity arrangement so that even the rough polishing procedure won't break open the electrodes and are in negotiations with the Russian Nuclear Power laboratory to produce these new sources for us. To actually get to the point that we can use such new sources will take quite some time because of the delays in contracting with the Russian lab and in getting the necessary approvals from our Radiation Control Office on campus.

Statement on FY06 funding

FY06 upgrade R&D funds for this work were available to us at the end of March 2006. Part of the delay was due to a fairly trivial mistake in the BNL contract that took some time to straighten out. And part of the delay was simply the time it takes to process paperwork at the University of Arizona. But our FY06 M&O funds arrived this year earlier than anticipated so we lived off a small fraction of these funds for awhile. It is possible to transfer funds between these two activities because BNL had the foresight to put the two on the same contract. But we haven't done this yet. Our work in FY05 was supported by our DOE University base grant.

Goals for FY07

Assuming we are able to reach significantly improved purity levels in the liquid argon during the remainder of FY06 and repeat our studies with new FCal-style electrodes, then for FY07 we will likely return to the parallel plate, adjustable gaps. With the oxygen attachment significantly reduced we can take quality data with the larger gaps (3 mm to 7 mm) allowing improved measurements of the two key parameters for positive ion buildup effects, 1) the positive argon ion mobility and 2) the bulk recombination rate constant. The new "button" 50 mCi ^{90}Sr source that we proposed last year will extend the available ionization rates well into the sLHC range.

Budget

Proposed budget for FY07

Technical support (salary)	$48k	
Misc. parts	$15k	
Supplies, cryogens, etc.	$18k	
50 mCi Sr(90) “button” source	$4k	
Total request		$85k

4.3.2.2 Development of an Analog Front-End ASIC for the LAr calorimeter readout upgrade

WBS: 4.3.2.2

Development of an Analog Front-End ASIC for the LAr calorimeter readout upgrade

Brookhaven National Laboratory, Upton, NY 11973-5000
o State University of New York at Stony Brook, Stony Brook, NY

1. Summary

The proposed project is to develop the radiation-resistant front end readout electronics for the ATLAS LAr calorimeter upgrade based on Silicon Germanium (SiGe) BiCMOS technology. This report includes the project status for 2006 as of now and provides the revised budget for FY 2007.

2. Status Report June 2006

The following is a list of the 2006 work so far:

1) Ionizing radiation studies of IBM SiGe devices of the 5AM, 7HP, 8HP (both bipolar devices and resistor) SiGe "generations". Devices have been characterized at 500krad, 1Mrad, 5Mrad, 10Mrad, 50Mrad and 100Mrad. Annealing studies after irradiations are also performed.
   This work is being carried out in collaboration with University of California at Santa Cruz (UCSC) and Georgia Tech. Tests are still in progress.
2) Design work on redesign of the front end preamplifier in SiGe BiCMOS technology. Pending results from the radiation resistance studies being carried on in parallel the 7WL technology has been tentatively targeted. Design is still in progress.

2.1 SiGe Ionizing Radiation Studies

Devices being irradiated are IBM process characterization structures obtained from IBM by John Cressler at Georgia Tech. The devices are being also characterized for proton irradiation and neutron irradiation at UCSC.
The gamma irradiation studies are being carried out using the BNL Cobalt-60 source. To be able to achieve a high total dose up to 100Mrad in a reasonable time the devices are being mounted on a supporting frame about 5cm from the source.
The irradiation field at such a short distance from the source is non uniform and has been characterized by means of TLD dosimeters in situ at a "high rate" position at 5cm from the source and at a "low rate position" at about 20cm. The average dose rate was about 275kRad/hr in the "high rate" location and about 29 krad/hr in the "low rate", with large but known variations across the irradiation field.

DOSIMETER ID #	rad	dose rate rad/hour	DOSIMETER ID #	rad	dose rate rad/hour
99101	7,984	191601	99113	9,605	27443
99102	8,822	211711	99114	9,281	26517

99103	11,686	280442	99115	9,768	27909
99104	11,308	271370	99116	9,849	28140
99105	12,415	297936	99117	9,876	28217
99106	12,929	310271	99118	10,092	28834
99107	8,309	199400	99119	9,632	27520
99108	7,471	179290	99120	8,957	25591
99109	11,578	277850	99121	9,335	26671
99110	11,281	270722	99122	9,876	28217
99111	11,497	275906	99123	10,200	29143
99112	11,578	277850	99124	9,281	26517

Time 101-112 0.04167 hours

Time 113-124 0.35 hours

Six groups of devices (8HP HBT, 7HP HBT, 5HP HBT, 5HP HBT, 5AM HBT, 8HP resistor, 8HP capacitors) will be characterized at the levels of 500krad, 1Mrad, 5Mrad, 10Mrad, 50Mrad and 100Mrad.

The following measurements are being performed:

Tests:
- 8HP HBT
- 8HP HBT--Biased
  - For gammas & protons
- 8HP HBT--Shield
  - For gammas & neutrons
- 7HP HBT
- 5AM HBT
- 8HP Resistor
- 8HP Capacitor

Measurements:
- Forward Gummel
  - Vcb=0V, 0.5V
- Inverse Gummel
  - Vcb=0V, 0.5V
- Early Voltage
- Neutral Base Recombination
- M-1, Avalanche Factor
- Resistance
- Capacitance

Runs:
- Characterization (Pre-Rad)
- Post-Rad (No Anneal)
- Anneal 1 (5 days @ 25C)
- Anneal 2 (1 day @ 60C)
- Anneal 3 (1 day @ 100C)
- Anneal 4 (6 days @ 100C)

To gather a quick glimpse of the gamma ray radiation resistance, first the 100Mrad irradiation at 275krad/hr has been carried out, interrupting the irradiation at each of the designated radiation levels. The data is being currently analyzed.
Fig 1 shows current gain for , 7HP and 8HP HBT transistors.
8HP has the best overall performance. The damage mechanism in the 7HP is distinctly different, possibly because the transistor had initially poor DC behavior (high VCE saturation voltage) due to structural differences.

Ionization damage is known to increase base current leakage by producing perimeter-dependent G/R centers. The 7HP has a distinctly thinner EB spacer oxide and a higher electric field in that region making it more susceptible to ionizing radiation damage

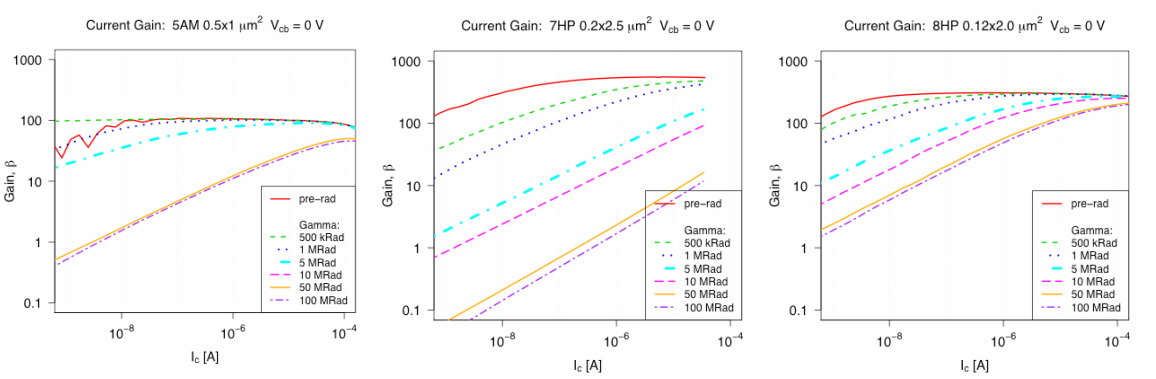


Fig 1: Current gain for the 5AM, 7HP and 8HP HBT transistors

The 8HP HBT was remarkably radiation resistant, with a gain of 77 after 100Mrad at 1uA.

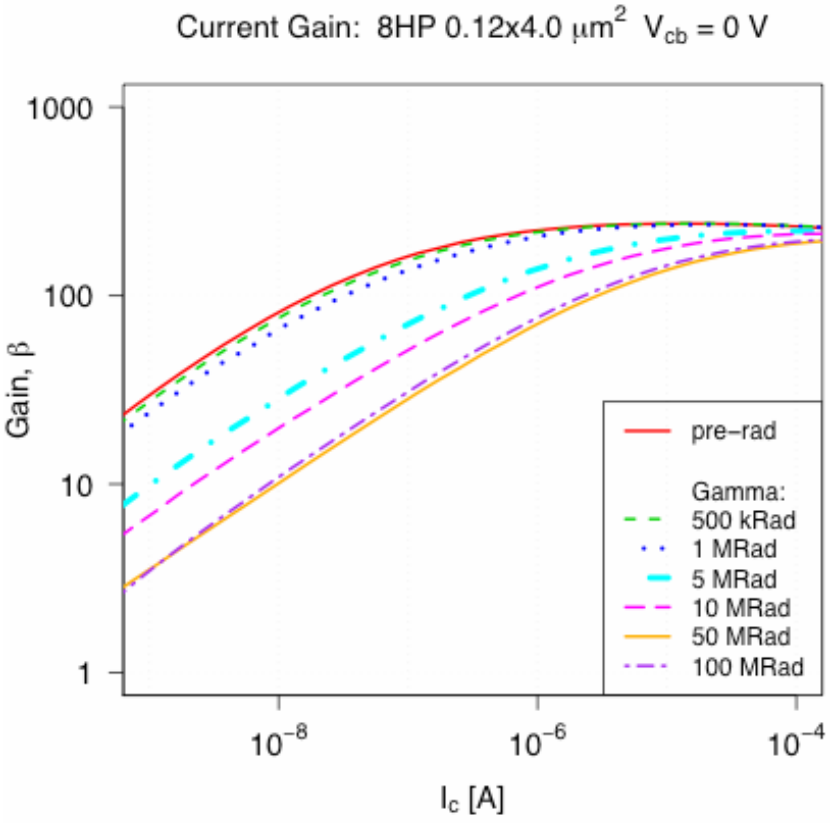


Fig. 2 Current gain for 8HP HBT at various total dose levels.

In the next irradiation runs a box of 2mm lead and 1.5mm aluminum will be installed around the devices under test to conform to ASTM F1892-98 standard for Co-60 irradiation and remove any

damage component due to soft x-rays generated by scattered gammas. As before the dose rate of the device positions will be calibrated with TLD dosimeters.

2.2 SiGe Front-End Preamplifier Design

A preliminary "exploratory" design has been started prior to the radiation damage studies to assess the feasibility of a SiGe design of a preamplifier for LAr calorimetry.
Among the available technologies the 7WL process has been targeted. It is a n analog process primarily targeted for wireless applications, and it provides a full complement of devices, both active and passives, including protection structures which may prove indispensable to protect the preamplifier from discharges in the calorimeter. Due to its "analog" applications it provides "high breakdown devices", capable of sustaining up to 6V EB breakdown voltage. It is also a relatively new process (2 years old) that will likely be available during the long radiation characterization, design, and production cycle for LAr upgrade electronics, which will stretch for 5 years or more.

Bipolar transistor noise is limited by the parasitic base spreading resistance, $r_{bb'}$. This resistance is minimized in "two emitters" transistors layout as represented in fig 3, which provides a triple base diffusion, thus minimizing the base resistance. It is also found that "high breakdown" devices minimize the base resistance.

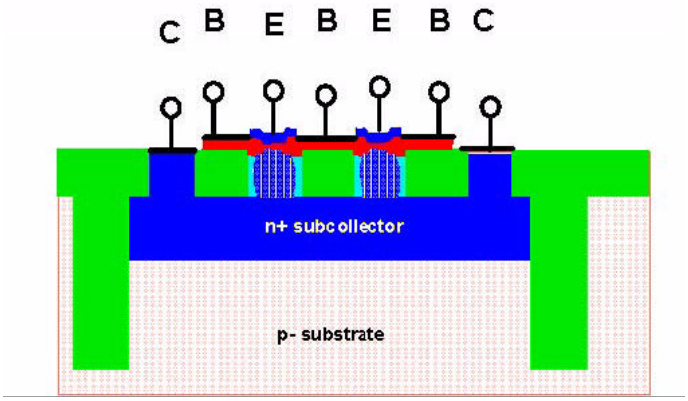


Fig 3: HBT "two emitter" layout

Table 1 summarizes transistor parameters for the high breakdown transistors.
A device size of 0.24x20x2 with 2 devices in parallel has been chosen to achieve a base resistance (sum of the intrinsic and extrinsic base resistances) less than 1.5Ω which is the value of the current discrete design.

TABLE 1: *High-Breakdown (HB) NPN Device Parameter Comparison*

Device Parameter	Drawn Emitter Dimensions (μm)								
	.24 x 1 x 1	.24 x 5 x 1	.24 x 20 x 1	.24 x 20 x 2	.48 x .48x 1	.48 x 2.5 x 1	.48 x 20 x 1	.8 x 3 x 1	.8 x 20 x 1
Extrinsic Re (ohms)	16.4	3.20	0.80	0.63	25.4	3.01	0.40	1.47	0.23
Extrinsic Rb (ohms)	89.1	26.8	11.2	3.02	73.2	42.7	11.2	35.1	11.3
Intrinsic Rb (ohms)	32.7	9.59	3.41	1.24	69.9	27.5	6.64	35.4	10.8
Extrinsic Rc (ohms)	107.2	36.2	17.0	7.12	144.2	52.7	16.5	44.4	16.0

Intrinsic Rc (ohms)	15.2k	3.49k	901.0	450.5	19.9k	4.15k	591.0	2.42k	410.2
BE intrinsic cap (fF)	1.96	9.51	37.8	75.6	2.166	8.38	62.2	15.5	95.3
BE oxide cap (fF)	0.75	2.52	9.16	18.3	0.57	1.50	9.56	1.84	9.96
BC extrinsic cap (fF)	0.32	0.90	3.08	6.15	0.28	0.57	3.11	0.69	3.16
BC intrinsic cap (fF)	0.26	0.95	3.54	7.08	0.22	0.69	4.72	1.07	6.29
BC oxide cap (fF)	1.35	2.56	7.11	9.96	1.26	1.88	7.19	2.12	7.28
CS intrinsic cap (fF)	7.45	11.4	26.4	32.7	7.17	9.23	27.1	10.1	28.1

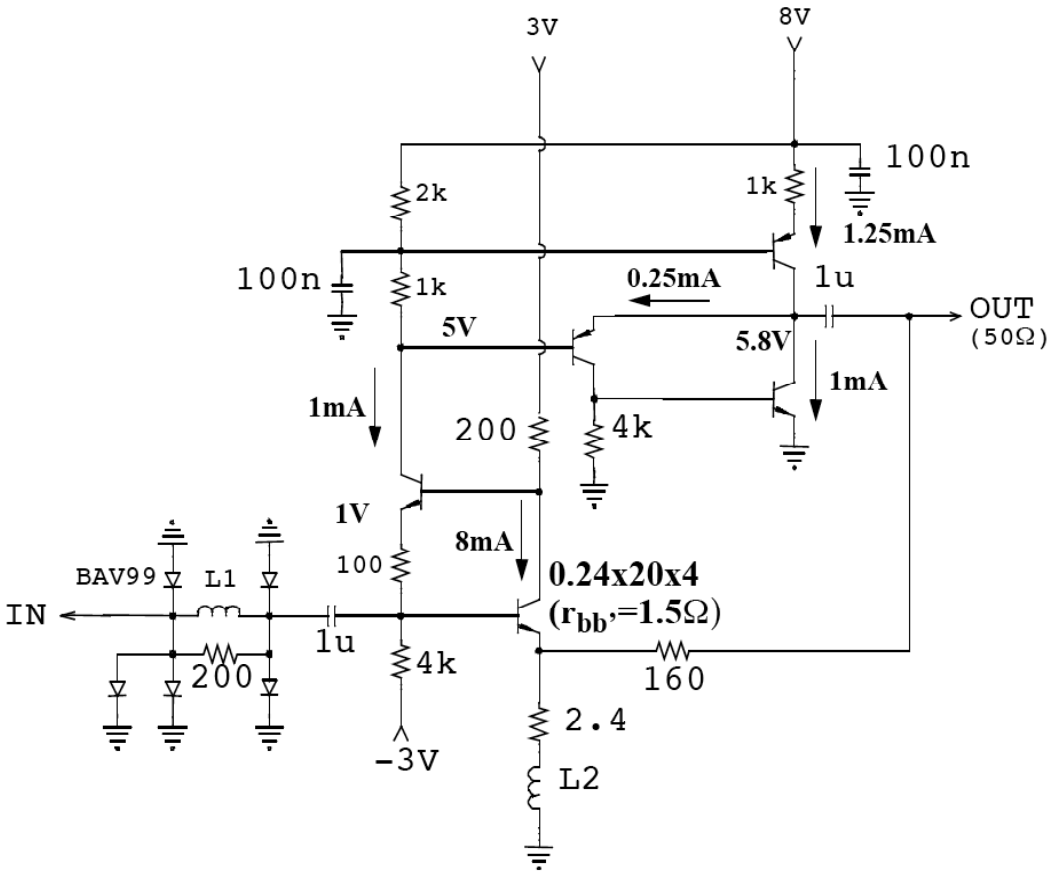


Fig 4: Preliminary preamplifier design.

Fig 4 shows the preliminary design. As in the current discrete design the first transistor of the White follower and the current source have been realized with PNP transistor. The 7WL process makes available a decent lateral PNP with a cutoff frequency of 600MHz.
Lateral PNP transistors are notoriously not very neutron resistance, ad a subsequent design iteration will make use of PMOS available in the BiCMOS technology. The 10V power supply rail has been reduced to 8V to limit the VCE of the last driver to 6V.
The power dissipations are therefore 40mW, slightly less than the existing design.

The high breakdown voltage of the 7WL process made possible to maintain the 1kW gain of the present design (the highest gain currently used). A future design iteration will explore the use of the 8-generation IBM technology, which sports a lower breakdown voltage and will therefore mandate a lower gain and lower power supply rails.

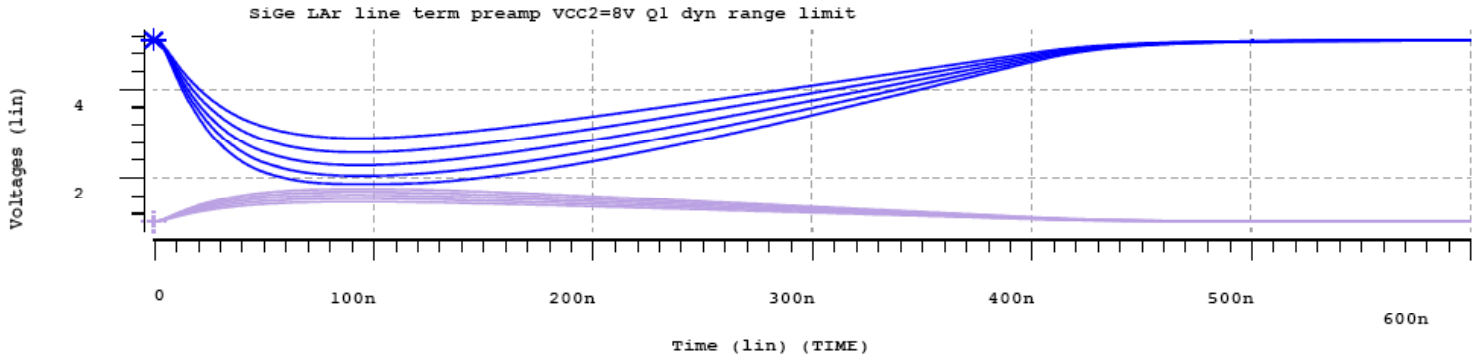


Fig 5: Preamplifier output

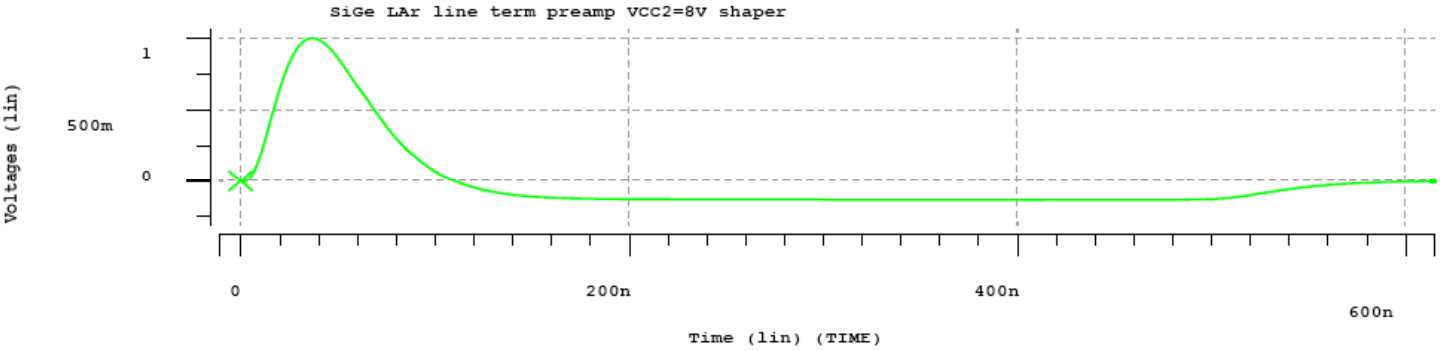


Fig 6: Shaped output

Fig 5 and 6 show the preamplifier response and the shaped response to a LAr triangular current signal with a drift time of 400ns. The shaping assumed is the current CR-RC2 shaping with a time constant of 13ns.

3. Plans for FY07

The stress in FY 2006 has been on radiation characterization of SiGe processes and on design of the preamplifier. For FY 07 the work plan includes:

- Study radiation damage of protection structures
- Radiation characterization of CMOS devices and lateral PNP, for gamma and neutron or high energy protons
- Develop SPICE models of “radiation damaged” devices, aiming first at the most important parameters (e.g. gain)
- Analyze the performance tradeoffs of preamplifier designed in different process (noise, bandwidth, dynamic range, radiation resistance, electrostatic discharge damage susceptibility, power) to identify the optimal technology for the LAr front-end electronics

- Examine, design and qualify input protection blocks based on manufacturer recommendation and on past experience (PENN had good results using NPN collectors as input protection diodes).
- Design of candidate shaping stages targeting the LAr front end electronics
- Design of "standard" analog and digital BiCMOS blocks (e.g. bandgap references, D/A, AND/OR, Track & Hold, comparators)
- Examine existing CMOS low level driver/receiver blocks (LVDS etc) and investigate potential power savings and performance improvements utilizing SiGe technology

4. Personnel

BNL:

S. Rescia	Electronic Engineer	Contact, Coordination, ASIC design, System, Tests
J.F. Pratte	Electronic Engineer	ASIC design, Layout
J. Kierstead	Physicist	Radiation Tests
H. Chen	Physicist	Evaluation, Tests, Layout
F. Lanni	Physicist	Coordination, System, Tests
Bob Hackenburg	Physicist	Tests
David Lissauer	Physicist	Coordination, Integration

SUNYSB:

Dean Schamberger	Physicist	Design,Coordination

UPENN:

Brig Williams	Physicist	Coordination, Integration
Mitch Newcomer	Physicist	Design,Test, Coordination
Rick VanBerg	Physicist	Design,Test
Nandor Dressnandt	Physicist	Design, Test

5. Institutions

Brookhaven National Laboratory, Upton, NY
State University of New York at Stony Brook, Stony Brook, NY
University of Pennsylvania, Philadelphia, PA

6. Budget Summary for FY07

Inst.	Activity	Budget Request
BNL	Design and fabrication of v1 ICs (PA/Shaper/TH integrated)	85,000.00
	Radiation Testing	10,000.00
	TOTAL Mat	95,000.00
	0.25 FTE Elec. Engineer	40,000.00
	0.5FTE Tech	60,000.00
	TOTAL ManPower	100,000.00

	TOTAL	195,000.00
SUNYSB		
	Cadence Licensing	9,000.00
	Rad. Test	10,000.00
	TOTAL Mat.	19,000.00
	0.1 FTE EE	6,000.00
	TOTAL ManPower	6,000.00
	TOTAL	25,000.00
UPENN		
	Transistor Parametric Analyzer	10,000.00
	Bonding Specialized Services	3,000.00
	TOTAL Mat	13,000.00
	0.5 FTE Stud	15,000.00
	0.2FTE EE	32,000.00
	TOTAL ManPower	47,000.00
	TOTAL	60,000.00
	TOTAL FY07	280,000.00

4.3.2.3: Development of the digital architecture and dataflow analysis for the LAr calorimeter readout upgrade

WBS: 4.3.2.3

Design of a Next Generation Front End Board Architecture for the ATLAS Liquid Argon Calorimeter

Columbia University, Nevis Labs

1. Overview

The readout of the ATLAS LAr calorimeters for the initial LHC run has been successfully developed by the Atlas-LARG collaboration. The Columbia group designed the Front End Board (FEB), designed five out of the eleven radiation-hard ASICs used on the board, and managed the production of the 1600+ FEBs needed for the experiment. The group is planning to play a similar role in the design and production of a second-generation board and its custom components. If a replacement of the FEBs is needed, the new boards would presumably be installed simultaneously with the upgraded inner detector (ID), thus profiting from a long shutdown and minimizing risk of damage to ID cables and services. Assuming that this will happen in 2013 implies that all components must be available by 2011 at the latest, and therefore imposes a tight, albeit manageable timeline for the project. This is however complicated by the fact that very few external constraints are currently known, the most important of which are the SLHC bunch-crossing rate and the future ATLAS trigger bandwidths and latencies. On the other hand, the few known constraints are stringent:

- Dynamic range: the energy deposited in a single cell can be as high as 3 TeV, while the low end is defined by energy deposits due to the multiple interactions in each beam crossing (pile-up). The latter is about 50 MeV at 10^{34} $cm^{-2}s^{-1}$ and increases with the square root of instantaneous luminosity. This imposes a minimal dynamic range between 14 and 16 bits at the SLHC.
- Since the FEBs cannot be moved further from the cryostats without unacceptable signal degradation, they will need to be installed in the same location, i.e. between the barrel and endcap calorimeters. This imposes significant constraints on the available space, radiation tolerance and power consumption.

A legitimate question is whether the FEBs will need to be replaced at all. If the trigger bandwidths and latencies don't change, and the interval between bunch crossings is 25 or 12.5 ns, it will in principle be possible to run with the existing FEBs from a technical point of view. In this case, it is necessary to determine if these boards will survive the increased radiation levels and extended running period. The radiation levels at the location of the FEBs will be measured when the LHC is running, and, independently of this proposal, we have started accelerated lifetime tests for the FEBs, using a set of preproduction boards.

2. Status in June 2006

Even though funding for FY06 did not arrive until Spring, the R&D program was started in late 2005 using funds advanced by Nevis Labs. This allowed us to start the design for the flow of digital data, from the ADCs to the optical transmitter.

The baseline architecture assumes that digitization is done for all bunch crossings and all of the data is sent off detector, and is shown schematically in Figure 1.

The data from four channels (assumed to be 12 bits of ADC data and 2 bits indicating the gain scale) is written together with 8 bits giving the bunch crossing to a 64-bit wide dual port RAM at the bunch crossing rate, taken to be 40 MHz at this time. This memory is shallow (eight 64 bit

words) to minimize the probability of upsets, and the management of read and write addresses in the memory is done using Gray codes to detect upsets there immediately. The data is read in four 16-bit words into a triply-redundant multiplexer at a rate that is slightly faster than the bunch crossing clock, allowing the regular insertion of commas. This clock is derived from a crystal running slightly faster than four times the bunch crossing clock. From the multiplexer, the data is sent in 16-bit words to a serializer using IBM 8B10B encoding, and then over an optical link off detector. The current choice of 40 MHz for the accelerator clock should be close to the bunch crossing rate at the SLHC, and the multiplexing in groups of four channels is partially motivated by the availability of a commercial transmitter capable of data transmission at 3.3 Gbps per channel (see below).

The design has been implemented in a small test board using an ALTERA Stratix GX FPGA and an Agilent HFBR-772 transmitter. The board is shown in Figure 2.

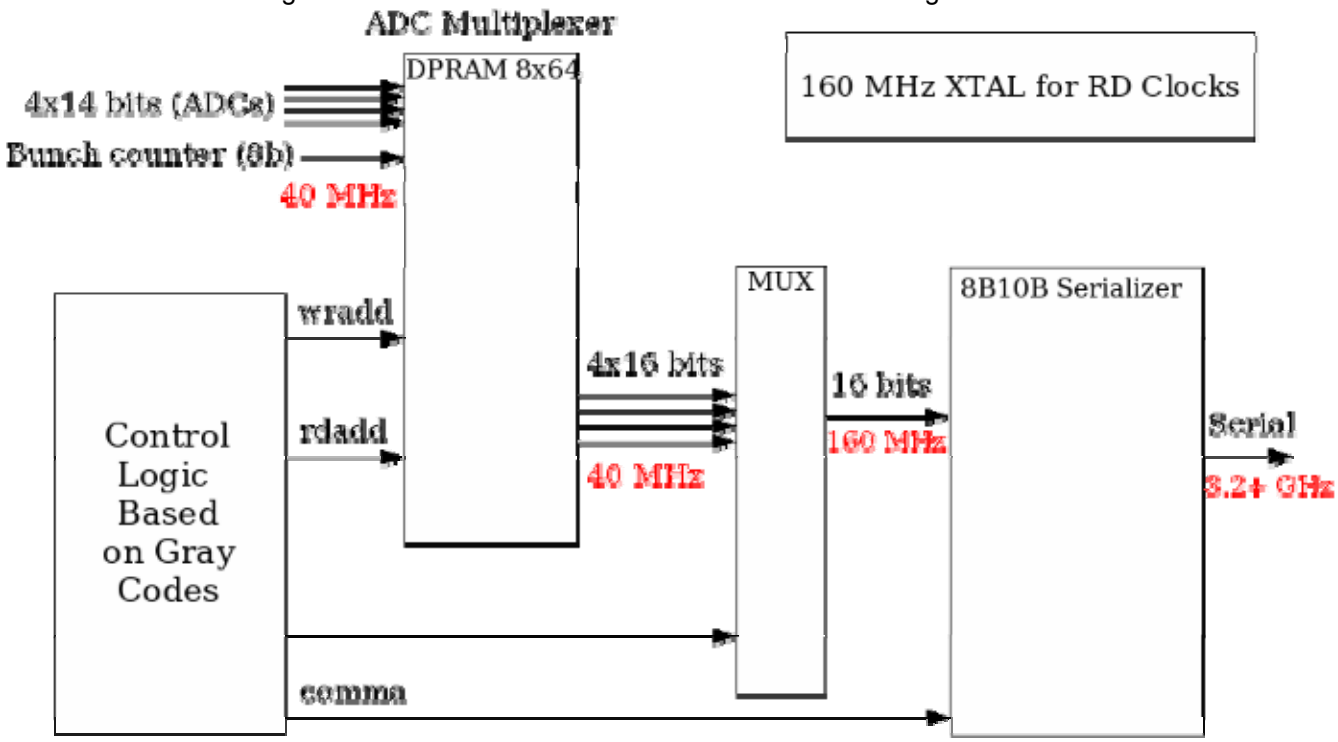


Figure 1: Schematic diagram of digital dataflow design for the baseline architecture.

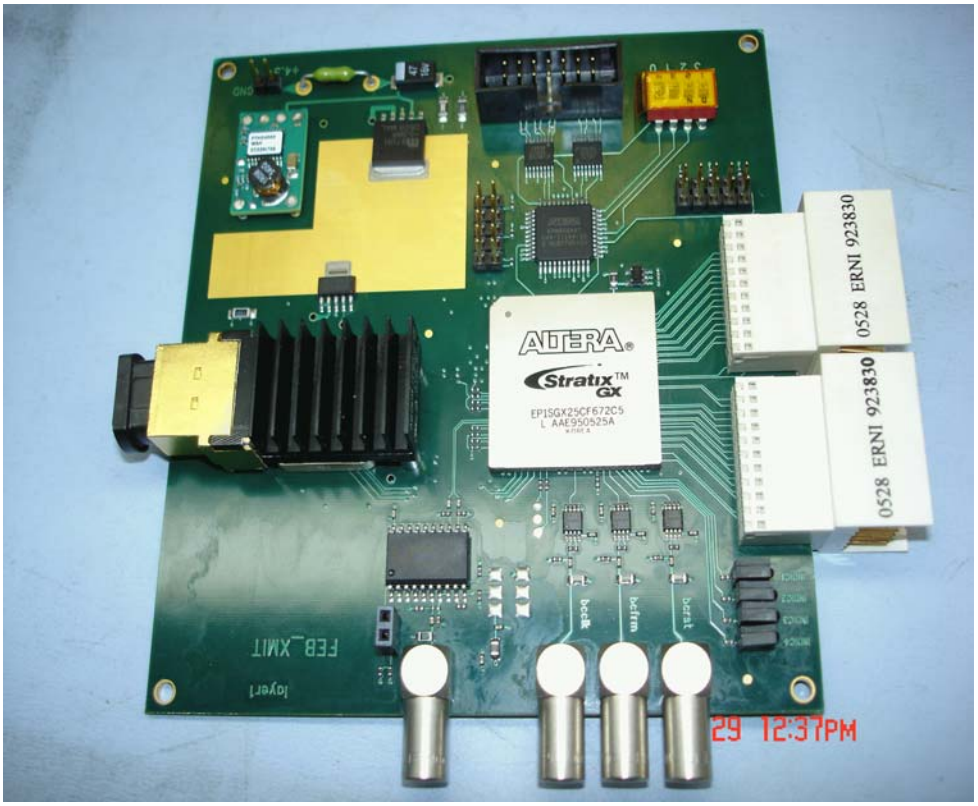


Figure 2: Transmitter test board.

All of the digital logic is implemented in the FPGA, with the possibility to feed in data from ADCs (white connectors on the right). The optical transmitter (on the left, with a cooling block) is a 12 x 2.5 Gbps device with an MTP ribbon connector. Simulation suggested that it would run cleanly at 3.3 Gbps, our preferred frequency, and to test this we made it possible to override the crystal frequency with an external clock. All clocks are fed in through the LEMO connectors and can be varied over a large range. The complete test setup includes a PC, a PCI board of Nevis design (in the PC) used to send control information and acquire data, the transmitter board shown above, a corresponding receiver board which is currently being assembled, and a control fan-out board to distribute the control information to all boards in the setup, including ADC boards later on. To determine whether the optical transmitter, which is rated for 2.5 Gbps per channel would indeed function well at 3.3 Gbps we measured the eye diagram at that rate. The result is shown in Figure 3, where it can clearly be seen that the device appears to be working extremely well at this speed.

Following this result, we decided to go ahead and build the receiver board, which is, to a large extent, a “mirror” of the transmitter board. The main difference is that the ADC inputs are replaced with an 18-bit wide output bus which connects to the PCI card for direct data transfers into the PC. The receiver board is being assembled at the time of this writing.

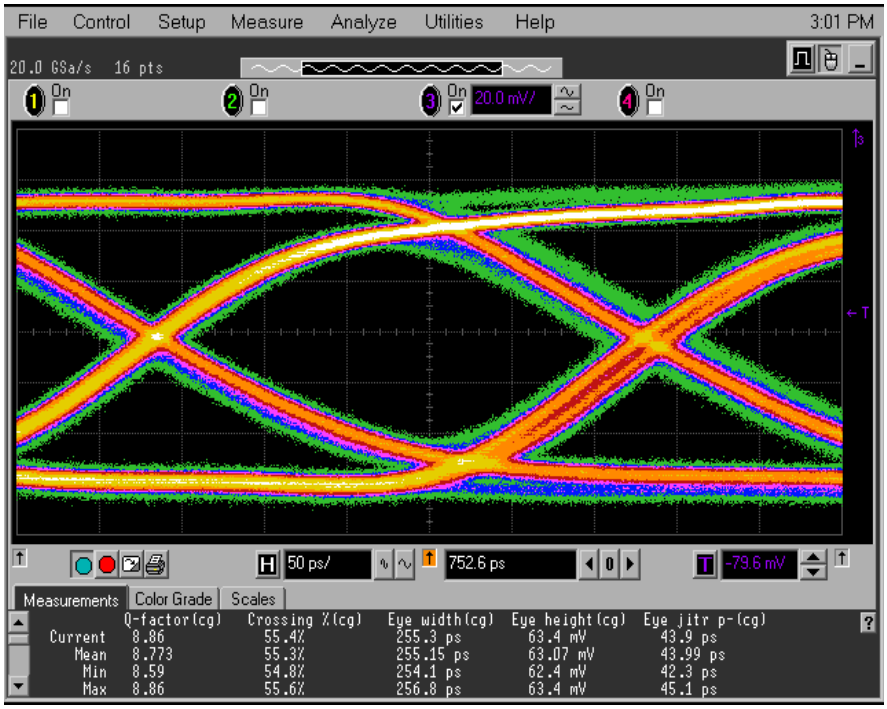


Figure 3: Measured eye diagram of the optical transmitter output at 3.30 Gbps.

3. Work plan FY06.

The receiver board should be completed soon. In the next few months we therefore expect to debug the board, then develop the data acquisition software needed to be able to do extensive performance tests of the digital dataflow architecture as designed. There are a number of tunable parameters that will be optimized during this process. In parallel, we are starting the design of ADC boards that will initially use commercial ADCs. At this time we have identified 2 commercial ADCs that we would like to characterize (one from Texas Instruments and one from Analog Devices). While we do not expect these to be radiation hard, they have characteristics that we believe are suitable: 4 to 8 channels with 12 or 14-bit dynamic range, 40 MSPS or faster, multiplexed LVDS output. This will allow us to complete our test setup from an architectural point of view. We also have some samples of the ADC developed for the CMS ECAL and are planning to test that, although we do not believe its characteristics will be suitable for our application. Note that each of these ADC boards also needs to have a means to inject controlled analog signals.

4. Work plan FY07.

There are a number of tasks we'd like to complete during FY07. The test setup needs to be completed and tuned up to represent a full slice, from ADC to receiver, with good data acquisition performance and user-friendly software.

Having completed a functional slice of the system using commercial components, we will turn our attention towards making a radiation-hard version. For the digital part of the system, an intriguing possibility is presented by ALTERA's “HARDCOPY” line: designs developed in FPGAs are migrated to a functionally equivalent, pin compatible device implemented in either 130 or 90 nm technology. Since tests indicate that the 130 nm process (at least IBM's) is intrinsically radiation hard, HARDCOPY might offer an interesting alternative to custom-designing the chip ourselves. HARDCOPY has the added advantage of reducing power consumption substantially compared to

the FPGA version. We are currently exploring the possibility to test a HARDCOPY for radiation hardness. If HARDCOPY is a viable solution, it would probably be substantially cheaper than designing and producing an ASIC. HARDCOPY does not appear to exist yet for the STRATIX GX, which we use in the transmitter board. But our choice of FPGA was driven by the need to drive the optical transmitter, and for the final board we expect the driver to be included in the chip, as described in the R&D plan for the optical link upgrade. It is also likely that ALTERA will expand this product line in the future. In any case, at this time testing of a HARDCOPY would require designing a new board that uses a STRATIX or STRATIX II. If discussions with ALTERA have a positive outcome, we will design such a board in FY07 for radiation testing in FY08.

We also want to expose the ADCs to test their radiation hardness. Even though we do not expect good results, it is not entirely impossible that the newer technologies used by ADC manufacturers make them more robust. Some representatives of ADC manufacturers in fact seem to suggest that this might be possible. Since we cannot rely on this, in FY07 we expect to start investigating ADC architectures in view of developing a custom ADC. The only other institution that has expressed interest in pursuing this is LAL-Orsay, and they will hopefully confirm their commitment soon. If they choose to work on this, we would start collaborating as soon as possible. If not, there is also the possibility of creating a partnership with industry similar to CMS' collaboration with ChipIdea. We think that the ADC is probably the most challenging component of a next generation FEB.

In terms of manpower, we are in the process of hiring a postdoctoral research assistant who will spend a substantial fraction of his/her time on this project, working in close connection with the engineers at Nevis. This position is funded from our base grant. We will need a large amount of engineering effort to work on the ADC development, and this will likely be limited by funding. Given the budget guidelines we would have Bill Sippach work on the project at 50% FTE, with the normal corresponding support staff (0.5 FTE electrical engineering for design verification and firmware development + 1.5 FTE electrical technician: total $262k) or a reduced support staff (0.5 FTE EE + 1 FTE ET: total $219k).

We will need to produce 6 ADC boards (2 for each type): $30k, and perform the radiation testing: $20k. We will need to produce a PCI Express version of our controls and DAQ card for increased DAQ speed: $10k. We would also like to design a test board that uses a STRATIX II to implement the digital logic for future radiation testing of a HARDCOPY ($10k). The total material costs therefore add up to approximately $70k.

5. Work plan FY08.

The evolution of the ADC design on this timescale is very difficult to predict, especially since at this time the partners are unknown. It is clear that at least 50% of Bill Sippach's time (with corresponding support staff) will be necessary to keep such a challenging project on course, but it would probably be better if that fraction could be increased. Given the difficulty in predicting the design pace, it is also almost impossible to predict the associated material costs. Assuming the needs are still limited to relatively simple expansions of the test setup, $30k should be a reasonable figure, albeit very uncertain. A chip submission this early seems unlikely.

We do hope to be able to perform radiation testing of a HARDCOPY in FY08, for which the basic board ($10k) and testing costs ($20k) add up to $30k. The major unknown is the cost of the HARDCOPY chip itself: while this is in principle rather expensive, the future market size in case of good performance is large enough that a discussion with ALTERA has started.

6. Differences with respect to last year's plan.

In the proposal submitted in June 2005, we anticipated the development of the full slice would take 24 months. We are currently substantially ahead of that pace and expect to complete the slice by the end of the year, thus recovering more than the delay caused by the late availability of funds.
This is partially due to a redirection of funds towards engineering, and makes it unlikely that we will do any radiation testing in FY06. We will be performing those tests in FY07. For all practical purposes, the funding delay has therefore been absorbed by a different ordering of tasks without any long term schedule slippage.

One year ago we also anticipated starting the design of the digital dataflow chip in 130 nm technology in FY07, with a possible preproduction run in FY08. While nothing stops us from proceeding with that plan, it now seems premature for multiple reasons: there has been remarkably little evolution in determination of the SLHC running parameters, the collaborative efforts for design of other board components are coming together at a slower pace than we had hoped, and the HARDCOPY option seems attractive enough to warrant an in-depth evaluation. Our limited investigations into ADC architectures have also led us to the conclusion that this will be an even more challenging task than we expected and we would like to get started on it sooner, increasing the corresponding engineering efforts.

7. Summary of funding requests.

FY07: $332k

-Electrical engineering: $166k.

-Electrical technician: $96k.

-Materials and supplies: $70k (6 ADC boards - $30k, 1 PCI Express DAQ board - $10k, radiation testing - $20k, , 1 transmitter board with Stratix II - $10k).

4.3.2.4 Development of a link-on-chip solution to the optical data link upgrade for the ATLAS LAr front-end readout

WBS: 4.3.2.4

Progress Report on the Project of "Development of a Link-on-chip Solution to the Optical Data Link Upgrade for the ATLAS Liquid Argon Front-end Readout" and Budget Revision for FY 2007

Ping Gui, Jingbo Ye,
Southern Methodist University
Dallas, Texas 75275

1. Summary

The proposed project is to develop the next generation optical data link, a Link on Chip (LoC) solution based on the Silicon-on-Sapphire technology, for the ATLAS Liquid Argon (LAr) Calorimeter front end electronics readout. We report the project status of 2006 as of now and provide our revised budget for FY 2007 in this document. The original proposal is attached to this document.

2. Progress report for 2006

The FY2006 funding arrived at SMU and was made available to us in late May 2006. We started this project on borrowed support from SMU.

The following is a list of the work we have been doing:

3) We irradiated a laser driver and PIN amplifier chip based on Peregrine's 0.5 micron SoS technology. Data analysis of this test is now completed and a note is being drafted to report the results.
4) This first look at SoS technology in radiation environment led us to design a dedicated test chip using Peregrine's 0.25 micron SoS technology. The purpose of this test chip is to measure leakage current of different transistor layout, and to evaluate the radiation-hardness of enclosed layout transistors (ELT). This test chip will also provides ELT transistor parameter measurements that will help model this special layout in chip designs. This test chip has been fabricated and we are in the process of constructing the test system that will evaluate this chip both in lab and in radiation environment.
5) The design of the Link-on-Chip version 1 (LoCV1) prototype. This work is in progress and will be reported in detail below.

We took advantage of the existing laser driver chip designed by us for other projects to have a first look at the Peregrine's SoS technology in radiation environment. This laser driver chip, based on a 0.5 micron SoS technology, is a 2-Gbps, 4-channel, DC coupled differential transceiver IC designed to drive VCSEL and amplify signals from a PID diode. We constructed a test system to measure the functions of this laser chip in proton radiation at Massachusetts General Hospital (MGH), Boston. The setup is shown in figure 1 and a picture of the proton test is shown in figure 2.

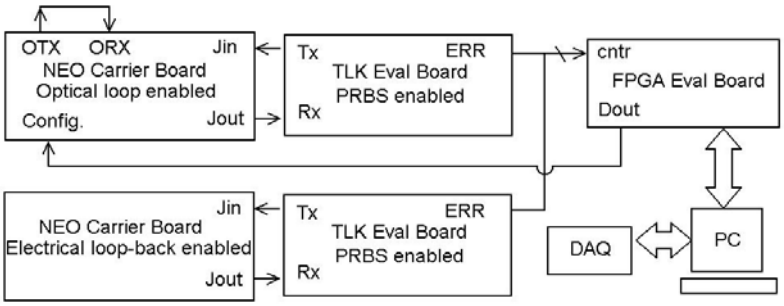


Figure 1, test setup for the 0.5 micron SoS chip.

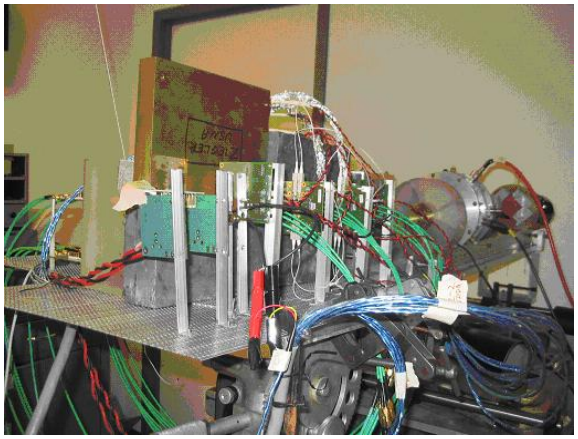


Figure 2, test setup in the proton beam at Boston

In this test we reached a total fluence of 1×10^{15} p/cm^2 with a peak flux of 1×10^{12} p/cm^2/sec. The chips worked error free up to a fluence of 3×10^{14} p/cm^2 at flux below 1×10^{9} p/cm^2/sec. The chips survived the total fluence with errors and fully recovered after some annealing periods. A more detailed report is being worked on and will be submitted later. During this test, we also noticed radiation induced leakage current from the increase of the total input current to the system. We understand that when we designed this chip for other projects we did not use any rad-hard layout techniques. In order to quantify the leakage currents and evaluate the ELT layout technique that has been proved to be effective in CMOS technology to mitigate total dose effect, we decided to design a dedicated SoS test chip using the 0.25 micron SoS technology that is now available through Peregrine. Peregrine is also interested in this work and provided $20k in-kind support on this test chip in the form of reduced chip fabrication cost.

We designed this test chip to probe the radiation resistance limits of the Peregrine's SoS process. Inside this test chip, we place transistor arrays to measure the radiation-induced leakage current. Different transistor sizes and layout techniques have different effects on mitigating this leakage current. The enclosed layout transistors (ELT) have been proved to be effective in eliminating radiation induced side leakage current in 0.25 micron bulk CMOS technologies. We need to check if the ELT is also effective in the SoS technology, and measure its parameters to be used in simulations and calculations in future chip designs. Since the SoS technology is relatively new, we can not find publications about such parameters. In the same chip, we also implemented test structures such as DFFs, shift registers and ring oscillators for SEU characterization and frequency measurements. Other basic function blocks like majority voting circuits are also placed in the test chip to provide parameter measurements for the design of the LoCV1.

The layout of this chip is shown in figure 3.

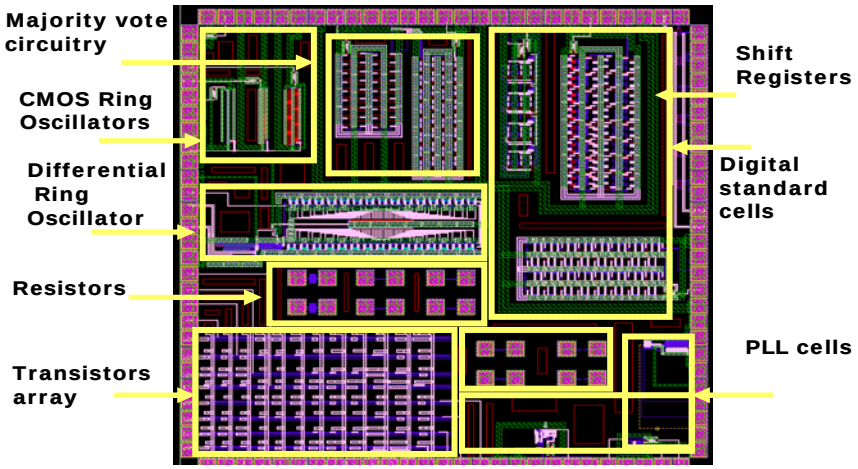


Figure 3, the test chip layout. Function blocks are indicated.

This test chip was submitted to Peregrine for fabrication in October 2005. To test this "test chip" a carrier board and its corresponding control board were designed and fabricated in March 2006. This system is now being debugged in lab. We expect to carry out the irradiation tests (gamma and proton) in late summer or in the fall on this test chip.

Shown in the following pictures are the two boards responsible for measuring all the parameters and function units on the test chip. A dedicated multi-channel power supply board is also developed to provide current monitoring of the device under test in radiation. This board will be reused for future irradiation tests.

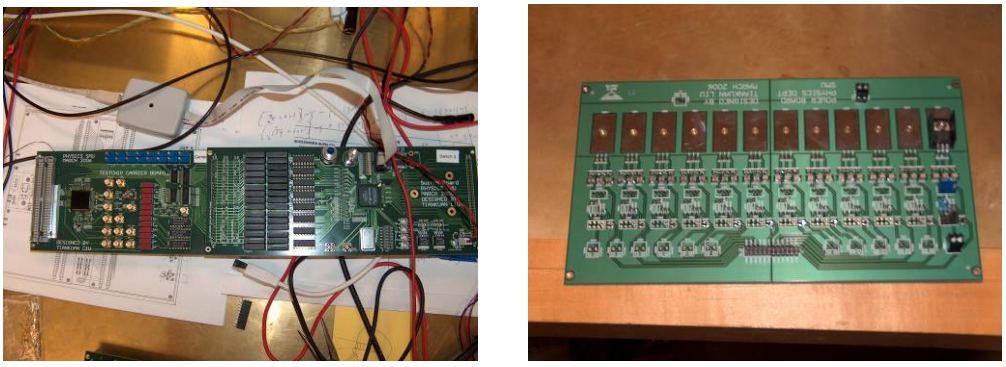


Figure 4, SoS test boards. Shown in the left picture are the carrier board and the control board. Shown on the right is the multi-channel power supply board (only one channel assembled for debugging use as of now) with current monitoring in each channel.

The design of the LoC version 1 (LoCV1) started November 2005. LoCV1 block diagram is shown in figure 5.

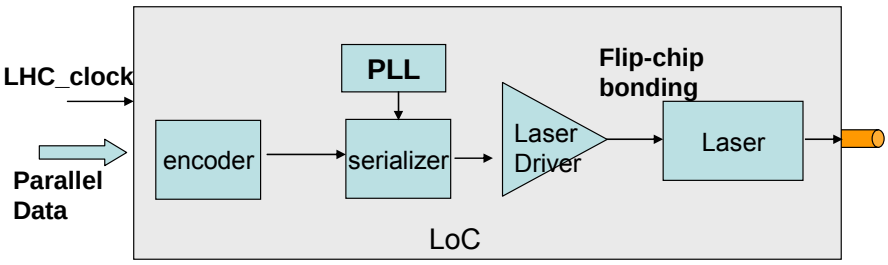


Figure 5, block diagram of the LoCV1 chip.

The key function block is the PLL that, together with the serializer block defines the speed of the LoCV1 chip. For the first prototype we choose a very conservative PLL design that is 2.5Gbps with the possibility to run at 3.125 Gbps.

The design of this PLL is shown in figure 6.

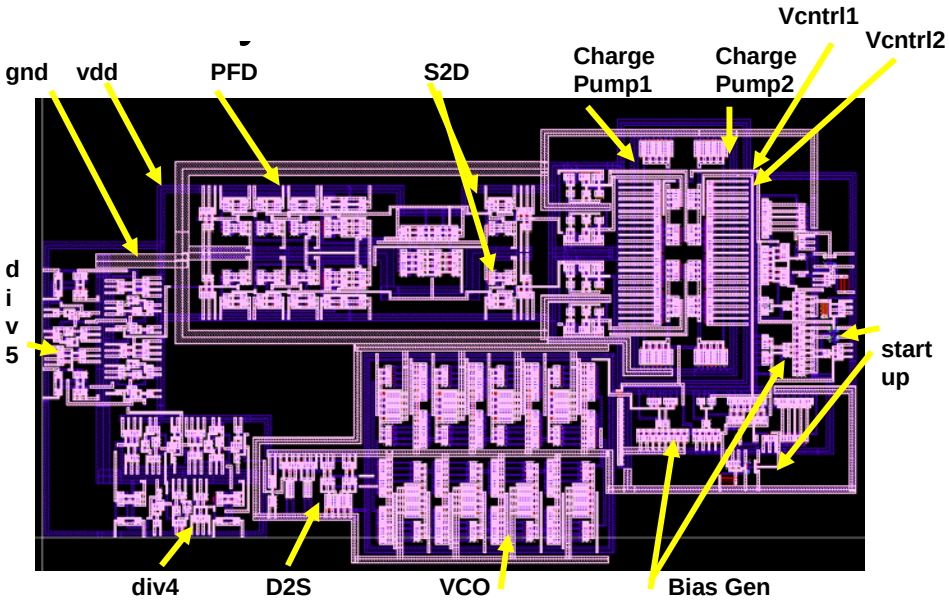


Figure 6, the PLL design and layout.

Post layout simulation in Cadence indicates that this PLL can run at a frequency at both 1.25 GHz and1.6 GHz, meaning that we may be able to achieve our design goal of 3.125 Gbps for LoCV1.

The design of the Serializer is shown in figure 7.

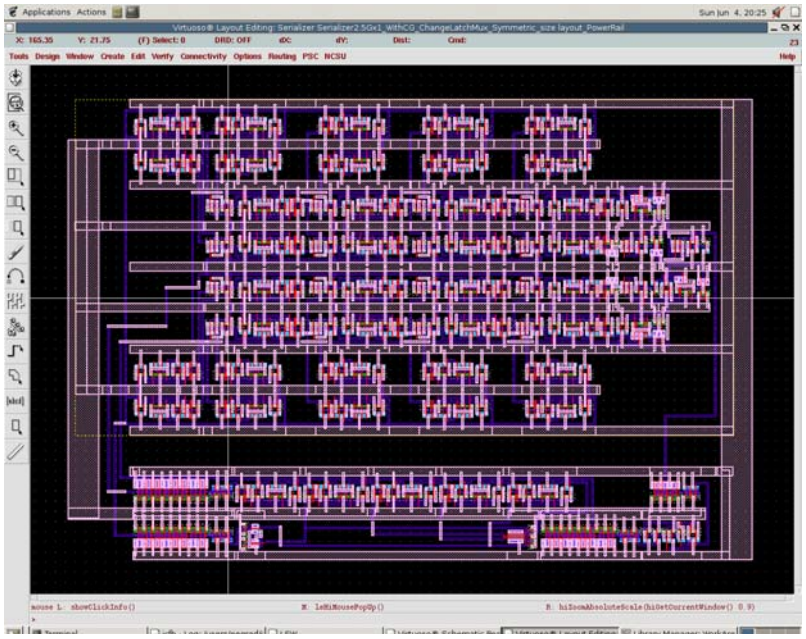


Figure 7, the Serializer design and layout.

Preliminary simulation results indicate that this Serializer can run at 3.125 Gbps speed. This design is now been integrated with the PLL design. We are fine tuning timing at each stage of the design.

So far we have not employed ELT layout in LoCV1. We are waiting for the test results of the test chip and parameters measured on it to guide us in the design simulations. Preliminary attempts to model ELT in Cadence prove to need a lot more work and we need the parameter measurement results to check our modeling. So far we are very much limited by manpower. For the first prototype, we will have a very conservative goal to just prove the concept of Link-on-Chip, and add rad-hard layout in later prototypes if our manpower availability does not allow us to have results before the submission of LoCV1.
The current plan is to submit this LoCV1 chip to Peregrine for fabrication at the end of this year or early next year, depending on their foundry schedule.

3. Plan for 2007

We plan to carefully evaluate LoCV1 in lab, and in radiation if we are able to employ rad-hard layout in its design. In order to evaluate LoCV1 in the link system, carrier board needs to be constructed. The complicity of the test system depends on whether LoCV1 runs at 2.5 Gbps or 3.125 Gbps, and whether ELT is employed in the design and needs to be tested or not. If it runs at 2.5 Gbps, our current test system for the GOL test can cope with this speed, otherwise a receiver board needs to be identified or constructed. If radiation tests are needed, special arrangements on the carrier board need to be taken into consideration in order to separate the chip under test from the rest of the active components, also a fiber needs to be securely attached to the chip, not coupled through a stage as it would be in a lab test environment.

According to the original proposal, we also plan to start designing the 2nd version of LoC (LoCV2) in the summer of 2007. This of course depends on the test results from LoCV1.
Based on the experience we have now, we realize that it takes a lot more engineering time than we initially estimated to design both the chip and its testing system, especially because the test system needs to cope with the irradiation test environment. System lab debugging also takes

more time than we initially anticipated. Our group has three EE graduate students and they all work in various aspects (design, modeling, simulation and verification) of the LoC design. We plan to take in one more student who can work both on chip design and in lab testing. We try to use SMU's TA support for 1.5 students and request RA support and summary salaries here for the students. Because of these considerations, we propose a revised budget requirement for the FY 2007.

FY07:

1. Laboratory tests and irradiation tests on LoCV1.

1.1 LoCV1 carrier board design.
Jan. 2007 – March 2007, work done at SMU

3 month FTE	$13k, w/ 25% benefit, 45% oh	➔	$23.6k
PCB fab. + assembly	$4k		
Components	$1k		
	w/ 45% oh	➔	7.3k

1.2 Laboratory tests.
April 2007 – May 2007, work done at SMU

2 month FTE	$8.7k, w/ 25% benefit, 45% oh	➔	$15.7k
2 month of one EE graduate student		➔	$5k

1.3 Preparation for Irradiation tests: special DAQ, supporting jigs and shielding.
May 2007, work done at SMU

1 month FTE	$4.3k, w/ 25% benefit, 45% oh	➔	$7.9k
Material cost	$2k, w/ 45% oh	➔	$2.9k

1.4 Irradiation tests using Co-60 gamma source, 200 MeV proton beam, including data analysis.
June 2007 – July 2007, work done at SMU with trips to radiation sites

2 months FTE	$8.7k, w/ 25% benefit, 45% oh	➔	$15.7k
3 month of 3 EE graduate student summer job.		➔	$11.7k
Proton beam (MGH) time	$600/hr*5hr = $3k		
Travel to BNL + Boston:	$2.5k*2 = $5k		
	w/ 45% overhead, total	➔	$11.6k

2. Design, layout and fabrication of LOC version 2 (LoCV2).

2.1 Chip, with the receiving side, design and layout.
July 2007 – Dec. 2007, work done at SMU

1 month PI (Ping Gui) summer salary	$8.6k w/ 25% benefit, 45% oh	➔	$15.6k
6 months of three EE graduate students		➔	$45k

2.2 Chip fabrication including flip-chip bonding.
Dec. 2007, work done by Peregrine

MPR submission fee:	$30k		
Flip-chip bonding:	$15k		
	total	➔	$45k

3. Prepare for LoCV2 tests.

3.1 Test circuit design and PCB layout.
Aug. 2007 – Sept.2007, work done at SMU

2 months FTE	$8.7k, w/ 25% benefit, 45% oh	➔	$15.7k

3.2 PCB fabrication.
Oct.2007 – Nov.2007, work done by Eagles Circuits

PCB fab. + assembly	$6k		
Components	$2k		
	total w/ 45%	➔	$11.6k

Total for FY07: ➔ $234.3k. In which, Material and supply is $71.1k, manpower $155.9k, travel $7.3k

4.3.4 Development of a Readout Driver Module for the upgrade of the LAr Calorimeter Front-End Readout

WBS: 4.3.4

Design of a Next Generation Read Out Driver (ROD) for the ATLAS Liquid Argon Calorimeter Upgrade

Brookhaven National Laboratory, Upton, NY 11973-5000
University of Arizona, Tucson, AZ 85721
June 20, 2006

7. Motivation of ROD R&D

The LHC upgrade (SLHC) is proposed to reach a factor of 10 more luminosity than present LHC, which implies different radiation environment, bunch-crossing rate, data throughput, trigger bandwidths and latencies etc. Liquid Argon (LAr) Calorimeter Front End Board (FEB) is designed for present LHC machine, the next generation FEB has been proposed for these new requirements of SLHC, at the same time, new optical link design is also proposed to accommodate the high data output bandwidth between FEB and ROD.
ROD is the vital part of the Back End Electronics System, which is crucial to data acquisition because it is the bridge between Front End Electronics System, Read Out System (ROS) and Trigger System. With the requirements of higher bandwidth, higher bunch-crossing rate etc, the current LAr ROD is not going to work in SLHC, we propose to follow up and evaluate the new implementation methods for signal processing, develop and upgrade ROD to make the Back End Electronics system consistent with the upgraded Front End Electronics system.

a) Digital Signal Processing (DSP)

The LAr ROD is mainly composed of Mother Board (MB), Processing Unit (PU) with some other additional accessorial parts. Each Mother Board can have four PUs plugged on as mezzanine boards, it receives data from at most 8 FEBs and sends the results of the optimal filtering algorithm calculations to the Transition Module (TM), which sends data to ROS through S-Link. PU is the data processing core of the ROD, it is implemented base on TI DSP TMS320C6414, and each PU has two DSPs and can process data from 2 FEBs.
In SLHC, higher bunch-crossing rate and data output bandwidth implies requirement of higher data processing capabilities to ROD. Over the years high-end digital signal processing solutions meant only traditional DSPs, such as Analog Devices TigerSHARC series and TI C6x series. Recently AltiVec PowerPC-based systems are firmly entrenched as an alternative to traditional DSPs. Now another prong of DSP functionality has crept into mainstream use: powerful FPGA-based DSP systems, which support user-programmable hardware configuration and on-the-fly reconfiguration.

There are a number of good reasons to consider using FPGA for DSP:

- Need for increased performance. FPGA can provide increased performance mainly because they can be configured with a custom hardware design, implementing control logic in the hardware. Precious clock cycles will not be used implementing control functionality like DSP usually does. User can choose the hardware architecture. If speed is top priority, a fully parallel approach for the data processing algorithm can be designed in FPGA.
- FPGA is already widely used in system design. For example, LAr ROD has 3 FPGAs on each PU and at least 10 FPGAs on Mother Board. If we implement DSP functionalities in these FPGAs, the ROD design will be optimized and simplified in a great deal, this provides cost savings for the system and reduces system real estate and power.
- DSP functionality of FPGA is ramping up. Two leading FPGA vendors, Altera and Xilinx, continue to ramp up the DSP functionality of their high-performance chip families. Altera Stratix II DSP Blocks are capable of running at 420 MHz and provide very high DSP

throughput (up to 322 GMACs) that is orders of magnitude higher than competing DSP processors available today. The largest Stratix II device, the EP2S180 device, has 96 DSP blocks that offer a throughput of 322 GMACS and can support up to 384 18x18 multipliers. Xilinx Virtex-4 is embedded up to 512 XtremeDSP slices running at 500 MHz, up to 256 GMACs performance. Both can provide more than 20 times the data throughput available from leading DSP devices.

- There are a few other advantages to use FPGA instead of DSP, for examples, there are many off-the-shell commercial algorithm IP available; both Altera Stratix II and Xilinx Virtex-4 are designed with 90-nm technology, which can dramatically reduce the system power consumption; moreover, the development tools (Matlab etc.) are rich and proven, in contrast, tools for ADI's TigerSHARC and TI's C6x DSPs are more esoteric and limited.

b) High Speed Serial Bus (PCI Express)

The speed of data path on LAr ROD is limited (80MHz 16bit) by link between staging FPGA and input FPGA, link between input FPGA and DSP etc. PCI Express is a new high performance serial PCI local bus, which is also far faster than local bus bandwidth (160 megabytes per second) on LAr ROD and S-Link (800 megabytes per second). The bandwidth of the traditional PCI local bus is shared between the PCI modules in the system, PCI as it exists today has some serious shortcomings that prevent it from providing the bandwidth and features needed by current and future generations of I/O and storage devices. Specifically, its highly parallel shared-bus architecture holds it back by limiting its bus speed and scalability, and its simple, load-store, flat memory-based communications model is less robust and extensible than a routed, packet-based model. PCI Express (PCIe) is the newest name for the technology formerly known as 3GIO, PCIe's most drastic and obvious improvement over PCI is its point-to-point bus topology. Each PCIe module in the system has direct and exclusive access to the bus switch, in other words, each module sits on its own dedicated bus, which in PCIe lingo is called a link. Each link is composed of one or more **lanes**, and each lane is capable of transmitting one byte at a time in both directions at once. A link that's composed of a single lane is called an x1 link; a link composed of two lanes is called an x2 link; a link composed of four lanes is called an x4 link, etc. PCIe supports x1, x2, x4, x8, x12, x16, and x32 link widths. PCIe's bandwidth gains over PCI are considerable. A single lane is capable of transmitting 2.5Gbps in each direction, simultaneously. Add two lanes together to form an x2 link and you've got 5 Gbps, and so on with each link width. In nowadays, PCIe has been widely adopted in PC system as a new graphics card interface, Gigabit Ethernet card etc.

Both Altera and Xilinx have announced the FPGA PCI Express solution last year. If we can take advantage of PCI-Express, which will make the ROD more powerful to process higher volume data from FEB with higher data rate, each ROD can process data from more FEBs that can reduce the number of ROD and total cost.

c) High Speed Optical Link & SERDES

We will use high speed optical link to transfer data from FEB to ROD, since the next generation FEB will be all digital design, with 40MHz 16bits sampling on 128 channels, each FEB will need 81.92Gbits/sec data throughput. Parallel fiber will be a good choice to implement this high speed data link, industry standard parallel fiber MPO/MTP connector is a good candidate, which has 12 fibers and is about 15mm wide.

To interface with high speed optical link, SERDES is another crucial part to the design of next generation ROD, FPGA is playing a leading role on integration of the high speed SERDES, RocketIO X of Xilinx provides 10.3125Gbps transceiver and Stratix II GX from Altera has 6.375Gbps transceiver. Considering limited board area, power consumption and

high density integration of SERDES, FPGA is better than discrete SERDES chips as it can provide multiple high speed SERDES in a single chip, plus its programmability, it is a very versatile design platform.

d) AdvancedTCA System Architecture

PICMG (The PCI Industrial Computer Manufacturers Group) is a consortium that has standardized ISA and PCI technologies for industrial backplane applications. It compiled many specifications that define complete hard ware architectures, including physical board sized, backplane layout and protocols and power, thermal issues. PICMG 3.0 defines AdvancedTCA (The Advanced Telecommunications and Computing Architecture) system, which has a few very important features. For example, AdvancedTCA will utilize multi-gigabit serial transport instead of traditional parallel buses, AdvancedTCA also defines large form factor (8U) and power budget, each card can consume 200W and total 16 cards per crate. PICMG 3.4 defines how PCI Express and PCIU Express Advanced Switching transport is mapped onto PICMG 3.0, with this system architecture, we can take advantages of both PCIe and high performance backplane for our ROD development.

AdvancedTCA has several advantages over the VME system the current ROD is using. AdvancedTCA provides higher data throughput by serial interface and mesh or dual-star topology, and also provides the possibility for communication between RODs, which can be utilized for energy calculation and trigger generation.

e) Gigabit Ethernet

Gigabit Ethernet is one of the communication protocol supported by AdvancedTCA platform. Commercial Gigabit Ethernet Switch module is already available in AdvancedTCA platform, the implementation of Gigabit in FPGA is a very interesting part for ROD design. With Gigabit Ethernet interface implemented in FPGA on ROD, ROD can be configured remotely from any host PC through Gigabit Ethernet.

8. Work of FY06 for FY07

In FY06, we have started the following works even if the funding arrived late.

2.1 Study of ROD data rate

The new FEB baseline design would digitize and transmit all samples from 128 calorimeter cells at 40MHz. The data rate from each FEB will be 128channels x 40MHz x 16bits=81.92Gbps, with 8B/10B encoding overhead it will reach 98Gbps. With this huge amount of data, single fiber optic is not able to handle, we have to split data on multiple fibers. Industrial standard parallel fiber connector MPO/MTP that is 15mm wide and has 12 fiber channels is a good candidate. With 12 parallel fibers, each fiber channel needs to transfer data at 6.825Gbps (8.2Gbps with 8B/10B overhead).

2.2 Study of ROD architecture

Since ROD will have very high data rate, design of ROD will be a challenging. The SERDES is a crucial part on ROD, how to implement it on ROD will affect the whole architecture of ROD. If we use external SERDES, ROD will be like

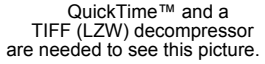


Figure 1. ROD architecture with external SERDES

With high speed differential I/O available in FPGA now, we can take advantage of the internal SERDES and dynamic phase alignment technology that is used to recover the sampling clock on FPGA. In this way, ROD design will be simplified to

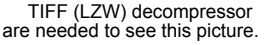


Figure 2. ROD architecture with internal SERDES in FPGA

Now, both Altera and Xilinx offer high speed transceiver and embedded SERDES with speed up to 6.5Gbps, which provide a good start point for ROD design.

Based on these two different architectures, we have created two possible parts layouts for the upgraded rod to see if there was a space issue.

2.3 DSP Algorithm in FPGA

We started to evaluate the DSP performance in FPGA, we purchased Altera DSP evaluation board, and trying to implement and test DSP algorithm in FPGA. Since Xilinx offers DSP functions and PowerPC core in FPGA too, and PowerPC has AltiVec efficient instruction set, we would also like to evaluate the DSP performance of Xilinx FPGA.

2.4 ROD Level 1 Trigger Sums

Another main interesting point in ROD upgrade is study if the level 1 trigger sum can be implemented digitally on ROD. If so, we can completely bypass the front end analog trigger chain. We take the EM barrel as start point to evaluate the trigger summing latency.

From the simulation, we might be running a little bit tight of the level 1 trigger total latency (2.5us). Further investigation will be followed.

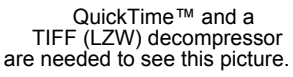
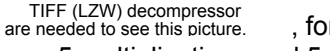


Figure 3. Level 1 Trigger Sum on ROD

2.5 Energy and Timing Calculations

Energy and Timing calculations are performed in FPGA at 100KHz level 1 trigger rate, calculations for all channels can be done independently and in parallel. To calculate energy using optimal filtering weights: 

, for 5 samples, each energy calculation requires 5 subtractions, 5 multiplications and 5 additions, total will be less than 150ns, actually Altera Stratix FPGA can perform 18x18-bit multiplication more than 300MHz.

2.6 System Level Consideration

The whole ROD system has to provide system monitoring function, can easily download system configuration and also have scalabilities, in case of 14 FEBs can not map to a single ROD, level 1 trigger sum will need communication between RODs.

PICMG 3.0 defines AdvancedTCA platform, which has multiple gigabit serial transport on backplane, 8U form factor and 200W power budget for each card, a system can have up

to 16 cards and consume 3kW without thermal problem. We have one AdvanceTCA crate in the lab and are evaluating its performance.

9. Plan for FY07

We plan to evaluate a number of commercial FPGAs to see if their DSP functionalities satisfy SLHC requirements, at the same time to evaluate PCI Express to see if they can be adopted on ROD system. BNL ATLAS group has finished ATLAS LAr FEB Production Test, a number of people involved in these programs and their expertise will be very important in the new ROD design. We propose the following work plan for FY07.

FY07:
We will evaluate the performance of FPGA-DSP and high speed SERDES in FPGA, evaluate the high speed optical link with parallel fiber. We will also evaluate AdvancedTCA architecture and test the performance of PCI Express in the AdvanceTCA system. We will design a sub-ROD that can take data from LAr FEB or serial data source, this sub-ROD has DSP algorithm implemented in FPGA, we can evaluate the performance of this algorithm. The sub-ROD could be an AdvancedTCA module, it can take the advantage of PCI Express on the backplane for data transportation, in this way, and we can test the communication between 2 RODs. We will evaluate Gigabit Ethernet implementation in FPGA and see if ROD can take advantage of it. To test sub-ROD module, we will design a ROD-tester module, which will be used to evaluate the optical communication of ROD and data processing on the ROD.

10. Personnel

BNL:

Physics Department	
Francesco Lanni	System design, DAQ, Test
Hucheng Chen	ROD Design, Layout, Test
David Lissauer	Coordination, Integration
Instrumentation Division	
Joe Mead	PCI Express, Simulation
University of Arizona	
Ken Johns	ROD tester design, Gigabit Ethernet
Joel Steinberg	ROD tester design, Optical Receiver

11. Institutions

Brookhaven National Laboratory, Upton, NY
University of Arizona, Tucson, AZ

12. Budget Summary

For FY07

Item	num	materials	total	hours	labor-cost
1. Sub-ROD board (BNL)					
1.1 Design/Layout				250	$20,000
1.2 NRE	1	$2,500	$2,500		
1.3 100% Electrical Test	1	$3,000	$3,000		
1.4 Fabrication	4	$1,650	$6,600		
1.5 Assembly				100	$8,000
1.6 Components	1	$34,400	$34,400		
2. FPGA Development (BNL)					
1.1 Xilinx ISE	1	$3,000	$3,000		
1.2 Altera SERDES Ev Brd	1	$2,000	$2,000		

	1.3 Xilinx ATCA Eval Brd	1	$6,000	$6,000		
	1.4 Xilinx DSP Eval Brd	1	$2,000	$2,000		
	1.5 Xilinx SERDES Ev Brd	1	$3,000	$3,000		
3.	Testing equipment (BNL)					
	3.1 AdvancedTCA Crate	1	$5,500	$5,500		
	3.2 ATCA Controller	1	$1,500	$1,500		
	3.3 Power Supply	1	$2,500	$2,500		
	3.4 PC	1	$2,400	$2,400		
4.	PCI Express (BNL)					
	4.1 PCI Express Spec.	1	$1,000	$1,000		
	4.2 PCI Express Eval Brd	1	$1,700	$1,700		
5.	Laboratory Test (BNL)					
	5.1 Test and Debug				250	$20,000
6.	Evaluate GBIT Ethernet using FPGA (AZ)					
	6.1 Nios II Dev Kit	1	$1,260	$1,000		
	6.2 PC to use in testing	1	$1,260	$1,000		
	6.3 Nios II Software (OS)	1	$1,260	$1,000		
	6.4 Altera Technical Training	1	$1,000	$1,000		
7.	Evaluate Receiver for ROD (AZ)					
	7.1 Purchase Eva. Kit	1	$3,000	$3,000		
	7.2 Purchase Fiber Cable	1	$500	$500		
	7.3 Purchase Eva. Units	1	$1,000	$1,000		
8.	Build ROD Tester (AZ)					
	8.1 Parts for first unit	1	$1,500	$1,500		
	8.2 PCB for first unit	1	$2,000	$2,000		
	8.3 Assembly	1	$500	$500		
	8.4 Parts for prototype	1	$2,000	$2,000		
	8.5 PCB for prototype	1	$3,000	$3,000		
	8.6 Assembly	1	$1,000	$1,000		
	8.7 Testing				125	$10,000
	Sum		$95,600			$58,000
	Total $153,600					

4.3.5 Design and Development of Low Voltage Power Supply for the upgrade of the LAr Front-End Electronics

WBS: 4.3.5

Development of Radiation Tolerant Power Supply Upgrade for ATLAS Liquid Argon Front End Crate

Brookhaven National Laboratory, Upton, NY 11973-5000

A proposed upgrade to the LHC will increase luminosity by a factor of 10 with a corresponding increase of radiation levels. This will require retesting and redesign of the power supply for the Liquid Argon Front End Crate. The current power supply is located above the Front End Crates in the gaps of the Tile fingers. The high currents needed by the front end crate make it impractical to locate the power supply further away in a less harsh environment. The present design will be tested to the anticipated radiation requirements and will be radiation hardened to meet the new environment. It is anticipated that the total power requirements will remain essentially the same.

Present and Anticipated Requirements

The present design of the Liquid Argon Front End Crate power supply uses commercial off the shelf components that have been tested and qualified for the computed radiation and magnetic field environments for the present LHC luminosity. A luminosity increase of 10 fold or more could present significant design challenges. The greatest anticipated effect would be in radiation damage in the DC-DC converters of the power supply. Using the same safety factors as in the present generation the TID requirement could rise to 4500 Gray. In commercial DC-DC converters the vulnerable components include the switching power MOSFET and the control ASICs. It might be necessary to replace the MOSFET with a radiation hardened version from a company like International Rectifiers. The ASICs could be re-engineered with a silicon-on-sapphire version or some other radiation tolerant technology. This approach has been used in the past for radiation hardening DC-DC converters manufactured by Vicor Corporation.

Another challenge in the power supply system is the high power density that it is required caused by the lack of space. Here, it is assumed that the power requirements of any upgrade to the power supply will remain the same due to the constraints of the cooling system. Potentially the power density and waste heat generation could be improved over the present design if Vicor Corporation or similar manufacturer's products could be used instead of the present generation of power modules produced by Modular Devices Inc.

Upgrade Strategy

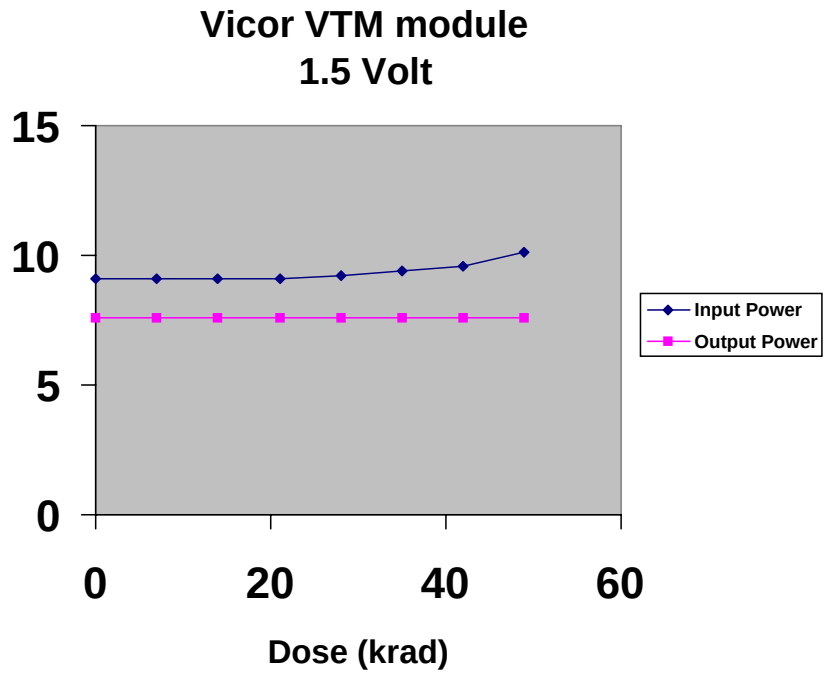
It is not known if the present power supply produced by Modular Devices Inc. would qualify in the increased radiation environment of an LHC upgrade. The power modules were tested in the past up to a total ionizing dose of 3000 Gray with one failure. When production and installation of MDI power supplies end in 2006, modules from either the company or from one of the existing current generation power supplies could be tested to the new radiation environment specifications. At the moment there is no intention to collaborate with the company in the development of any new products.

In parallel, converters from other commercial manufacturers would be tested in the same way. Two companies have been selected to date. These are Vicor Corporation and Wiener. Vicor produces power supply products that are very efficient and have very high power densities. The downside is that there is little data on radiation tolerance or behavior in magnetic field environments. Wiener has developed a product line (Maraton HHE) that has been tested in ionizing radiation environments of up to 722 Gray and in magnetic fields of 1200 Gauss.

After the modes of failure have been determined specific components would be targeted for radiation hardening. The power MOSFET can be replaced by a radiation hard version or potentially by a different approach such as using a p-channel FET rather than an n-channel FET. Also, as stated above control ASICs can be re-engineered in a more radiation hard technology or replaced with one that is already proven to be rad-hardened. Other components can be hardened or replaced when identified. This process will go on through FY07 and FY08 and perhaps beyond this.

WORK TO DATE FOR FY06

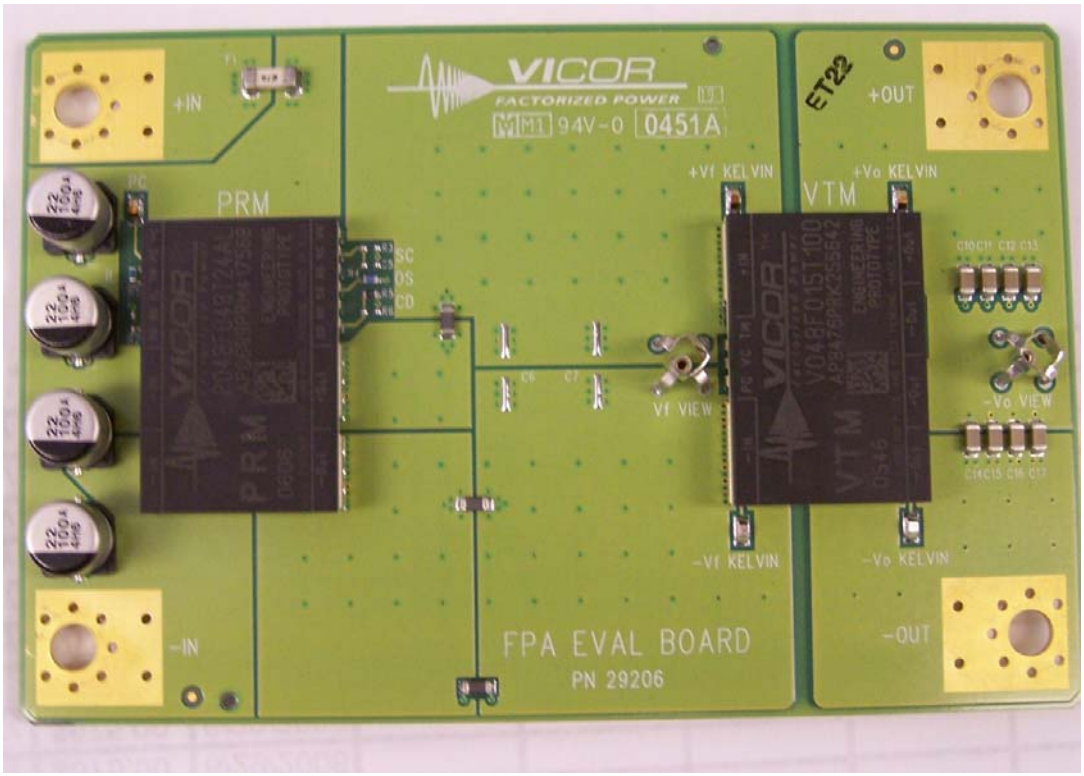
The possibility of using components from Vicor Corp. factorized power architecture has been investigated. Irradiation testing has been started on two of the products. One was a single Vicor VTM module powered from a regulated 48 volt power supply. The VTM module provides isolation but no regulation. The input was monitored and the irradiation was interrupted at selected doses when the output was measured. The result is shown below.



Note that the input current (power consumption) increases with dose. At a total dose of between 500-600 Grays the input current dropped to zero.

A test board was purchased from Vicor which is made up of a pair of modules which together give a dc-dc converter which takes a 36-75 volt dc input and provides a regulated and isolated lower voltage output (see picture below). This board again had a VTM module but in addition had a second Vicor product called a PRM module. The PRM module provides regulation and can be powered from a voltage of up to 75 volts dc and VTM modules. Again a failure occurred at a little more than 500 Gray. This failure occurred when the power to the

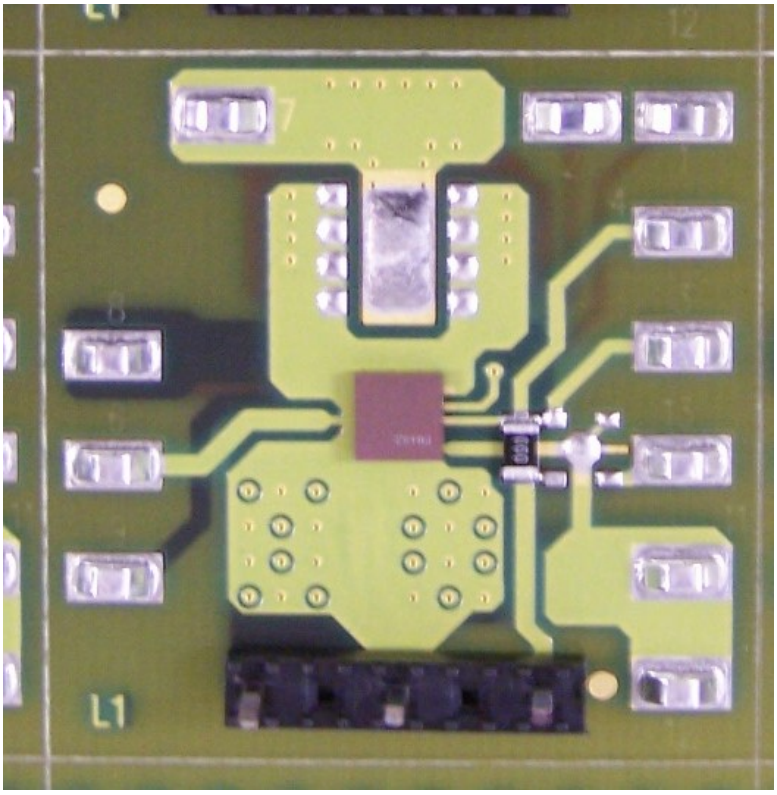
board was recycled. The VTM module from the first test and the evaluation board from the second test have been returned to Vicor for failure analysis.



Vicor Corporation has been very supportive in providing samples, engineering support and failure analysis in this effort.

A similar evaluation board was used in a noise test. The board was used to power the -4 volt input of a current generation FEB board to test for coherent noise and provided a satisfactory result. In process is a prototype board that would provide +4, -4, +11 and +6 using two pairs of PRM and VTM Vicor modules in parallel for each voltage. This would give data on both the behavior of the modules when operated in parallel and on the noise characteristics in powering multiple FEB board(s).

Another test board was designed/produced by Vicor Corporation for the testing of the MOSFET switches that are used in their product line. Shown below is one of 10 test boards provided by Vicor Corporation. In the center is the MOSFET used by Vicor in VTM modules that produce 4 volts or greater. An ionizing irradiation test is scheduled to test the radiation effects on this component and if necessary start on steps to replace it.



Also, depending on the results of the ionizing radiation tests additional tests may be conducted on neutron effects or SEU effects. Because of the lower voltage that these MOSFETs are operated at compared to MDI modules there is good reason to believe that these parts would be immune to Single Event Burnout but that has to be verified.

We are also investigating the Maraton HE power supply system from Wiener. A crate plus two voltage modules was purchased to start. As stated earlier this product line has the advantage of having already been tested in radiation and magnetic field environments. In summer, FY06, this unit will be tested to a gamma dose equal to that anticipated in the upgraded LHC and in a magnetic field environment to verify the data from the manufacturer.

Goals for FY07

As described above in FY06 we are designing and producing a small prototype power board for the testing of Vicor modules. This will be used for determining the small scale current sharing and noise behavior of modules operating in parallel. In late FY06 or early FY07 this will be finished. Depending on the result a second larger prototype is planned. This would include enough voltages and modules to allow a reasonable simulation of what we might encounter in a power supply that would power a crate.

It is already clear that Vicor products will not meet the radiation tolerance requirements for the upgrade. Starting in FY06 and continuing into early FY07 it is necessary to identify the radiation sensitive components in the product line. The goal would be to find radiation hard replacement components or estimate the cost of engineering/producing radiation hard components. This needs to be accomplished early to determine whether this approach is feasible.

In parallel the product line from Wiener will be investigated. Testing that commenced in FY06 will continue into FY07. Specifically, the vendor reported qualifications for radiation and magnetic field will be confirmed and extended to the anticipated values for the upgrade. This includes single event testing and neutron testing. If the product line meets the environmental qualifications then a dialogue would be started with Wiener to produce a product in the form we require. This would require the production of an individual power converter for testing purposes.

Budget Request

FY07

Salaries (0.75 FTE Tech.)	$90,000
Material costs	$30,000
Radiation Testing	$30,000

Total Requested for FY07 is $150,000

WBS 4.5

Proposal to U.S. ATLAS for LHC Upgrade R&D in FY07
Pulsed Mode Radiation Backgrounds Monitors for the ATLAS Muon System

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Purpose and Goals

In summer of 2004, the Arizona group initiated a project within ATLAS to measure radiation backgrounds in the muon system soon after startup in 2007. This is a natural follow-on to the simulation studies of these backgrounds done by Arizona since 1998, providing a majority of the information used by the ATLAS Radiation Task Force and by the ATLAS shielding engineering group during detector shielding development and construction.

ATLAS radiation backgrounds will degrade detector and trigger performance, cause detector and electronics damage, and induce digital upsets that can corrupt the data. These backgrounds, and their effects, have been simulated extensively since the early 1990's using various event generators and particle transport codes. This effort involved extensive input from ATLAS collaborators from all detector subsystems, and since mid-2000 was organized and carried out by the Radiation Task Force, which completed its Summary Document early this year (ATL-GEN-2005-001). Despite the time and care put into these studies, there are still large "safety factors"—in the range 2.5 to 5.0 for the muon system—associated with the predicted rates. They reflect uncertainties caused by (1) running the event generators and transport codes at LHC energies, (2) simulating calorimeter and shielding depths that are much larger than those in existing collider experiments, (3) simplifying the ATLAS geometry and materials specifications to make the calculations tractable, and (4) using neutron and photon cross section tables that continue to evolve from year to year.

Backgrounds simulations have focused on the engineered ATLAS baseline design for 2007, operating at the full luminosity of $10^{34}/cm^2/s$. It is the judgment of the Radiation Task Force that the experiment will "just operate" at full luminosity if the true backgrounds turn out to be at the simulated rates multiplied by the upper limits of their corresponding safety factors.

The Arizona radiation monitors project has two purposes:

1. To measure the neutron and photon backgrounds at various places in the muon system to assure that standard running at 10^{34} will not be a problem.
2. To apply this knowledge to extrapolate the background to operation at the Super-LHC, at a luminosity of $10^{35}/cm^2/s$.

One sees immediately that there is a problem when planning for operation at an upgraded LHC luminosity. If the true rates are at the upper limit of the safety factors, this implies the need for major detector and shielding upgrades. At the opposite extreme, if true rates are at or below the simulated rates, minor upgrades (or no upgrades) may be needed in the muon system. The truth probably lies somewhere in between. But timescales for detector upgrades are long, and we cannot improve our knowledge simply by further simulation, so direct measurement of the backgrounds is of critical importance.

Monitor Types and Placements

At Arizona, we have constructed four sets, each containing a group of pulse-mode monitors sensitive to neutrons and photons at specific points in their spectra. These sets will be placed at distinct locations in the muon system, each seeing a different combination of secondary sources and having a different mix of background components. Some monitor pulses will be discriminated and counted, and others will be pulse-height analyzed. But all should be sensitive to fluxes of a few Hz/cm^2, making measurements possible shortly after ATLAS startup.

Each set will contain an array of six or seven pulse-mode detectors, chosen to respond to photons or neutrons of various energy ranges. We have purchased the following detectors, and have tested and calibrated them with standard gamma sources, as well as neutron sources (PuBe and ^{252}Cf):

(1) Thermal and slow neutron (< 10^{-5} MeV) gas detector: boron lined proportional tube filled with argon/CO2 gas (sealed). Each interaction n + ^{10}B → Li + α sends either a slow Li or α into the tube. The cross section for this reaction falls as 1/v of the neutron. The large ionization pulse associated with the Li or α is used for pulse-height discrimination against Compton electrons and MIP's, making this detector relatively insensitive to photons and charged particles.

(2) Thermal and slow neutron scintillators, two monitors: Plastic detectors can be prepared in various ways to detect thermal neutrons. We have purchased (a) a boron loaded plastic scintillator, BC-454, sensitive to the reaction products listed above, and (b) a plastic disk coated with a thin layer of ZnS(Ag) scintillator, loaded with ^{6}LiF, and sensitive to the ^{3}H- and α reaction products due to thermal neutron capture by lithium.

(3) Fast neutrons (few MeV or greater), two monitors: These detectors contain hydrogen, from which incoming neutrons scatter to produce recoil protons. These protons will ionize heavily compared to MIP's or low energy electrons, allowing for schemes that give good discrimination against these backgrounds. We have purchased two monitors for this energy regime, one traditional and simple, the other requiring sophisticated pulse-shape analysis:
(a) ZnS(Ag) scintillator in plastic, with pulse-height discrimination. Traditional.
(b) Liquid scintillator, with pulse-shape discrimination (PSD) electronics.

(4) Low energy photon spectrum, (0 to 10 MeV), two monitors: The spectrum will be dominated by photons, but also contains an overlaid neutron spectrum—typically containing more "features". As in test beam runs, these will be separated by simulation and fitting. The two monitors are:
(a) A 1 x 1" NaI crystal.
(b) An LSO crystal of same dimension, St. Gobain PreLUde420 with increased light output, greater radiation resistance, and higher density to extend the effective energy range.

(5) Ionization chamber: Total ionizing dose is an important measure of overall background activity and energy flow. Such a chamber is read by a sensitive ammeter connected via triaxial cable. (We have not had sufficient funds to purchase an ion chamber yet.)

Each set has its own coaxial cables, both signal and high voltage. The cables are routed to a rack in the ATLAS side cavern, USA15, where the pulse analysis and counting equipment reside. For simplicity and flexibility, the components in each box are kept to a bare minimum. The sets are being placed at the following locations:

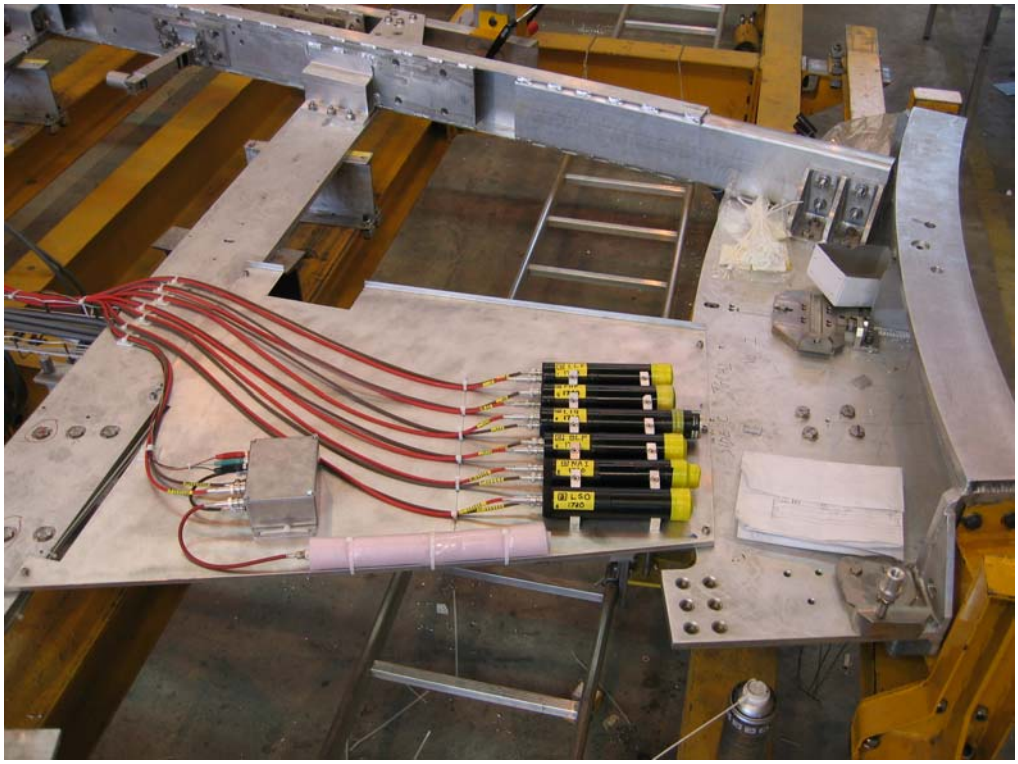
(1) The CSC region of the Small Wheel, nearest the beam. (Winter, 2007.)

(2) Big Wheel TGC1, nearest the beam. (Mounted Feb/06 in TGC1 sector.)

(3) Big Wheel TGC2, at slightly larger radius. (Mounted July/06 in TGC2 sector.)

(4) The TAS collimator region. (As soon as cableways are ready for loading.)

Monitor set installed in Big Wheel sector 7 of C-End TGC2. July 6, 2006.



The original 2005 proposal provided for four monitor sets , and did not include the TGC2 set at location (3) above. But George Mikenberg argued that one is needed at this location to allow for comparison with chip-based dose monitors (Mikuz et al.). So we shifted a set originally intended for installation in USA15 to TGC2.

The USA15 location is important since it is a region to be accessed during running. The rates are expected to be close to the maximum allowed for access, and the backgrounds must be understood in detail. (The standard dose monitors are insufficient for "unfolding" the backgrounds.) We are requesting funds in FY07 for an additional monitor set to place in USA15.

Also, more recently, Frank Taylor argued that a set was needed for the barrel muon because of the sensitivity of RPC's in this region to relatively low background fluxes. The hottest spot in the barrel muon region is at the exit to the large gap between barrel and endcap cryostats—a region that is notoriously difficult to simulate. Our proposal is to put a monitor set near the exit to this gap.

In summary, we are proposing to extend the above list of sets as follows, with modest funding for FY07:

(5) USA15 side cavern, just inside wall. (When DAQ goes to CERN, early 2007.)

(6) Barrel muon region, outside gap. (Mounted as soon as possible.)

Progress to Date

This project has been under way since early summer of 2005, funded as a U.S. ATLAS LHC Upgrade R&D Project at the University of Arizona**.** Michael Shupe and Leif Shaver are the primary workers, with some undergrad and graduate student help.

We received $50K of U.S. ATLAS LHC funding for FY 2005/06. With this we acquired the rack-mount data acquisition computer to be placed in USA15, a pulse-height analyzer, and a fast transient recorder for PSD analysis. Both of these measurement devices are controlled and read by the computer, which can be operated locally or remotely. Scintillation detectors and proportional tubes were purchased for four monitor sets, which have been assembled and tested at Arizona.

Installation progress is most easily seen by referring to the Baseline Dates listed in our 2006 MOU:

Muon Upgrade R&D: WBS 4.5

Description	Baseline	Actual
Install monitors and cables on TGC1 wheel	2/20/06	2/19/06
Install monitors in TAS region, with full cabling to USA15 data acquisition rack	6/15/06	(10/15/06)
Commission data acquisition system in USA15 rack using TAS monitors	6/30/06	(10/15/06)
Install monitors and cables on TGC2 wheel	8/15/06	7/6/06
Install monitors and cables on CSC wheel	10/15/06	(2/20/07)
TGC1, TGC2, CSC cabling through chains	1/15/07	(various)
Begin full monitor commissioning	2/15/07	(5/20/07)

The monitors for the TGC1 Wheel (End C) were mounted one day ahead of schedule in February, 2006. The TGC2 Wheel sector assembly happened a bit sooner than we had anticipated in the baseline, so these monitors were shipped to CERN and installed on July 6, 2006. (We have put revised future installation dates in parentheses.) Because monitor testing and installation have been intense this spring, we will delay taking the DAQ system to CERN until October, 2006. Delays in CSC assembly have forced us to plan for installation of its monitors in early 2007. The last items on the list will occur as ATLAS installation progresses. The main point to be taken from this is that we are proceeding very much in step with the baseline dates. This radiation backgrounds monitoring system will be fully operational in time for first collisions.

Individuals and Responsibilities

Michael Shupe, Professor – Participating in all phases of project.
Leif Shaver, Engineer – Design, fabrication, installation at CERN.
Graduate Student – Data taking, simulation, and analysis. (Supervised by Shupe)

Budget

The attached tables detail the expenditures to date (including indirect costs), and the funding request for FY07.

Expenditures for FY 2005/06:

Four monitor sets for cavern (CSC, TGC1, TGC2, TAS)		$ 28,500
Cabling and connectors		4,500
USA15 DAQ: rackmount PC, PHA, transient recorder		17,000
	Total	**50,000**

Proposed Budget for FY 2007:

Monitor set for barrel muon region (F. Taylor)		$ 7,500
Monitor set for USA15 wall		7,500
Flex chain cables, and cabling to USA15		2,500
	Total	**17,500**

Budget Explanation

The justification for the fifth and sixth monitors set was discussed at the end of the "Monitors Type and Placements" section. The monitor set costs cover scintillation crystals and photomultiplier tube assemblies. The third item, cabling, connects these two monitor sets to USA15.