Project Specification
Project Name: ATLAS Binary Chip (ABC)
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Revision History

Revision	Change Description, Pages Revised	Engineer in Charge	Date Approved
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5.00	Changes before second submission: Add some documents to "Related Documents"; Rephrase some Requirements for clarity; Change reference from CAFE-M to CAFE-P; Add third DAC for IVI1; DAC registers cleared by Power-up Reset; Add "en" output in Fig. 3.2.1 & Table 3.2.1a; Add pulseinputreg column to Figure 3.2.1.b; Modify signals in Figure 3.2.9 and Table 3.2.9a; Remove Cal_Enable from Table 3.2.9b and Table 3.2.10; Add DataoutDelay bit to Table 3.2.9b; Fix Table 3.2.10; Spec value of counters after resets; Add test pads and test circuitry to Section 3.2.17; Correct spec of Trailer to "1" + 15 "0"; Expand Erroneous Command Handling Spec; Spec load order of Mask Reg in Table 3.2.19b, note that load order is changed from first chip submission; Spec supply voltage min/max; Add table for power consumption; Correct electrical spec for Hit Input; Add spec for pull-ups/-downs on input pads Add Section for timing specs; Modify spec for IDAR input; Renumber figures and tables by section number; Clean up figure formatting; Improve misc. formatting;	M. French	11-Jan-99
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1. SCOPE

The aim of this project is to develop a chip suitable for the binary readout of the proposed LHC ATLAS Semi-Conductor Tracker (SCT). This chip is to be based on the work already carried out for ATLAS, in particular the DDR2 chip and CDP128 chip. The chip will be designed to interface to the CAFE-P and the DORIC chips. In addition, it must also be compatible with the protocols for receiving and sending data as defined for the ATLAS silicon micro-strip detector. (See Section 2, documents 1, 3 and 14.) While the compatibility to the CAFE-P chip is required absolutely by this design it is noted that the previous version, named CAFE-M, should also be compatible with the ABC in all aspects except in the use of the 4-bit DAC for which the CAFE-M has no compatible connection.

1.1. ATLAS Binary Front End Readout Architecture

The ATLAS binary front-end readout architecture is based on amplifier/discriminator and CMOS pipeline chips. In one configuration this is arranged as two chips, a bipolar amplifier/discriminator chip (CAFE-P) and a CMOS pipeline chip (ABC). The ABC chip reads out 128 channels of silicon strip data from a CAFE-P chip. Data are stored for the duration of the level 1 trigger (L1) latency in a 128 deep 1 bit pipeline. In normal data taking, the data corresponding to hit strips are read out ("sparse" read out). Four modes of data read out are possible: in the Level mode the decision is based on the data in the BC corresponding to the L1 trigger only, but in the Edge mode there must be a "0" in the channel for the bunch crossing preceding the trigger. The efficiency is highest for level mode but the occupancy may be up to a factor of two higher. The optimum mode to run will, therefore, depend on luminosity and therefore both modes of operation should be possible. A third mode named Hit demands a "1" in any of three bunch crossings, that of the given L1 trigger, the one preceding and the one following. This mode is used for beam tests and diagnostics. The final mode ReadAll places no requirements on the data. All channels are read out. This mode is used during chip testing.

In order to reduce dead time due to queuing losses all the data from an L1 trigger are transferred to an 8 deep de-randomising buffer. The dead time of the system should be less than 1% for a mean occupancy of 1% and a mean L1 rate of 100 kHz. The data from the 6 ABCs corresponding to one side of an SCT module are readout in a daisy chain via a token passing scheme. The bunch crossing clock, the L1 trigger and the other control information are sent to the chips from the DORIC chip.

In order for the system to run reliably for many years at the LHC it must be immune to single point failures. If a single ABC on a module fails, then the module can be re-configured so that bypass lines are used to route data and tokens around the bad chip. If a fibre optic data transmission link fails, then the data can be re-routed via the fibre optic link on the other side of the hybrid. If the clock and control link to a module fails, then the clock and control can be taken from a neighbouring module. Soft errors caused by a loss of a bit in data transmission or clock & control are detected in many cases by consistency checks on the data. This is informational since the system will be reset frequently to clear such errors, rather than corrected on error detection. Errors caused by buffer overflows are detected and lost events are labeled as such in the output data stream. Although an excess data rate can cause loss of data, it should never result in the data being read out for the wrong trigger.

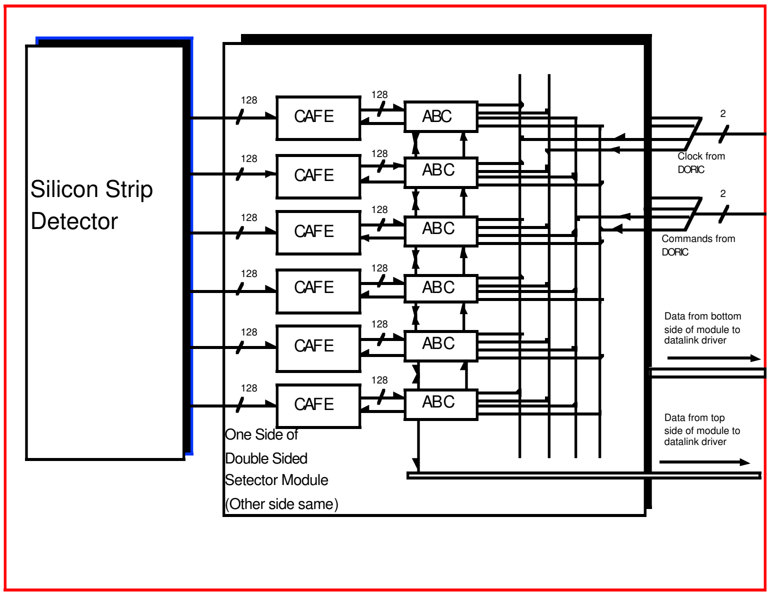

Figure 1.1: Block Diagram of the Binary Readout System

2. RELATED PROJECTS AND DOCUMENTS

1) CAFE-P ATLAS-SCT Specification.

2) ABCD ATLAS-SCT Specification.

3) DORIC4 ATLAS-SCT Specification.

4) VDC ATLAS-SCT Specification.

5) J.R. Gorbold and P. Seller, "DORIC. A Front End Clock and L1 Distribution Chip".

6) Kanex Shankar, Nikhil Kundu et al., "Digital Read-out Chip for Silicon Strip Detectors at SDC".

7) Joel DeWitt, "A 128-Channel Digital Pipeline Chip for Silicon Strip Detector Read-Out".

8) Issy Kipsis, "CAFE: A Complementary Bipolar Analog Front End Integrated Circuit for the ATLAS SCT", 1995.

9) K. Shankar, "DDR2RH Operating Manual".

10) A. Ciocio, T. Collins, "A Binary Readout System for Silicon Strip Detectors at the LHC".

11) F. Anghinolfi, et al., "AROW - A 128 Channel Analogue Pipeline with Wilkinson ADC and Sparsification ASIC"

12) J. Gorbold, "AROW Specification for Input Decoding v.11".

13) Eric Evans, "Requirements for Wilkinson ADC Based Digitisation and Sparsification Circuits for ATLAS".

14) A. Grillo, et al., "Proposed Protocols for Data Transmission and Control Functions for the ATLAS Silicon Micro-strip Detector".

15) A.R. Weidberg, "Dead Time Calculations for SCT Readout Architectures", ATLAS-INDET-124.

3. TECHNICAL ASPECTS

3.1. Requirements

1) The chip will be designed to accept the 128 output signals from the CAFE-P amplifier and comparator chip

2) At the start of each clock cycle the chip must sample the outputs from the CAFE-P and store these values in a pipeline until a decision can be made whether to keep the data.

3) Upon receipt of a Level 1 Trigger signal the corresponding set of values together with it's neighbours are to be copied into another buffer, the readout buffer.

4) The data written into the readout buffer is to be compressed before being transmitted off the chip.

5) Transmission of data from the chip must be compatible with the ATLAS-SCT protocol. Data will be serialized from multiple chips via token passing.

6) The chip will be responsible for supplying the CAFE-P chips with their calibration pulses.

7) The chip is required to provide reporting of some of the errors that occur
a) Attempt to readout data from the chip when no data is available.
b) Readout Buffer Overflow: The readout buffer is full and data from the oldest event/s has been overwritten.
c) Readout Buffer Error: The readout buffer is no longer able to account for the data held in it. (Chip reset required)
d) Configuration error (ChipID sent).

8) The chip will incorporate such features that will enable it to be tested both at the wafer level and in situ. Tests include but are not restricted to:
a) The functionality of input level translators
b) Transmission of programmable pattern through the pipeline and readout circuitry.

9) The chip shall incorporate features that will enable the system to continue operating in the event of a single chip failure by bypassing the single failed chip.

10) The fraction of data which is lost due to the readout buffer on the chip being full must be less than 1%. This assumes that on average only 1% of the silicon strip detectors are hit during any particular bunch crossing.

11) DACs will be included on the chip to enable the thresholds of the comparators, the calibration amplitude and the front-end bias current of the CAFE-P chip to be set .

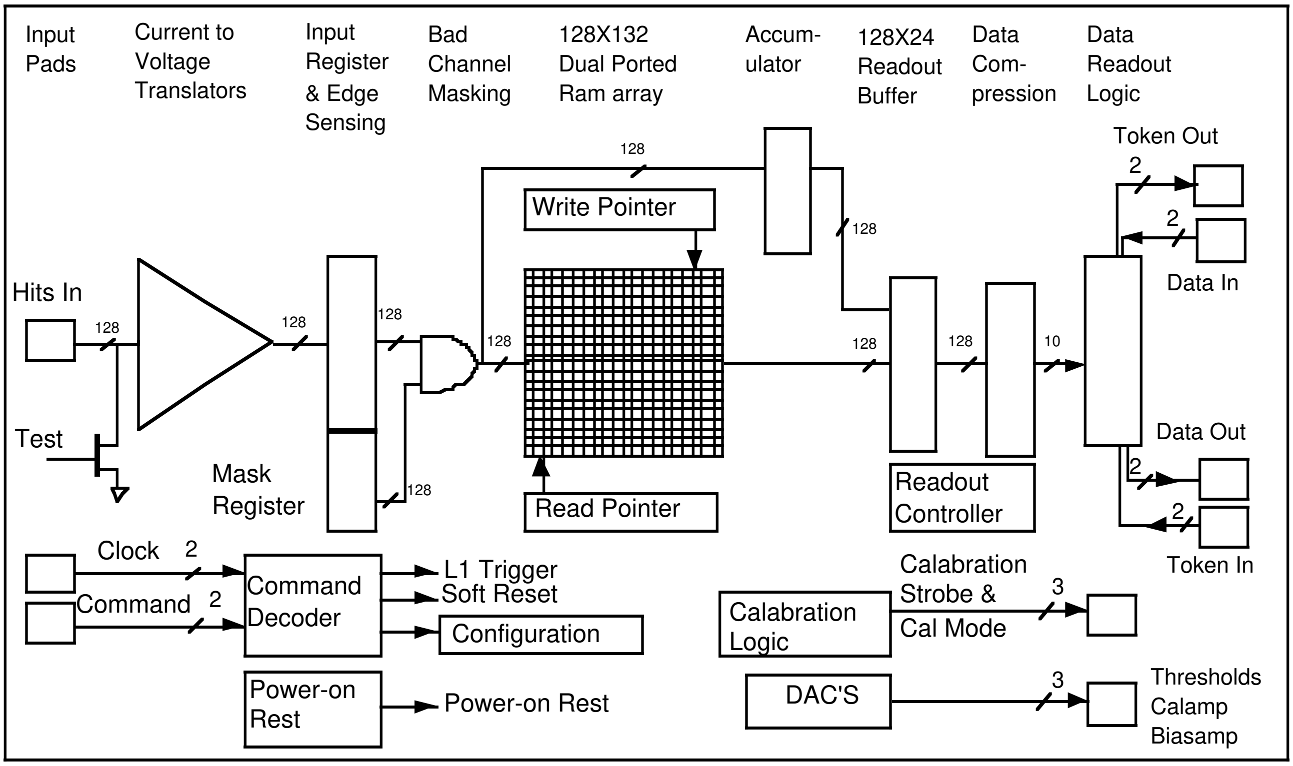

Figure 3.1: Block Diagram of the Binary Readout Chip

3.2. Specification of Deliverables

3.2.1. Input Level Translators

The outputs from the CAFE-P chip, which are fed to the inputs of the Binary Readout Chip are open collector to enable a low voltage swing current mode interface to be formed between the two chips. The input level translators on the ABC must provide a source of current which can be sunk by the outputs of the CAFE-P chip. The line labeled "return" provides a return path for the current sunk by the CAFE-P outputs to be returned to the ABC to minimise any noise coupling between the two chips. The inputs must also be able to detect the amount of current sunk by the individual outputs of the CAFE-P chip and translate it into the logic levels used inside the Binary Readout Chip. The input impedance and circuit response time must ensure transition times < 2 ns on both the rising and falling edges. The effective threshold to distinguish between "hit" and "no-hit" signals from the CAFE-P is set by a high and low reference current provided by the CAFE-P chip with threshold = (inrh+inrl)/2. The design of these inputs is such that the chip is operational with inputs floating or shorted to ground. Built into the block will be the facility to selectively set a quarter of the input channels at a time to the level of a hit channel. This facility is required to enable the inputs to the chip to be tested without the need to probe all input pads. The signals calmode(1:0) are used as a binary address to select one of 4 groups of 32 channels to test. (See Figure 3.2.27b for the physical location of channel addresses.) These signals are derived from two bits in the configuration register named calmode(1:0) (See Table 3.2.9b.) The logic signals "test_inputs" and pulseintputreg are used as a test enable. When either is active, a current equal to inrh is injected into the channels selected by calmode(1:0). The signal test_inputs is activated as a level with the bit named Test_Mode in the configuration register (see Table 3.2.9b). The signal pulseintputreg is a one clock wide pulse generated by a control command. (See Table 3.2.19b.) A special input named CA is provided to modify the effective threshold during chip testing. The actual threshold will be (inrh+inrl)/2+CA. This input will be brought out to a test pad but is intended to be unconnected during normal operation in which case CA will not modify the threshold.

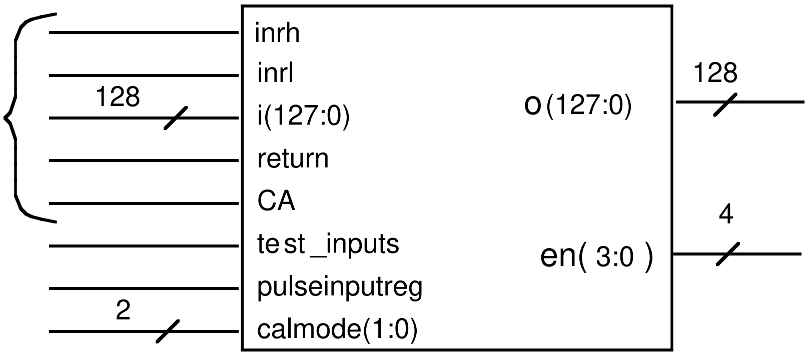

Figure 3.2.1: Input Level Translators Inputs/Outputs

Table 3.2.1a: Input Level Translator I/O Signal Definitions

Signal Name	Active State/Edge	Function
inrh		High ref current (from CAFE-P chip)
inrl		Low ref (from CAFE-P chip)
i(127:0)		Hit Inputs (from CAFE-P chip))
return		Signal Return (to CAFE-P Chip)
CA		Bipolar current to modify threshold during testing
test_inputs	High	Enables testing of inputs
pulseinputreg	High	Pulses test inputs
calmode(1:0)		Selects group of channels to be tested
o(127:0)		Data Outputs (to input reg.)
en(3:0)		Select lines connected to test multiplexor. (See Section 3.2.17.)

Table 3.2.1b: Test Modes for Input Level Translator

test_inputs [Config Reg bit 5]	**pulseinputreg** [command]	**calmode(1)** [Config Reg bit 3]	**calmode(0)** [Config Reg bit 2]	**Channels of Chip Tested**
0	0	X	X	Testing disabled
1	X	0	0	in0, in4 in8,...in124 - Level Applied
1	X	0	1	in1, in5 in9,...in125 - Level Applied
1	X	1	0	in2, in6 in10,...in126 - Level Applied
1	X	1	1	in3, in7 in11,...in127 - Level Applied
0	High Pulse	0	0	in0, in4 in8,...in124 - Single Pulse
0	High Pulse	0	1	in1, in5 in9,...in125 - Single Pulse
0	High Pulse	1	0	in2, in6 in10,...in126 - Single Pulse
0	High Pulse	1	1	in3, in7 in11,...in127 - Single Pulse

N.B. The calmode bits are also used for selecting the calibration mode of the CAFE-P chip. (See Section 3.2.10.)
X = Don't care state.

3.2.2. Input Register and Mask Register

The functions of the input register and mask register will be implemented in a single functional block. The input/output connections to this block are shown in Figure 3.2.2

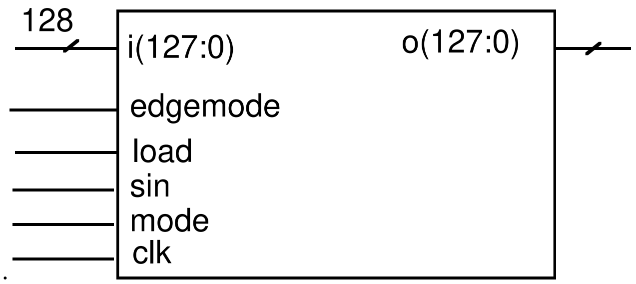

Figure 3.2.2: Input Register Inputs/Outputs

Table 3.2.2a: Input Register I/O Signal Definitions

Signal Name	Active State/Edge	Function
i(127:0)		Hit Inputs (from input translators)
load	Active High	
sin		Configuration Data Inputs
mode	See Table 3.2.2b	
clk	Pos Edge	
o(127:0)		Data Outputs (to pipeline)
edgemode	High	Enables edge detection logic.

3.2.2.1. Input Register

This register latches the incoming data, delivering a well defined pulse width to the pipeline.

3.2.2.2. Edge Detection Circuitry

The function of this block is to detect a low to high transition in the data entering the chip, and for each of such transition found the circuit block outputs a pulse of duration 1 clock cycle irrespective of the length of the incoming pulse. The effect of this block is that only a single "1" is written into the pipeline for every hit detected regardless of the response time of the CAFE-P chip. This circuitry can be turned on or off by setting the appropriate bit in the configuration register.

3.2.2.3. Channel Masking Register

This register serves a dual purpose. Firstly, the Channel Mask register enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate to a level which would create dead-time from false hits. To turn a bad channel off the corresponding bit of the register should be set to a '0' and to turn a channel on the corresponding bit should be set to a '1'. Secondly, it can be used during chip testing to apply a set of test patterns to the pipeline. The operation of the mask register is controlled by a bit in the Configuration Register (See Section 3.2.9.) as shown in the table below. The contents of this register can be changed by sending the appropriate control command to the chip.

Table 3.2.2b: Masking Register Modes of Operation

mode [Config Reg bit 7]	**Mode of Operation**
0	Normal Data Taking (Contents of register used to "Mask Inputs")
1	Test Mode (Contents of mask register are used to supply test values to pipeline)

3.2.3. Pipeline

This consists of a block of dual ported RAM 128-bits wide by 132 locations deep. This must run at 40 MHz, synchronized to the LHC beam crossings. The RAM block is addressed by an address pointer. During data taking the chip is instructed to write into the RAM and increment the address pointer every clock cycle. When the address register reaches a count of 131, it automatically resets to zero on the following clock cycle. When a level one trigger arrives, the hit-pattern from the appropriate time bin is copied into the readout buffer together with the hit pattern from the previous and next clock cycle. There is also an accumulator register which spies on the pipeline.

3.2.3.1. Accumulator Register

This is a 128-bit wide by 1-bit deep register used for accumulating hits in the pipeline. This register marks all channels that have been hit since it was last cleared. If the Accumulator Mode is selected in the configuration register, an L1 trigger results in the transfer of the contents of this accumulator into the readout buffer instead of the appropriate time bins of the pipeline. In order to maintain buffer synchronization with normal (non-accumulator) L1 readout, the accumulator contents are transferred three times for each L1. This accumulator column is cleared by a power-up or soft reset command.

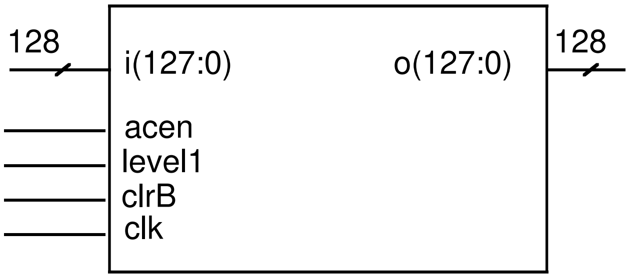

Figure 3.2.3: Pipeline Input/Outputs

Table 3.2.3: Pipeline Input/Output Signal Definitions

Signal Name	**Active State/Edge**	**Function**
i(127:0)		Data Input
acen	High	Enables Accumulator Register
level1	High	Reads Value out of pipeline
clrB	Low	Initialises pipeline pointers and clears accumulator register
clk	Pos edge	Clock input
o(127:0)		Data Output

3.2.4. Readout Buffer

Data corresponding to each L1 trigger will be held in a Readout buffer pending readout. This data buffering is needed to remove the statistical fluctuations in the arrival time of L1 triggers. Data compression and read out will be started only when this buffer is not empty. Three bits of data will be stored in this buffer for each channel per L1 trigger. These bits represents the three bunch crossings centred on the L1 trigger time and are set if the input was above threshold during the corresponding crossings. In the case when the Accumulator Register has been enabled, the contents of this register will be copied into the buffer 3 times resulting in the same amount of data being written into the readout buffer regardless of the operating mode. This buffer will be 128 bits wide by 24 locations deep. This is sufficient to hold the data from eight L1 triggers. This satisfies the ATLAS specification of maintaining $\leq$ 1% data loss at an L1 trigger rate of 100 kHz and a strip occupancy of up to 1% [10].

3.2.4.1. RAM and Pointers

This buffer will be implemented as a "barrel store", i.e. it will be addressed by 2 cyclic pointers, a write pointer and a read pointer. Once a pointer has reached the end of the block of RAM, it will return to the beginning of the block of RAM the next time it is incremented.

The write pointer will be allowed to go past the read pointer and over-write data that has not yet been read out. However, if this happens the Overflow flag will be set to indicate that data has been over-written. The read pointer will not be allowed to pass the write pointer and if the read pointer should catch up with the write pointer the EMPTY flag will be set. This is to prevent attempts to readout the buffer when there is no data in it.

3.2.4.2. Overflow Counter

A counter will be used to track the number of events that have been over-written in the buffer. This counter will be incremented for every time an event is written into the buffer while the buffer is full. The outputs from this counter represents the number of events from which data has been lost. This counter is decremented for every event that is readout of the buffer, until it's value reaches zero. Once its value has reached zero, it is no longer decremented. This is because in this state all the events from which data have been lost will have been cleared and none of the data in the buffer will have been overwritten. Should this counter overflow, the ERROR flag will be set. This will occur after 16 events have been overwritten. This flag will remain set until either a software reset, or power-up resets has been issued to the readout buffer and associated logic.

3.2.4.3. Flag Logic

Three signals DATA_AVAIL, OVERFLOW and ERROR are produced by the readout buffer. DATA_AVAIL indicates when there is data in the buffer to be readout. This signal is used by the Data Compression logic to determine when to start a readout cycle. OVERFLOW indicates when data in the buffer has been overwritten and hence data lost. OVERFLOW occurs when the buffer contains more than 8 events i.e. 24 samples . This signal is sent to the readout logic which results in the readout logic sending an error message to say that data from the current event being readout has been lost. Finally, the ERROR signal is generated when the buffer has overflowed and it has also lost track of the number of events from which data has been lost. This simulation occurs if the data from more than 16 events have been lost. This flag can only be cleared by issuing a reset to the chip.

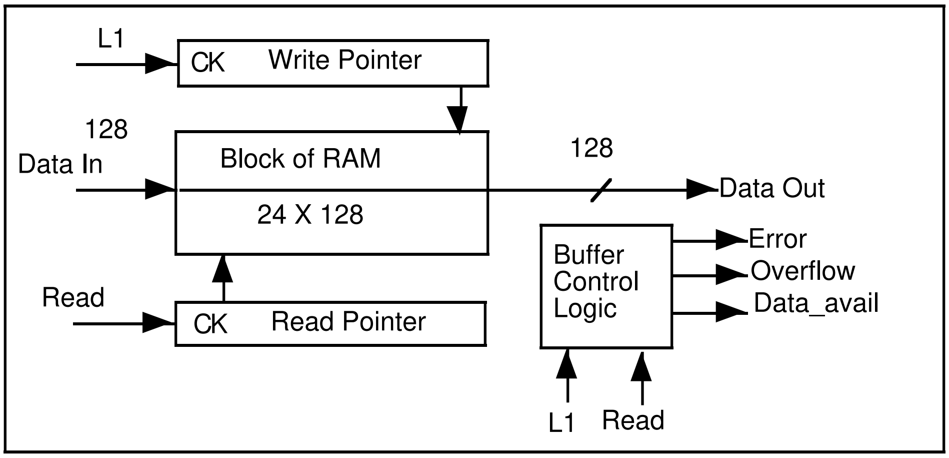

Figure 3.2.4a: Block Diagram of the Readout Buffer

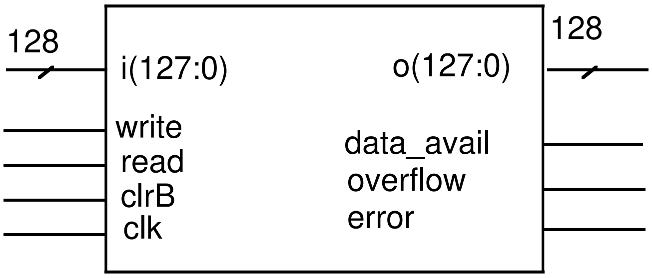

Figure 3.2.4b: Readout Buffer Input/Outputs

Table 3.2.4: Readout Buffer Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
i(127:0)		Data Input
write	High	Write value into readout buffer
read	High	Reads value from readout buffer
clrB	Low	Resets buffers pointers and counter
clk	Pos edge	Clock input
o(127:0)		Data Output
data_avail	High	Data available in buffer
overflow	High	Buffer Overflow
error	High	Buffer Error

3.2.5. Data Compression Logic

It is anticipated that on any event very few channels will contain hits. This fact can be used to reduce the number of bits of data that have to be read out of the chip for each event. The data compression logic works by examining in turn the 3 bits of data that make up the hit pattern for each channel. Each group of 3 bits is compared against one of 4 selectable criteria. If the pattern meets the criteria, then the hit pattern from that channel is sent to the readout circuitry for transmission, if not, no data is sent from that channel and the hit pattern from the next channel is examined. This process is repeated until the hit patterns from all 128 channels have been examined. The following table shows the four selection criteria. Note that the "Edge" criteria (mode=10) is an alternative to using the edgemode of the Input Register (See Section 3.2.2). The ReadAll criteria is intended for test purposes. These mode bits are set in the Configuration Register. (See Section 3.2.9.)

Table 3.2.5a: Data Compression Criteria

mode(1:0) [Config Reg bits 1,0]	**Name of Selection Criteria**	**Hit Pattern** (Oldest data bit 1st)	**Usage**
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	ReadAll	XXX	All channels read out

N.B. X = Don't care state.

This block operates as follows:

As soon as the chip receives an L1 trigger, the three 128-bit words that make up an event are written into the read out buffer. This results in the empty flag on the readout buffer being negated, indicating that there is data to be processed. The data compression logic monitors the state of this flag until it finds that there is data available. Providing that it is not already processing data, it then proceeds to read in the three 128-bit words that make up an event from the readout buffer.

The next thing that happens is that the data compression logic re-arranges the order of the data from being 3 128-bit words into 128 3-bit words. The reason for this is that the data compression algorithm requires all 3 samples of an event to be examined in parallel.

The data compression logic then starts to scan through all the channels in turn until it finds one which has a pattern of hits which matches the data selection criteria. If it finds such a pattern of hits, it asserts the "datavalid" signal and places the pattern of hit bits on the "hit<2:0>" outputs and places the address of the hit channel on the address outputs "ch<6:0>". The logic then waits until the readout logic signals it to proceed by asserting the "next" input. The data compression logic responds to "next" by presenting the address and data for the next hit found if any. If the next hit found is on the next adjacent channel, the "adj" is asserted with the data from the previous channel. If no more hits are found, the "end" signal is asserted.

In certain situations, e.g. in the case of a overflow of the readout buffer, it is not necessary for the data compression logic to process the data from the readout buffer but it is still necessary for it to read the 3 values from the buffer in order to flush them from the readout buffer. There are 3 cases when this happens, these are listed below in order of priority:

1) When the chip is in its SEND_ID mode of operation.
2) When the Readout Buffer error flag has been set.
3) When the Readout Buffer overflow flag has been set.

The following table shows how the datavalid, end and overflowout outputs are used to indicate the status of the data compression logic.

Table 3.2.5b: Data Compression Logic Output States

datavalid	end	overflowout	condition
low	low	low	no events available to be read out i.e. readout buffer empty.
high	low	low	data from hit channel waiting to be read out. (not last channel)
high	high	low	data from last hit channel waiting to be read out.
low	high	low	all hits read out or no hits found
low	low	high	data for event lost due to readout buffer overflow

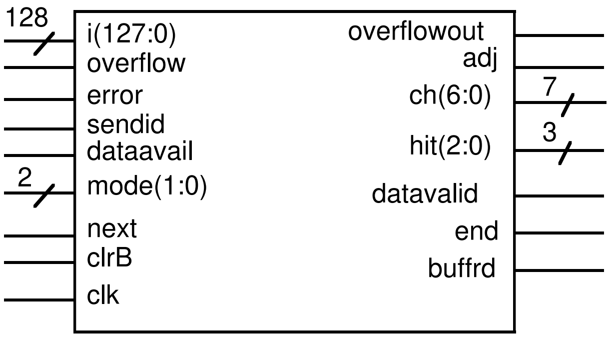

Figure 3.2.5: Data Compression Logic Input/Outputs

Table 3.2.5c: Data Compression Logic Input/Output Signal Definitions

Signal Name	Input/Output	Active State/Edge	Function
i(127:0)	input		Data Input
overflow	input		Overflow output from readout buffer
error	input		Error output from readout buffer
sendid	input		indicates chips mode of operation
dataavail	input	High	Data available to be readout
mode(1:0)	input		Selects data compression mode
next	input	High	Find next hit channel.
clrB	input	Low	Resets logic
clk	input	Pos Edge	Clock Input
overflowout	output	High	Overflow output to readout circuitry
adj	output	High	Next Hit found on adjacent channel
ch(6:0)	output		Channel address of Hits
hit(2:0)	output		Hit Data pattern
datavalid	output	High	Hit Data outputs valid
end	output	High	Last Channel scanned
buffrd	output	High	Reads Value out of Readout Buffer

3.2.6. Readout Circuitry

The readout circuitry will be responsible for capture and release of the token and outputting data from the chip. The readout circuit always waits until the token arrives. On arrival of the token, it checks if any hits have been found by the data compression logic. If so, it then outputs the appropriate header information. It then proceeds to output the address of the hit channel together with the data from that channel. Once the readout circuitry has finished sending the data from one channel, it proceeds to output the data from then next channel. In the situation where one or more neighbouring channels are to be read out, only the address of the first channel is output., but the data from all hit channels is sent. This process continues until the data compression logic indicates that all channels have been examined by asserting "end". Once all the data corresponding to a single event has been read out, a token is sent out to the next chip in the readout chain. This token will be sent out ahead of the last bit of data sent out. If the chip has no data to be readout, circuitry sends out a "No hit data " code and passes the token on to the next chip in the chain.

If the chip is in "send-id" mode or the readout buffer has overflowed or generated an error condition, the readout circuitry sends the appropriate error packet or configuration data packet. In these cases the readout circuitry is still required to signal to the data compression logic that it has processed an event by asserting the "next" signal. This operation is needed so that a correct count of the number of events waiting to be read out can be maintained.

In the case of an error condition occurring, e.g. attempt to readout data and no data available, the appropriate error code will be sent by the readout logic. If the chip is in the "send_id" mode of operation, no data or error codes are output from the chip but instead a special packet of data containing information about the chips current configuration is sent.

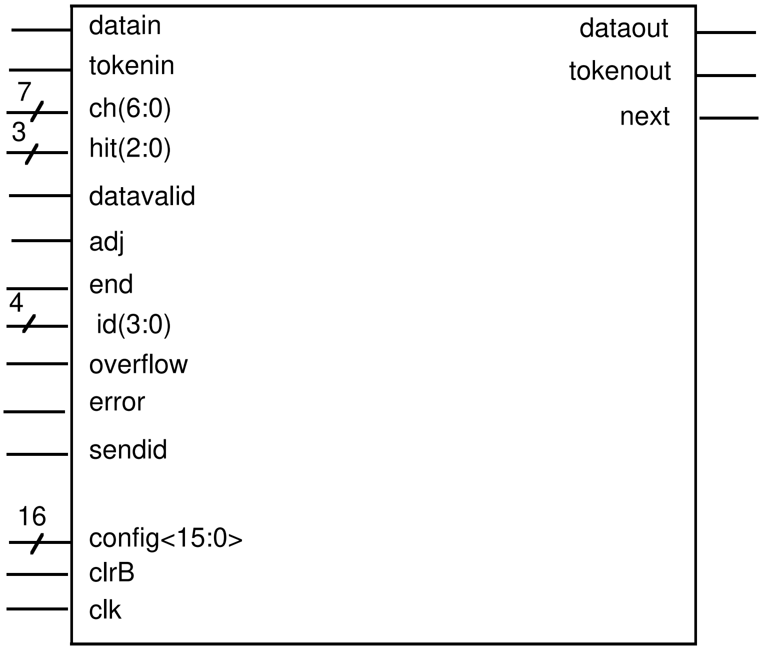

Figure 3.2.6: Connections to Readout Circuitry

Table 3.2.6: Readout Logic Input/Output Signal Definitions

Signal Name	**Input/Output**	**Active State/Edge**	**Function**
datain	input		Data Input
tokenin	input	High	Token Input
ch(6:0)	input		Address of Hit Channel
hit(2:0)	input		Hit data pattern
datavalid	input	High	Data available for sending
adj	input	High	Hit found on adjacent channel
end	input	High	End of data to be sent
id(3:0)	input		LS 4 bits of chip address
overflow	input	High	Readout buffer Overflow
error	input	High	Readout Buffer Error
sendid	input		Chip mode of operation
config<15:0>	input		Data from config-reg
clrB	input	Low	Resets circuit
clk	input	Pos Edge	Clock input
dataout	output		Data output
tokenout	output		Token Output
next	output	High	Scan Next Channel

3.2.7. Readout Controller Block

This block is to control the readout of data from several ABC chips connected together in a token chain. This block is enabled by placing the chip in "Master Mode". This block has to detect when an L1 trigger has been received, issue a token to all the ABC chips connected to it, collect all the data from the chips and tag the data with the bunch crossing number from which it came and the number of Level 1 Trigger. This block then has to transmit this data serially to the datalink driver chip.

3.2.7.1. L1 Counter

This a 4-bit binary counter which is incremented every time the chip receives a level 1 trigger. The counter is zeroed by either a hardware reset or a software reset.

3.2.7.2. Bunch Crossing Counter

This is an 8-bit binary counter which is incremented on every clock cycle. This counter is zeroed by either a hardware reset, a software reset., or a special BC Reset Command

3.2.7.3. Event FIFO

This is a 24 location deep, 12-bit wide FIFO. Each time the chip receives an L1 trigger, the output of the L1-Counter and the Bunch crossing counter are loaded into the FIFO prior to the counters being incremented. These values are read from the FIFO every time an Event is readout and are used to tag the data with 12-bits of information about which trigger number and bunch crossing number the data came from.

3.2.7.4. Token Generation Logic

The purpose of the token generation logic is to detect when the chip has received an L1 trigger and to generate a token to initiate the read out of data from that L1 trigger. This logic waits until the Event FIFO becomes not empty and it then issues a token. It then monitors the data passing through it from all the chips in the chain looking for a "Trailer" bit pattern. It waits until this trailer is detected before checking to see if the Event FIFO is empty. If the Event FIFO is still not empty it repeats the cycle.

3.2.7.5. Data Formatting Logic

The purpose of this logic is to attach the header information to the packets of data output from the chip on the Serial Data Output.

3.2.7.6. Serial Data Output Driver

This circuit block generates the output signals to the data links which send data to the DAQ system.

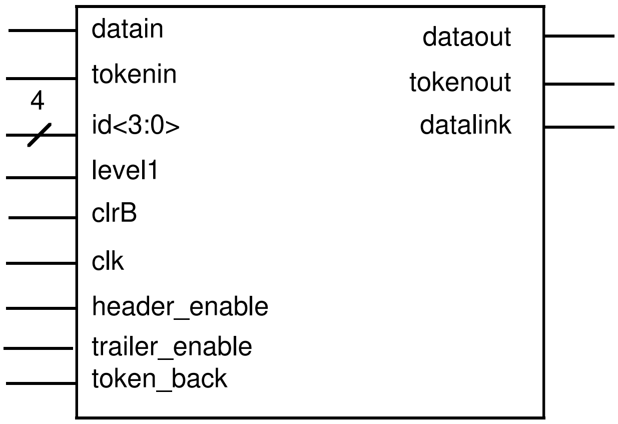

Figure 3.2.7: Connections to Readout Controller Circuitry

Table 3.2.7: Readout Controller Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
datain		Serial Data Input
tokenin	High	Token Input
id<5:0>		Address of chip
level1	High	Level 1 Trigger
clrB	Low	Resets block
clk	Pos Edge	Clock input
dataout		Serial data output
tokenout	High	Token Output
header_enable	High	Enables Generation of Packet Header
trailer_enable	High	Enables Generation of Packet Trailer
token_back	High	Input for Token output from ROL
datalink		Serial data out to link driver

3.2.8. Command Decoding

The command and control information all comes into the chip on the command input pads. There are two main classes of information which arrive here, Level 1 Trigger Commands and Control Commands. These are distinguished by a 3-bit code. Furthermore two types of Control Commands are possible, Fast Control Commands and Slow Control Commands. Depending on which class arrives, further information may follow. This further information will also need decoding, formatting and sending to the appropriate functional blocks of the chip. More detailed information is contained in 3.2.18 and the actual data fields of the commands are listed in Tables 3.2.19a and 3.2.19b. The two classes of Commands and two types of Control Commands are:

Level 1 Trigger Command

If the 3-bit code indicating this command is received, the control logic writes 3 samples from the pipeline or the accumulator register, into the Readout Buffer.

Control Commands

If the 3-bit code indicating a Control Command is received, the second field of 4 bits is decoded to determine if it is a Fast Control Command or a Slow Control Command. If a Fast Control Command is decoded, the appropriate command is executed. No address or data fields are included in these commands..

Slow Control Command

If the second field of the command is decoded to be a Slow Control Command, the third, forth, fifth and possibly sixth field is decoded to determine the full action required. These Slow Control Commands are of variable length and the contents of the third field determines the total number of bits to be processed.

The command decoder block is required to decode the command and send the relevant instruction and data to other parts of the chip. The input/output connections to this block are shown in Figure 3.2.8.

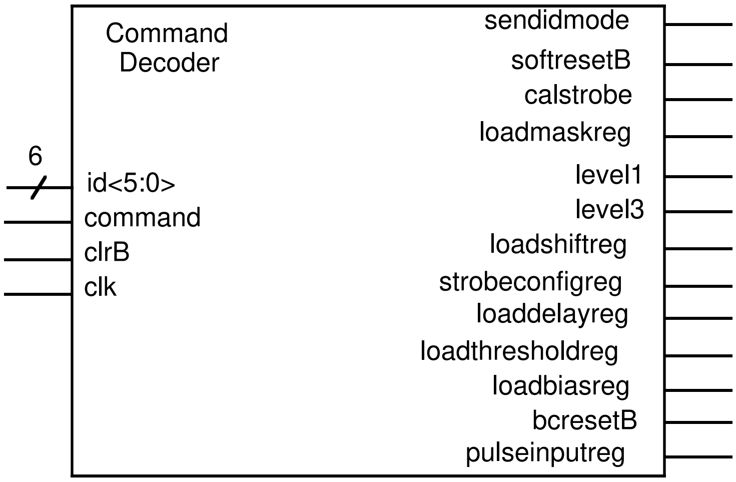

Figure 3.2.8: Command Decoder Inputs/Outputs

Table 3.2.8: Command Decoder Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
id<5:0>		Chip ID
command		Command Data Input
clrB	Low	Reset Block
clk	Pos Edge	Clock Input
sendidmode		Sets chips mode of operation
softresetB	Low	Software controlled reset
calstrobe	High	Send Calibration pulse to CAFE-P
loadmaskreg	High	Load Mask Register
level1	High	Level_1 Trigger received
level3	High	Same as level1 but High for 3 cycles
loadshiftreg	High	Loads Configuration reg.
strobeconfigreg	High	Strobes data into configuration reg
loaddelayreg	High	Load Strobe Delay Register
loadthresholdreg	High	Load Threshold/Calibration DAC Register
loadbiasreg	High	Load Bias DAC Register
bcresetB	Low	Bunch crossing reset

3.2.9. Configuration Register

This circuit block contains a shift register to accept serial data input as part of various commands, a serial-to-parallel converter and a 16-bit register to hold data for the configuration register. Data intended for other registers is presented at the parallel output shiftreg. The contents of the 16-bit latched configuration register is presented at the parallel output dataout. Shiftreg presents the data just shifted in upon a high load signal. The configuration register is latched on the falling edge of the load signal. The input/output connections to this block are shown in Figure 3.2.9. Data is shifted into this register MS bit first. The configuration register holds information about the chip's current configuration. The following Table 3.2.9b defines the usage of the bits in this register. The power up value of this register will be zero as cleared by the clrB signal. The contents of this register are not effected by a software reset command.

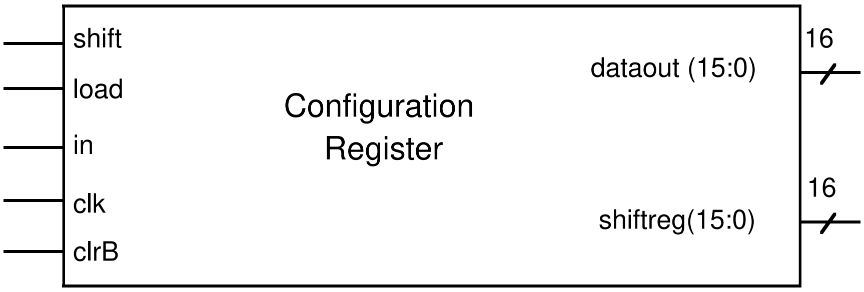

Figure 3.2.9: Configuration Register Inputs/Outputs

Table 3.2.9a: Configuration Register Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
shift	High	Enables data to be shifted into reg
load	High; Latch at Negative edge	Transfers data to register outputs
in		Serial Data input
clk	Positive Edge	Clock input
clrB	Low	Resets register to default values
dataout(15:0)		Configuration Data Outputs (See Table 3.2.9b.)
shiftreg(15:0)		Data to be latched by Delay or DAC Registers

Table 3.2.9b: Configuration Register Contents

Bit	Name	Function
0-1	Readout Mode	Selects the data compression Criteria. (See Table 3.2.5a.)
2-3	Cal_Mode(1:0)	Selects the Calibration code for the CAFE-P chip (See Table 3.2.10.) and also determines which channels of the Input Level Translators are tested when Test Mode is enabled. (See Table 3.2.1b.)
4	Dataout Delay	Enable extra 4 clock delay before initiating data output stream to data link driver
5	Test_Mode	When this bit is set, test values are applied continuously at the Input Level Translators to the channels defined by bits 2 & 3 of this register. Use with Mask (bit 7) = 0.
6	Edge_Detect	When this bit is Set the edge detection circuitry in the input stage is enabled.
7	Mask	When this bit is set the input register is disabled and the contents of the mask register are routed into the L1 pipeline.
8	Accumulate	When this bit is set the Accumulate function is enabled. (See Section 3.2.3.1)
9	Input_Bypass	This bit determines which set of token/data inputs are active. (See Section 3.2.22)
10	Output Bypass	This bit determines which set of token/data outputs are active. (See Section 3.2.22)
11	Master *	When clear the chip acts as a Master providing the masterB input pad has be asserted
12	End	When set this bit configures the chip as the end of a readout chain.
13	Feed_Through	When clear the chip outputs a clock signal at one-half the clk frequency through the datalink output but only if the chip has been configured as a Master. (See above.)
14	Not used	
15	Not used	

* This bit is "ored" with the value on the "masterB" input. If the result is "0", the chip is placed into master mode. Otherwise, it is placed into slave mode.

3.2.10. Calibration Logic

The calibration logic produces a calibration strobe signal for the CAFE-P chip. This strobe is produced in response to a control command. (See Table 3.2.19b.) A two-bit calibration code is also sent to the CAFE-P chip which selects one of the four possible patterns in the CAFE-P chip. The two-bit calibration code outputs are single-ended CMOS levels. The calibration Strobe is a differential current output. The calibration Strobe signal must be sent to the CAFE-P chip a fixed number of clock pulses after receipt of the control command. The delay from the rising edge of the clock signal to the rising edge of the strobe signal is determined by the value loaded into the Strobe Delay Register. This delay can be adjusted in 64 equal steps over a range of values exceeding the length of one clock period.

Table 3.2.10: Intended Effect of Calibration Codes Sent to CAFE-P

Cal_Mode(1) [Config Reg bit 3]	**Cal_Mode(0)** [Config Reg bit 2]	**Channels of CAFE-P Chip Pulsed**
X	X	Calibration disabled
0	0	in0, in4 in8,...in124
0	1	in1, in5 in9,...in125
1	0	in2, in6 in10,...in126
1	1	in3, in7 in11,...in127

3.2.11. Strobe Delay Register

The Strobe Delay Register is an 8 bit register of which only the least significant 6 bits are used. The value stored in this register determines the relative delay between the rising edge of the Calibration Strobe output to the CAFE-P chip and the rising edge of the clock input. This delay can be set in 64 steps, of approximately 1.1 ns ±0.5 ns each. This enables the delay of the Calibration Strobe to be swept though a complete clock cycle at 40 MHz. Data is shifted into this register with the MS bit first.

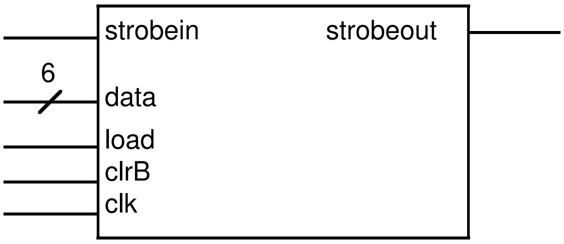

Figure 3.2.11: Strobe Delay Register Inputs/Outputs

Table 3.2.11: Strobe Delay Register Input/Output Signal Definitions

Signal Name	**Active State/Edge**	**Function**
strobein		Strobe input
data		Data input to register
load	High; Latch on falling edge	Loads delay value into register
clrB	Low	Resets register
clk	Pos Edge	Clock input
strobeout		Delayed version of STROBE_IN

The value of delay is determined according to the following formula:

delay = min_delay + (register_value x step_value)

Where :

min_delay: the delay produced when the register is set to zero .
register_value: the value written into the delay register (least significant 6 bits only)
step_value: the increase in delay produced by incrementing the contents of the delay register (typically 1.13 ns.)

3.2.12. DAC Register

The DAC registers are two 16-bit registers which hold 2 8-bit values and one 4-bit value. A threshold value is held in the MS byte of the first register and a calibration amplitude value is held in the LS byte of this register. The outputs of this register are used to control 2 separate 8-bit DACs. The second register contains a 4-bit value in bit positions 11-8 used to control a separate 4-bit DAC for the front-end bias current of the CAFE-P. The outputs from these DACs supply three independent DC current levels to the CAFE-P chip. The MS bit is shifted into these registers first. See Table 3.2.19b for the load sequence of the DAC registers. All DAC registers are cleared by the Power-up Reset signal.

Figure 3.2.12: DAC Register Inputs/Outputs

Table 3.2.12: DAC Register Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
loadthresholdreg	High; Latch at falling edge	Load values into threshold/cal register
loadbiasreg	High; Latch at falling edge	Load value into bias register
data		Data input to register
clrB	Low	Resets register
clk	Pos Edge	clock input to register
threshold		Threshold Output for 1st DAC
cal amp		Calibration Amplitude Output for 2nd DAC
biasamp		Bias Amplitude Output for 3rd DAC

3.2.13. DACs

All three DACs supply control currents to the CAFE-P. Two 8-bit DACs are used to set a threshold (ith output) and calibration value (cali output) in the CAFE-P chip. The single 4-bit DAC is used to set the bias current (ivi1 output) for the front-end stage of the CAFE-P. These DACs will receive an input reference current "iref" (pad name IDAR) from the CAFE-P chip. This reference current will be scaled at the output of the DAC by a value between 0 and full scale of the DAC (255 or 15) depending upon the setting of the DAC register. The exact scaling is given in Table 3.2.25j.

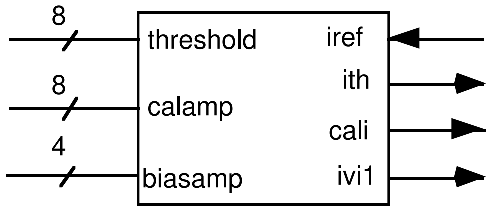

Figure 3.2.13: I/O connections to DACs

3.2.14. Clock and Command Inputs

Two sets of clock and command inputs will be provided in order to make the system in which the ABCs will be used fault tolerant and to provide an additional method of setting up the timing of the system. Each chip will be supplied with two independent sources of clock and commands. In the event of the fall out of one of these sources, the alternative source can be used. An external input to the chip "select" pad will be used to determine which pair of inputs will be used by the chip. This "select" pad has an internal pull-down which defines its state as low if left unconnected.

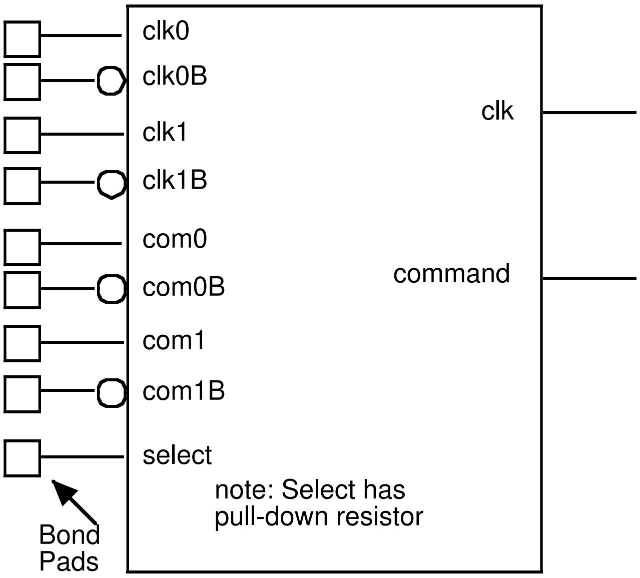

Figure 3.2.14: Clock & Command Data Inputs

Table 3.2.14a: Clock Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
clk0		default Clock Input
clk0B		Complement of above
clk1		alternate Clock Input
clk1B		Complement of above
com0		default Command Input
com0B		Complement of above
com1		alternate Command Input
com1B		Complement of above
select	Low for default clk/command; High for alternate	Selects which pair of inputs to use
clk		Clock output
command		Command Data Output

Table 3.2.14b: Clock Input Modes of Operation

select	clk	command
Low	clk0	com0
High	clk1	com1

N.B. internal pull-down defines state as low if left unconnected

3.2.15. Chip ID.

To enable a chip to be individually addressed five inputs (ID(4:0) will be used to implement a geographical addressing scheme. This is because there will be a total of 12 chips on each module (6 per side), and under certain conditions it may be necessary to address all the chips on 2 modules using the same control line. These inputs will be wire bonded to a unique set of logic levels on each chip mounted on the detector module. This set of logic levels will form a geographical address which will enable individual chips on the module to be addressed. The chips will be bonded according to the following scheme. For historical reasons the command decoder on the chip has been designed to decode a 6-bit geographical address, however the MS bit of the chips geographical address is always set to a '1' . The sixth bit ID(5) is not brought out of the chip but instead is set internally to a logic '1' level. ID(3:0) have internal pull-up resistors to force these inputs to a logic '1' if left unconnected. ID(4) has an internal pull-down to force it to a logic '0' if unconnected.

Table 3.2.15a: Geographical Addresses (ID5-0)

id(5:0)	Type of Chip Selected	Odd/Even Module
10aaaa	ABC	Even
11aaaa	ABC	Odd
111111	All ABC chips	Both

N.B. aaaa is the 4-bit address of the ABC chip on the hybrid. See Table 3.2.15b

Table 3.2.15b: ABC Geographical Addresses (ID3-0)

Chip Position on Hybrid *	ID(3)	ID(2)	ID(1)	ID(0)
M0 (Master)	LOW	LOW	LOW	LOW
S1 (Slave)	LOW	LOW	LOW	HIGH
S2	LOW	LOW	HIGH	LOW
S3	LOW	LOW	HIGH	HIGH
S4	LOW	HIGH	LOW	LOW
E5 (End Slave)	LOW	HIGH	LOW	HIGH
M8	HIGH	LOW	LOW	LOW
S9	HIGH	LOW	LOW	HIGH
S10	HIGH	LOW	HIGH	LOW
S11	HIGH	LOW	HIGH	HIGH
S12	HIGH	HIGH	LOW	LOW
E13	HIGH	HIGH	LOW	HIGH

* Refer to diagram of chip interconnections in Figure 3.2.22b

3.2.16. Token Input/Output Circuit

In order to provide some measure of fault tolerance in the system, a token and data bypass circuit will be built into each chip. The purpose of this circuit is to enable a chip to source or send it's token and data to another chip other then it's direct neighbours. Each chip will have 2 token and data inputs. It will also have two token or data outputs. Pairs of inputs and pairs of outputs will be connected to different chips enabling it to send or receive data from one of two chips. In this way, should one of the chip's neighbours fail, an alternative chip can take its place. Commands are used to direct each chip to use its normal or bypass inputs and outputs.

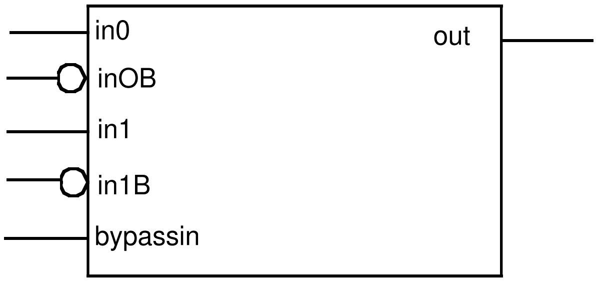

Figure 3.2.16a: Token and Data Inputs circuit

Table 3.2.16a: Token and Data Input Signal Definitions

Signal Name	Active State/Edge	Function
in0		1st Data/Token Input
in0B		Complement of above
in1		2nd Data/Token Input
in1B		Complement of above
bypassin		When High in1 is selected else in0
out		Token /Data Output

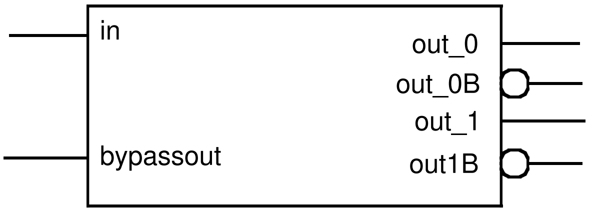

Figure 3.2.16b: Token and Data Outputs circuit

Table 3.2.16b: Token and Data Output Signal Definitions

Signal Name	Active State/Edge	Function
in		Token/Data in
bypassout		When High out1 is enabled else out0
out0		1st Data/Token Output
out0B		Complement of above
out1		2nd Data/Token Output
outB		Complement of above

3.2.17. Test Circuitry

Several features have been added to aid in the testing of the chip. First, the Input Level Translators have a test feature included which allows test levels and test pulses to be injected into the front-end of the chip. This allows the full data path to be exercised with the exception of the input pads and metal trace leading to the Input Level Translator block. Since the possibility for defects to kill a channel in this small area is low, it should be possible to perform adequate wafer screening without probing the dense input pad area. Furthermore, the CA input is provided to alter the effective threshold level of the Input Level Translators to test the discrimination margin. (See Section 3.2.1.) It will be required to probe all of the pads in the upper end of the input section which provide control interface to the CAFE-P (e.g. ITH, CALI, CALSP, CALSN). To ease the difficulty of probing this dense region of pads, four of the pads (CALD1, INRH, INRL, CALD0) are duplicated along the upper side of the chip. These duplicate pads are intended for wafer probing only.

To aid with chip debug, several test points have been provided. Some of these points are provided as directly probable pads. Other internal logic signals are fed to a 128:1 multiplexor. The multiplexor is controlled by a 7-bit counter. Four pads accompany the testmultiplexor. The first clears the counter; the second increments the counter with each pulse; the third presents a high signal when the counter is at 0; the fourth presents the test point selected by the counter

Table 3.2.17a: Directly Probable Test Pads

Test Pad	Signal Description
ITH	Same as external pad. See Table 3.2.24b.
IDAR	Same as external pad See Table 3.2.24a
CALSP	Same as external pad See Table 3.2.24b
CALSN	Same as external pad See Table 3.2.24b
ILT_out(125,122,65,62,5,2)	Unbuffered output from Input Level Translators for 6 channels
tokenin	
datout	
clk<1>	Internal clk after clk0/clk1 multiplexor
com<1>	Internal command signal after com0/com1 multiplexor
datalink_test	Buffered signal to LVDS output after clk_div2 multiplexor
toknnext	
datain	
poweron_rst	
token_startB	
data_validB	

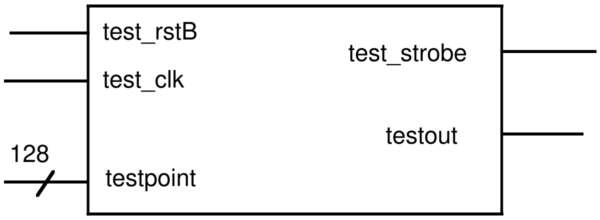

Figure 3.2.17: Test Multiplexor Circuit

Table 3.2.17b: Test Multiplexor Signal Definitions

Signal Name	Active State/Edge	Function
test_rstB	Low (15 kΩ pull-down resistor)	Clear Multiplexor Counter
test_clk	Positive Edge	Increment Multiplexor Counter
testpoint		128 test point inputs
test_strobe	High	High when MUX Counter = 0
test_out		Selected testpoint output to test pad

N.B. All these signal except the 128 testpoint inputs appear as test pads on the chip.
The 15kΩ pull-down on pad test_rstB assures that the MUX defaults to testpoint(0) and does not chatter if unused.

The following table lists the test points presented for each value of the 7-bit MUX counter. Most signal names are defined in the sections of this specification dealing with the related circuit block.

Table 3.2.17c: Test Multiplexor Signal Definitions

Count Value	Testpoint		Count Value	Testpoint
	Input Level Translators			TOP Left Circuit Block
0-3	EN<3:0>		96	CStrobe
	Pipeline			Command Decoder
4	serial_out		97	L1
5	d_dataavail		98	L3
6	d-error		99	bcresetB
7	d_overflow0		100	calstrobe
8-11	PIPE_test<3:0>		101	fcUnusedCode
	Data Compression Logic		102	invalidFL
12	token_startB		103	loadshiftreg
13	buffrd		104	loaddelayreg
14	datavalid		105	loadmaskreg
15-21	ch<6:0>		106	loadthresholdreg
22	adj		107	pulseinputreg
23-25	hit<2:0>		108	scInvalidFL
26	end		109	scUnusedCode
27	overflowout		110	sendidmode
28-38	DCLsm1<11:1>		111	softresetB
39-45	DCLsm2<7:1>		112	strobeconfigregB
46-49	DCLloop<3:0>		113	tcUnusedCode
50	data_validB_int		114	loadbiasreg
51-57	ch_int<6:0>			RIGHT SIDE Circuit Block
58	adjB_int		115	clk0_test
59-61	hit_int<2:0>		116	clk1_test
62	end_int		117	com0_test
	Readout Logic		118	com1_test
63	adj_int		119	tokenin
64-73	ROLsm<10:1>		120	datain
74	databack		121	tokenout0_test
75	tokenback		122	tokenout1_test
	Readout Control		123	dataout0_test
76	dataout		124	dataout1_test
77	ledout		125	datalink_test
78	tokennext		126	clrB
79	tokenout		127	intrstB
80	FifoRead			
81	TrailDtect			
82	TrlDtectM1			
83	BCRstB			
84	PSCLoad			
85	PSCIn			
86	FifoEmpty			
87-95	ROCsm<8:0>			

3.2.18. Readout Protocols

Output data from the ABC can be grouped into one of five classes:

3.2.18.1. Module Data

This type of data packet is only output from chips which have been configured as Masters. The packet consists of four elements. A 5-bit Preamble and a 14-bit Header containing information about the data are both generated by the Master ABC chip. A string of data blocks sent from all ABC chips are daisy-chained together through the Master ABC chip. The Trailer bit sequence (a "1" followed by 15 "0") is appended to the data stream by the chip configured as END.

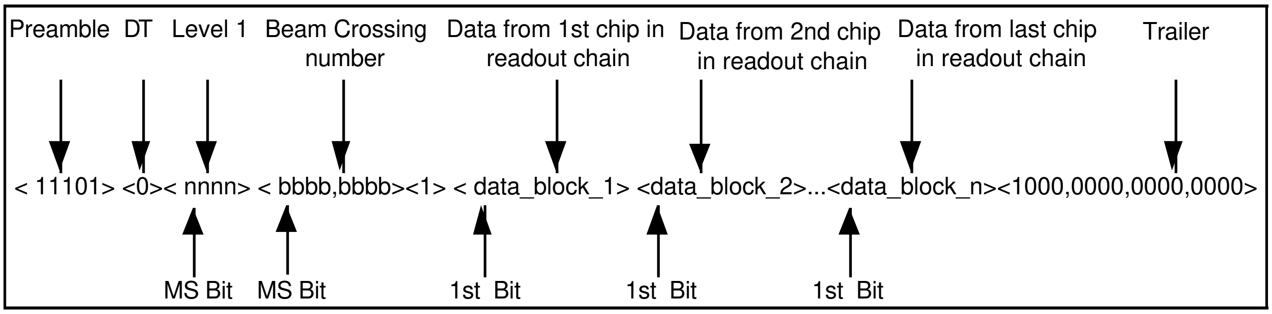

Figure 3.2.18a: Module Data Format

DT(Data Type) (Part of Header)

The value of this bit determines the type of data which follows. This can either be Level 1 Trigger Data (DT=0) or Information Data (DT=1). In the case of the ABC chip only Level 1 trigger Data is Sent and hence this field is always set to '0'.

Level 1 (Part of Header)

Current count of Level1 Trigger modulo 16 since the last system reset. This field can be used for event building by the DAQ and also to monitor for lost data. Note that the value of Level 1 for the first trigger read out after a Soft Reset command is 1.

Bunch Crossing Number (Part of Header)

Current count of Bunch Crossing modulo 256 since the last system reset or BC Reset command. It is intended to monitor for clock pulses lost by the on-detector electronics and can be used to tag one bunch crossing out of the complete ring of the LHC. Note that the value of the Bunch Crossing Number for an event read out from an L1 Trigger command occurring immediately (no clock gaps) after a BC Reset command or Soft Reset command is 3.

Data Block

This is the data packet sent from each chip including the master chip. This data block can be any of the four following types, Physics Data, No-Hit Data, Error Data or Configuration Data.

3.2.18.2. Physics Data

This type of data packet is used to send the compressed hit data from the detector. The format of this data is a series of one or more data packets.

<data_packet_1><data_packet_2> - - - <data_packet_n><data_packet_n+1>

There are two types of data_packet, isolated hit packet and adjacent hit packet. A physics data packet can consist of any combination of these two types of packets. Note that if Data Compression has been disabled by selecting the ReadAll option (See Section 3.2.5), the whole chip will be readout as one cluster of 128 adjacent hits.

Isolated Hit Data-Packet.

This type of packet is used to send the hit information from a hit channel on a chip when non of it's neighbouring channels have been hit.

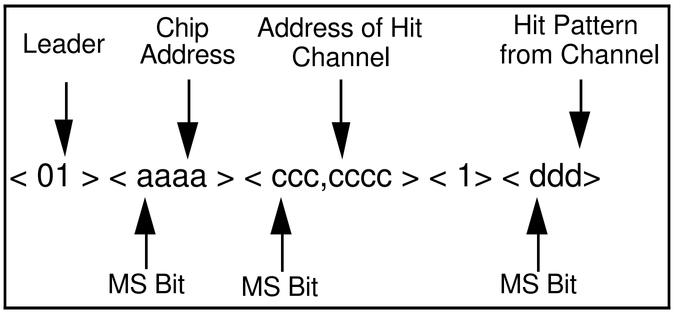

Figure 3.2.18b: Isolated Hit Data Format

Adjacent Hit Data-Packet

This type of packet is used to send data from a group of 2 or more adjacent channels which have been hit. Only the channel address of the 1st channel in the group is sent. It should be noted that this will also be the lowest numbered channel in the group. The chip address and channel address's of the other channels can be derived from that of the 1st and hence are not sent.

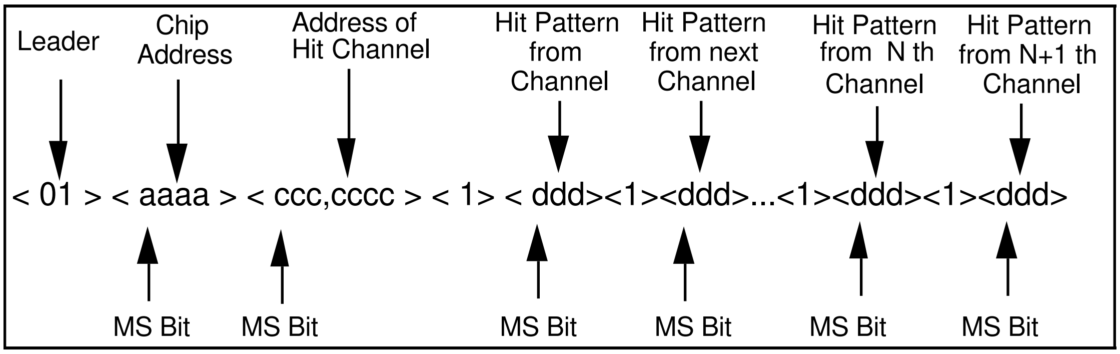

Figure 3.2.18c: Adjacent Hit Data Format

where

aaaa	LS 4 bits of the chips geographical address
ccc,cccc	7-bit address of the channel on which the hit or 1st channel in a groups of hits was found (See Figure 3.2.27a for the physical location of channel addresses.)
ddd	Is the 3 bit hit pattern read out from the hit channel. (Previous, Current, Next)

Example

The following physics data packet would be send out from a chip with a geographical address of $2D_H$ and hits on channels 3, 5 and 6.

<01><1101><000,0011><1><ddd_3><01><1101><000,0101><1><ddd_5><1><ddd_6>

where ddd_3 = data from channel 3, ddd_5 = data from channel 5, ddd_6 = data from channel 6

Note that if Accumulator Mode is selected in the Configuration Register (See Section 3.2.3.1), a hit channel will usually read as '111' and a non-hit channel as '000'. This, however, is not always true. If a channel is hit during the three clocks needed to transfer data into the Readout Buffer, a pattern of '011' or '001' can result.

3.2.18.3. No-Hit Data

If a chip has received the event currently being read out but has not found any hit channels, it outputs a Null Data Packet.

< 001>

Figure 3.2.18d: Null Data Packet

3.2.18.4. Configuration Data

Configuration data is sent by the chip in response to an L1 trigger when the chip is in its Send_ID mode of operation, i.e. the chip is not sending data. A packet of data is sent from the chip which contains the chips address and the contents of the chips configuration register.

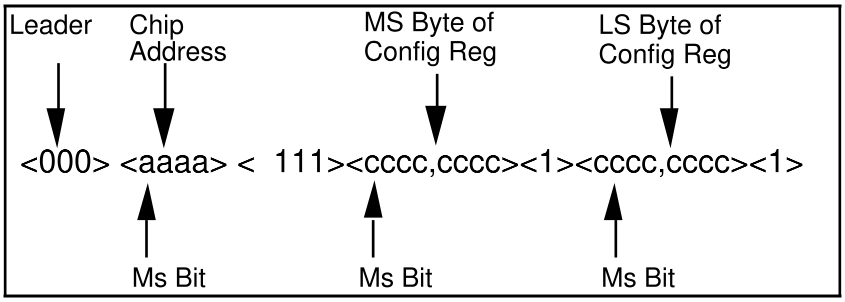

Figure 3.2.18e: Configuration Data Packet

3.2.18.5. Error Data

Error data is only sent if the chip detects an error, e.g. Buffer overflow. In this cases a data packet of the following format is sent:

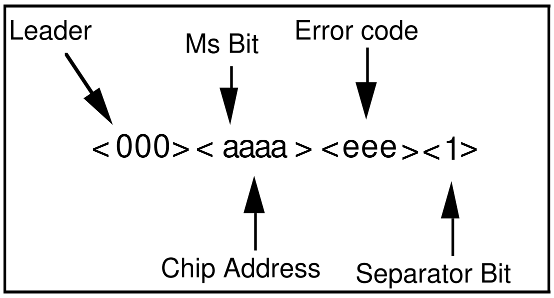

Figure 3.2.18f: Error Data Format

Error Codes:

3 codes have been defined :

eee = 001 No Data Available (The chip has not received an L1 command, only possible in Slave Mode.)
eee = 010 Buffer Overflow
eee = 100 Buffer Error (Soft Reset needed)
N.B. Error messages are only sent if the chip is in Data_Taking Mode. (See Section 3.2.19.)

3.2.19. Control Protocol

There are two main classes of commands, Level 1 Trigger Commands and Control Commands, and there are two types of Control Commands, Fast Control Commands and Slow Control Commands. It is not expected that the Slow Control Commands will be issued during data taking operation.

Table 3.2.19a: Commands

Type	Field 1	Field 2	Field 3	Description
Level 1	110	---	---	Level one Trigger
Fast	101	0100 or 0010		Soft Reset BC Reset
Slow	101	0111	Command	Slow Control Command. See Table 3.2.19b.

3.2.19.1. Level 1 trigger Command:

This is the most frequently issued packet and hence the smallest. All ABC chips that receive this packet act on it. There is no addressing. If this command is received 3 samples are readout out of the pipeline and written into the readout buffer.

3.2.19.2. Fast Control Command:

This type of command is sent when a command has to be issued to the chip more quickly than can be achieved by sending a slow command to the chip. In the case of the ABC chip, only two commands of this type have been defined, i.e. the Soft Reset and BC Reset commands. It is expected that these commands will be sent to the chip at regular intervals during periods of time when no Level 1 Triggers will be sent to the chip. The purpose of these commands is to perform a limited reset of the chip. (See Section 3.2.19 for details.)

3.2.19.3. Control commands

These are long packets that enable the operation of the chip to be controlled. While they are being sent, it is not possible to send a first level trigger. Only the addressed ABCs will act on the packet, unless the address sent equals '111111', in which case all chips will act on the packet. All chips that receive the packet must decode it, even if they do not act on it. This is to avoid un-addressed ABCs erroneously decoding parts of the data field as the start of packets. To ensure that the chip does not respond to erroneous commands the chip will be placed out of data taking mode for any command it receives which effects the configuration of the chip, i.e. all commands in which the 1st bit of field 5 is '0'. Hence it will be necessary to issue a command to the chip to enable data taking after issuing a command to change its configuration. When the chip is not in data taking mode, it will send its ID instead of real data in response to an L1 Trigger. This is the power-on default state.

3.2.19.4. Erroneous Commands

If the chip should receive a command that it does not recognise it is dealt with in the following manners depending upon which field is in error.

Error in Field 1: If field 1 is not equal to 110 or 101, the command decoder ignores the command and immediately starts to accept new commands.

Error in Field 2: If field 2 is not equal to one of the three valid values, the command decoder ignores the command. The command is considered to be an unrecognized fast-command. The rest of the command is ignored and the command decoder waits the number of bits of a valid fast-command before it starts accepting new commands.

Error in Field 3: Field 3 contains the length of the slow-command. Only 3 lengths are allowed: 28 (0001_1100), 140 (1000_1100) and 12 (0000_1100). The command is considered to be an unrecognized slow-command if Field 3 does not equal one of these 3 allowed values. In such a case, the command decoder waits the number of bits which is specified by field 3 before it starts accepting new commands.

Error in Field 4: When the chip address in the command does not match the chip address established by bonding pads id(4:0), when the first bit of field 4 is not equal to 1 or when the address is not the "all chips" address (111111), the rest of the command is ignored. In such a case, the command decoder waits the number of bits which is specified by field 3 before it starts accepting new commands.

Error in Field 5: When the command is not recognized or when the command is recognized but the length specified in field 3 does not match the correct length for the recognized command, the rest of the command is ignored. In such a case, the command decoder waits the number of bits which is specified by field 3 before it starts accepting new commands.

Table 3.2.19b: Control Commands

Field 3	Field 4	Field 5	Field 6	Description
0001,1100	aaaaaa	000 000	dddd,dddd,dddd,dddd	Write to Configuration Register
1000,1100	aaaaaa	001 000	d---,----,----,---d	Write to Mask Register (MSB=Ch127)
0001,1100	aaaaaa	010 000	dddd,dddd,dddd,dddd	Write to Strobe Delay Register
0001,1100	aaaaaa	011 000	dddd,dddd,dddd,dddd	Write to Threshold/Cal DAC
0000,1100	aaaaaa	100 000	-------------------	Pulse Test Inputs of Input Level Translators
0000,1100	aaaaaa	101 000	-------------------	Enable Data taking Mode
0000,1100	aaaaaa	110 000	-------------------	Issue Calibration Pulse
0001,1100	aaaaaa	111 000	xxxx,dddd,xxxx,xxxx	Load Bias DAC

N.B.
xxxx = don't care state.
aaaaaa = 6 bit chip address(MS bit first)
dddd = data value for register (MS bit first)

Field 3

This is an 8 bit count of the number of bits in the following instruction.

Field 4

This is the 6-bit address of the chip for which the command is intended. (See Section on Geographical Address.) N.B. To Address an ABC chip the MS bit must always be set.

Field 5

This 6 bit field is used to determine into which register on the chip the data contained in the following field will be written or which command sequence is to be executed.

Field 6

This field holds the data that is to be written into the selected register. With the exception of instruction which loads the mask register, this field will be 16-bits long.

3.2.20. Chip Initialisation and Configuration

The chip has 3 modes of operation, "Send_ID Mode", "Data_Taking Mode" and "Clock_Feed_Through_Mode". After a Power-up reset the chip is placed into Send_ID mode unless it is configured as a master with the Master input pad pulled low in which case it will be in Clock_Feed_Through_Mode.

3.2.20.1. Send ID Mode

In this mode of operation the chip sends its ID and Configuration data in response to an L1 trigger. There is no command which explicitly places the chip into this mode of operation, however, any attempt to alter the contents of the chip's various registers automatically results in the chip being placed into Send_ID mode.

3.2.20.2. Data Taking Mode.

When the chip is not in Send_ID mode it is in Data_Taking Mode and visa-versa. In this mode of operation the chip sends out any physics data that it has. The chip may be placed in this mode of operation by sending a command to the chip to enable data taking. The chip may be taken out of this mode of operation and placed into Send_ID mode by either a Power_up reset or any attempt to change the contents of the chip's registers.

3.2.20.3. Clock Feed Through Mode

If the clock feed through bit in the configuration register has been cleared and the chip has been configured as a Master, the chip outputs the chips system clock divided down by 2 from it's data output pads. This feature has been included to simplify system testing. Note that this is the power up condition if the Master input pad is pulled low.

The following sequence of instructions should normally be sent to the chip after power-up

1) Send command to load the configuration register with the appropriate settings.
2) Send a command to load the mask register
3) Send a series of commands to load the DAC register/s and Delay registers
4) Send a command to place the chip into data taking mode.
5) Send a Soft Reset command.

The chip will now be in a state to receive L1 trigger command and send data.

3.2.21. Resets

There are three kinds of reset in the system.

3.2.21.1. Power-up Reset

The Power-up Reset is an asynchronous (i.e. clock independent) reset that sets the value of the chips command register to zero, it's default value, and clears all the buffers in the chip, thus placing the chip into a well defined state. This type of reset is issued automatically when power is first applied to the chip. This reset signal can also be supplied externally via the resetB pad. The resetB pad includes an internal pull-up which maintains a non-reset state if the pad is left unconnected.

3.2.21.2. Soft Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to clear all the buffers in the chip, while leaving the configuration of the chip unaffected. This type of reset will be issued to the chip periodically during data taking to eliminate synchronisation errors.

Upon receipt of the reset command, the ABC chip resets all internal counters, clears tokens and sets itself to the no-data state. If it was transmitting data, it terminates this immediately. The value of the Level 1 counter for the first trigger read out after this command is 1. The value of the Bunch Crossing counter for an event read out from an L1 Trigger command occurring immediately (no clock gaps) after this command is 3.

N.B. It should be noted that the off-detector system must then be able to determine the last complete event transmitted before the reset and discard it (Complete in the sense that all read-out chains supply a header and trailer). With either reset it must also be able to recognise and discard partial events since there is no guarantee that different read-out chains will be reading the same event when the periodic reset arrives.

3.2.21.3. BC Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to zero the Bunch Crossing counter. It has no effect on the operation of any other part of the chip. The value of the Bunch Crossing counter for an event read out from an L1 Trigger command occurring immediately (no clock gaps) after this command is 3.

3.2.22. Data Readout and Redundancy

The figures below show the data and token interconnections on a typical silicon detector module. The module has 6-ABC chips on each side. The datalink outputs of 2 of these chips are connected to a fibre-optic interface and are configured to act as Masters in controlling the readout of data from each side of the module. On the diagrams the Master chips are denoted by a "M" and all the other chips are configured to act as slaves as denoted by a "S" or "E' on the diagram. A redundancy scheme is also employed with extra interconnections between non-adjacent chips. This scheme is intended to bypass one or more non-working chips without disabling the whole module provided no two-adjacent chips are bad. Even one Master chip can be bypassed if it or the datalink to which it connects is bad. This will be illustrated in the following figures.

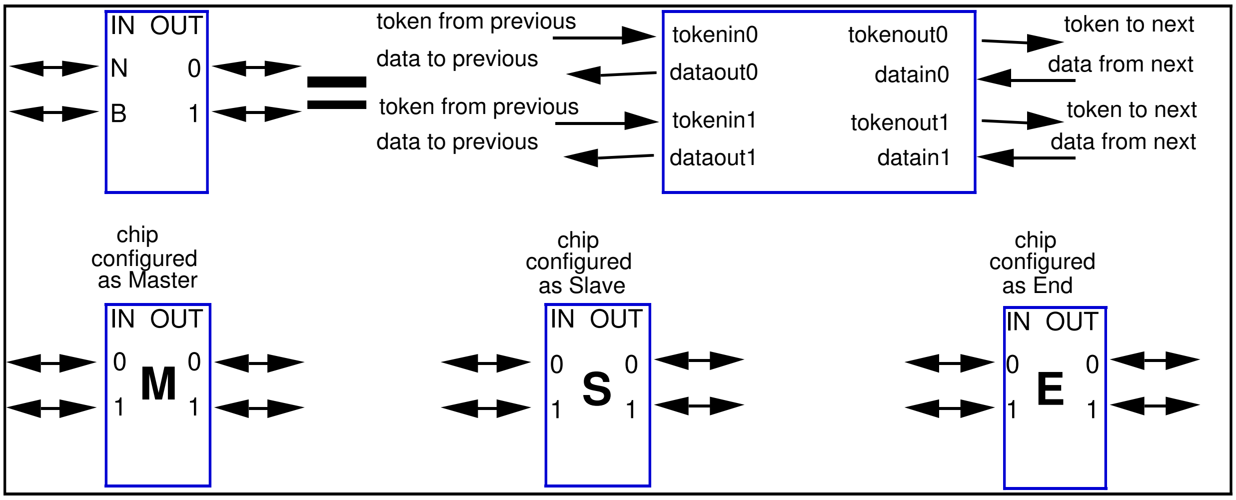

Figure 3.2.22a: Key to symbols used in following Diagrams

After the receipt of a Level 1 Trigger, the Master chip initiates a readout cycle by sending the pre-amble bits at the start of each data block to the datalink driver. It then appends its data bits to the output stream sent to the datalink driver. A few clock cycles before the last bit has been sent, it sends a token to the slave chip on it's right. The slave chip on the right responds by sending its data packet to the Master which in turn is appended to the pre-amble and data bits from the Master already sent to the datalink driver.

N.B. each chip always sends at least 3 bits of data even if it hasn't found any hit channels in the event being read out.

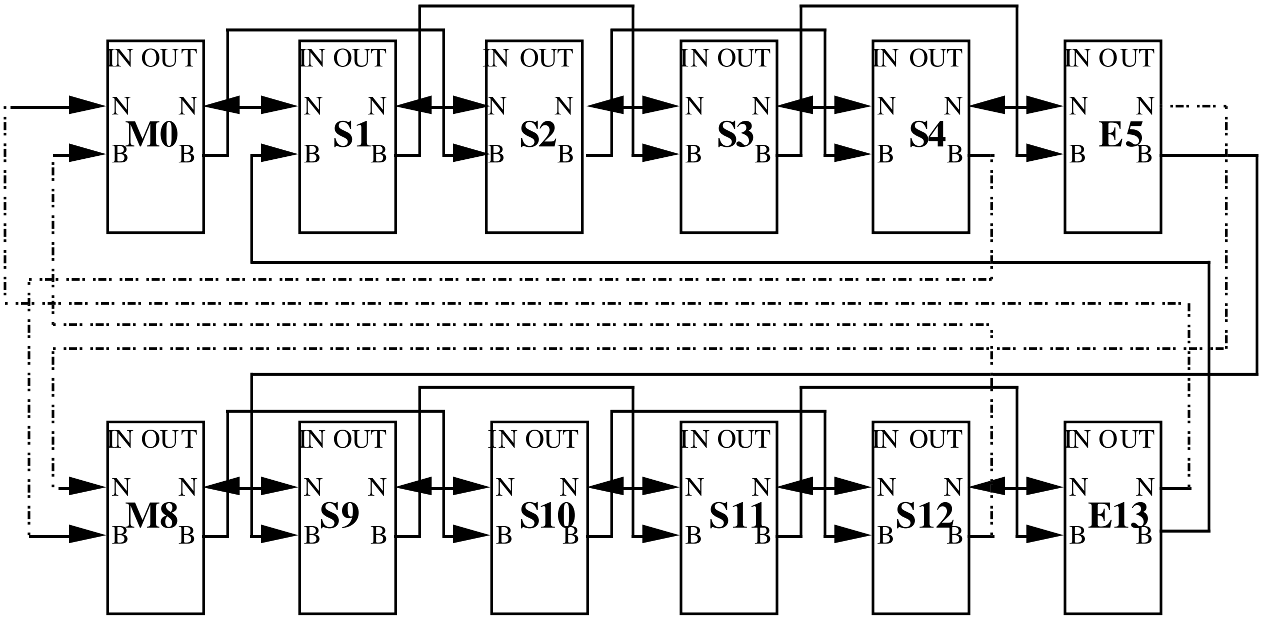

Figure 3.2.22b: Diagram of the Interconnection of ABC chips on a Silicon Detector Module

Once this slave chip has finished sending its data, it also passes on the token to the next chip on the right. The next chip on the right passes its data onto the previous chip on the left which in turn passes it back to the Master chip for transmission to the datalink driver. This process continues until the last chip in the chain has sent it's data.

A bit is set in the last chip in the chain to inform it that it is the last chip (these chips are shown as 'E' on the diagrams). When this chip has sent it's data it appends a trailer to the end of the data stream. While the Master chip is outputting data, it is constantly looking for the trailer pattern which has been carefully chosen to be distinct from the data. Once it finds the trailer pattern, it knows that all the data from the event has been sent and it can start processing the next event.

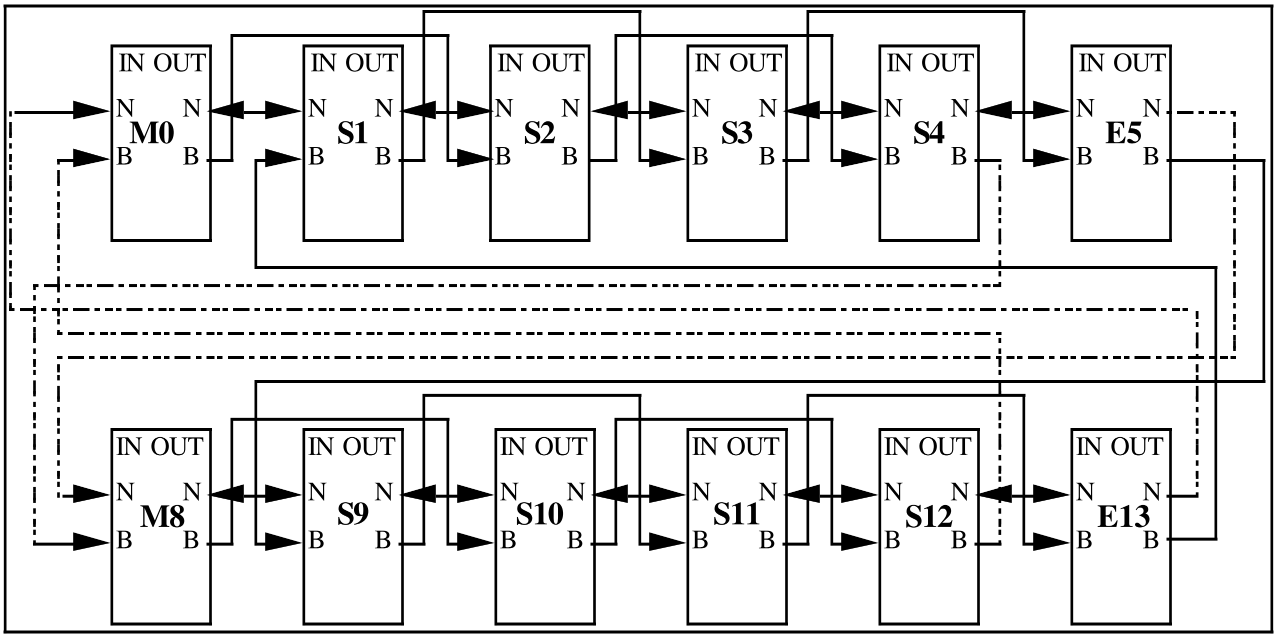

Figure 3.2.22c: Diagram Showing the Normal Flow of Data and Tokens Between Chips (Active links are highlighted with solid lines.)

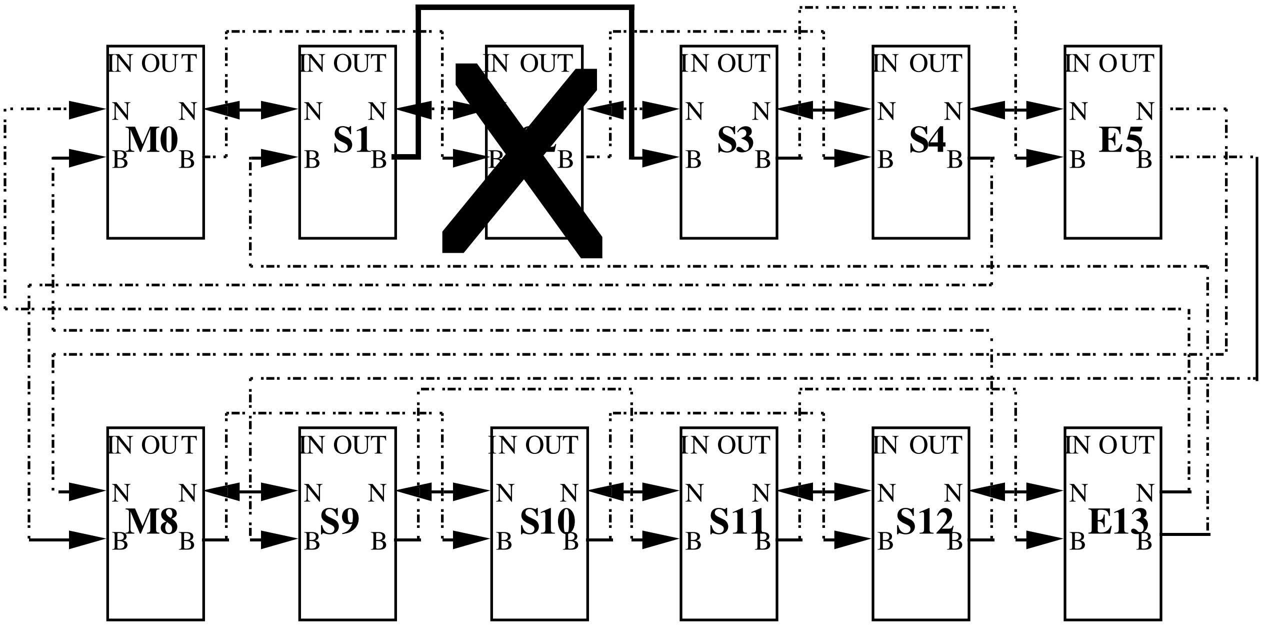

Figure 3.2.22d: Diagram Showing flow of Tokens and Data with a failed Slave ABC chip

In the event of the failure of one of the Slave chips, the previous and next slave chips in the chain are programmed to route their data and tokens around the failed chip. If the last chip in the chain should fail, then the penultimate chip in the chain is programmed to perform the operation of the "End chip".

In the event of the failure of a Master chip in the chain, the data and tokens from the chain with the failed Master chip are routed to the working master chip as shown in the next diagram .

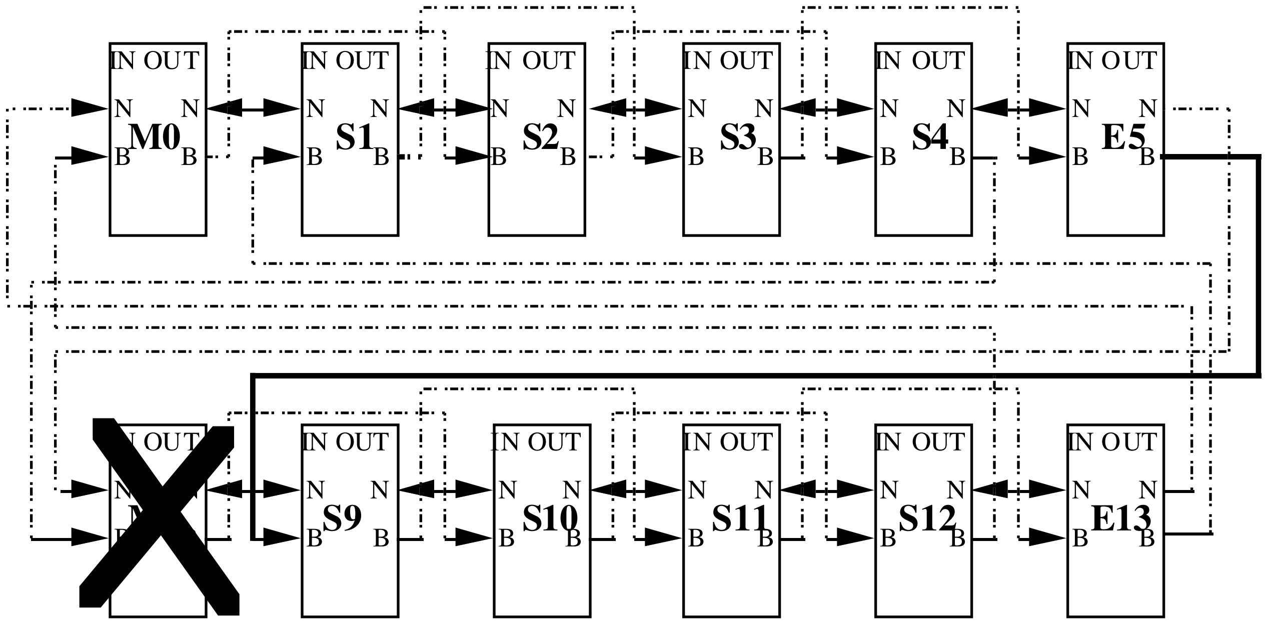

Figure 3.2.22e: Diagram Showing flow of Tokens and Data with a failed Master ABC chip

3.2.23. Default Register Values

On power up, the contents of the configuration register will be set to zero. This results in the following configuration.

Read Out Mode is set to Detector alignment mode
Calibration Mode is disabled
Send_ID mode is enabled.
tokenin0 and datain0 inputs are enabled
tokenout0 and dataout0 outputs are enabled.
Input test mode is disabled.
Edge Detection Mode disabled
Clock Feed Through Mode is Enabled if the chip is acting as a Master.
Chip will not be configured as the end of a readout chain.
The chip will be configured as a Master if masterB is asserted (i.e. pulled low), else it will be configured as a Slave.

3.2.23.1. Master/Slave Selection

The default state of the chip on power up is determined by the state on the masterB input pad. This pad has an internal pull-up which defines its state as high if left unconnected. If this pad has been left unconnected or tied high, the chip will power-up as a Slave. If this pad has been tied to ground, the chip will power up as a Master. If the chip is configured as a Master on power up it may be re-configured as a Slave. However if the chip has been configured as a Slave on power up it may not be re configured as a Master.

3.2.24. Input/Output Connections

The following the following tables describes the names and function of the various Input/Output connections to the chip.

Table 3.2.24a: Input Signals

Name	Function	Type
in<0:127>	Signal Inputs	Current Mode
clk0 & clk1	Clock input	LVDS
clk0B & clk1B	Complement of above signal	LVDS
com0 & com1	Command Input	LVDS
com0B & com1B	Complement of above signal	LVDS
tokenin0 & tokenin1	Token Input	Current Mode
tokenin0B & tokenin1B	Complement of above signal	Current Mode
datain0 & datain1	Data Input	Current Mode
datain0B & datain1B	Complement of above signal	Current Mode
id<5:0>	Geographical address of chip (with internal pull-ups on 5 & 3:0, pull-down on 4) (See Section 3.2.15.)	CMOS
masterB	Sets chip default to master (with internal pull-up)	CMOS
select	Selects clock/command inputs (with internal pull-down)	CMOS
resetB	Resets Chip (with internal pull-up)	CMOS
IDAR	Current reference for DAC	analog
CA	Input level adjustment	analog
INRH	High level input reference	analog
INRL	Low Level Input reference	analog

Table 3.2.24b: Output Signals

Name	Function	Type
tokenout0 tokenout1	Token Output	Current Mode
tokenout0B tokenout1B	Complement of above	Current Mode
dataout0 dataout1	Data Output	Current Mode
dataout0B dataout1B	Complement of above	Current Mode
datalink	Data Output to data link driver	LVDS
datalinkB	Complement of above	LVDS
CALD0	Calibration Mode Output to CAFE-P Chip	CMOS
CALD1	Calibration Mode Output to CAFE-P Chip	CMOS
CALSP	Positive Calibration Strobe Output to CAFE-P Chip	Open drain
CALSN	Complement of above	Open drain
ITH	Threshold output to CAFE-P chip	Analogue
CALI	Calibration Amplitude output to CAFE-P chip	Analogue
IVI1	Bias Current for Front Pre-amp output to CAFE-P chip	Analogue

3.2.25. Electrical Specifications

3.2.25.1. Supply Voltage

Only one supply named V_{DD} is required for the chip. See Section 3.2.25.3 below for discussion of various supply pads.

Table 3.2.25a: Supply Voltage Requirements

	Operational		Absolute
Minimum	Nominal	Maximum	Maximum
3.8 V	4.0 V	4.2 V	6.5 V

For the on chip Power-on Reset circuitry to operate correctly the power supply must be ramped up to 90% of its final value in less than 10 ms.

3.2.25.2. Power Consumption

Power consumption depends upon the mode of operation of the chip since the LVDS driver circuit for the datalink output only operates in Master mode. Nominal values in Table 3.2.25b are for nominal fabrication parameters and nominal supply voltage. Max values are for worst case fabrication parameters and Max operating supply voltage. Both Nominal and Max assume either 1% hit occupancy and 100 kHz trigger rate or 25% hit occupancy and 4 kHz trigger rate whichever is largest.

Table 3.2.25b: Current Requirements

Mode	Nominal Pre-rad	Max Pre-rad	Nominal Post-rad	Max Post-rad
Master	TBD	TBD	TBD	TBD
Slave	TBD	TBD	TBD	TBD
Master - no clk	TBD	TBD	TBD	TBD
Slave - no clk	TBD	TBD	TBD	TBD

3.2.25.3. Power Supply Connections

The chip has a total of 11 power supply connection pads. (In the following discussion, the orientation of chip edges refers to that shown in Figure 3.2.27b.) Three of these 11 pads, labeled DRET, are in the row of pads on the left edge of the chip. These pads are intended to provide a return path for the switching currents in the input stage of the chip. These pads should be connected directly to the corresponding pads on the CAFE-P chip. The set of 2 pairs of power connections, labeled vdd! and gnd!, on the right edge of the chip provide all the power to the digital Sections. These pads should be connected to the digital power supply for the chip. There is another pair of power pads along the top edge of the chip, labeled dac_vdd! and dac_gnd!, to provide power to the DAC section and another pair of pads along the bottom edge labeled ILT_vdd! and ILT_gnd! to provide power to the Input Level Translator section. Both of these pairs of pads must also be connected to the same digital supply for the chip. The separate pads are provided for better isolation on chip. Note that DRET and ILT_gnd! are internally the same node. ILT_gnd!, dac_gnd! and gnd! are internally connected through resistive metal lines. This is to insure that all ground metal is at the same potential as the substrate ground.

3.2.25.4 Input /Output Levels

Table 3.2.25c: Input Levels for Hit Inputs

Parameter	Minimum	Typical	Maximum
Low Level Input Current I_{IL}		0µA	10µA
High Level Input Current I_{IH}	75µA	200µ	320µA
Compliance (active or inactive state)	0.7V		VDD
Voltage Diff of any INRH, INRL, INxx			0.5V

Table 3.2.25d: Output Levels for Calibration Code Outputs

Parameter	Minimum	Typical	Maximum
Low Level Voltage V_{OL}	VSS		0.5 V
High Level Voltage V_{OH}	VDD - 0.5V		VDD

Table 3.2.25e: Output Levels for Calibration Strobe Outputs

Parameter	Minimum	Typical	Maximum
Low Level Output Current I_{OL}		11µA	18µA
High Level Output Current I_{OH}	180µ	242µ	

Load capacitance for all cases is less then 1pF.

Table 3.2.25f: Input Levels for LVDS Inputs (Clock, Control)

Parameter	Conditions	Minimum	Maximum	Units
Input Voltage Range V_i	$V_{gpd} \leq 950mV$	0	2400	mV
InputVoltage Common mode V_{icm}	$V_{gpd} \leq 950mV$	50	2350	mV
Differential high input threshold $+V_{idth}$	$V_{gpd} \leq 950mV$		100	mV
Differential high input threshold $-V_{idth}$	R_{load} =100Ω±1%	-100		mV
Threshold hysteresis	(+Vid) - (Vid)	25		mV
Receiver input impedance		100 k		Ω

N.B. No internal terminating resistor is built into these inputs and consequently an external resistor terminated resistor is required.

Table 3.2.25g: Input Levels for Token and Data Inputs (Token_in, Data_in)

Parameter	Minimum	Typical	Maximum
Low Level Input Voltage V_{IL}		VDD/2 - 100 mV	
High Level Input Voltage V_{IH}		VDD/2 + 100 mV	
Receiver input impedance		120 Ω	

Table 3.2.25h: Output Levels for Token and Data Outputs (Token_Out, Data_out)

Parameter	Conditions	Minimum	Typical	Maximum
Output Voltage Low V_{OL}	C_L=50 pf R_{load}=125 Ω		VDD/2 - 100mV	
Output Voltage High V_{OH}	C_L=50 pf R_{load}=125 Ω		VDD/2 - 100mV	
Output Differential Voltage	C_L=50 pf R_{load}=125 Ω		200 mV	

Table 3.2.25i: Output Levels for Datalink Outputs

Parameter		Minimum	Maximum	Units
Output Voltage low V_{OL}	R_{load} =100Ω±1%	1000		mV
Output Voltage High V_{OH}	R_{load} =100Ω±1%		1400	mV
Output offset Voltage	R_{load} =100Ω±1%	1125	1275	mV
Output Differential Voltage	R_{load} =100Ω±1%	250	400	mV
Output impedance	I_{load} =2mA to 3mA	40	280	Ω

Table 3.2.25j: DAC Input and Output levels

Parameter	Minimum	Typical	Maximum
IDAR DAC reference current	-270µA	-300µA	-363µA
CALI	-(IDAR/256) *num -10%	-(IDAR/256) *num	-(IDAR/256) *num +10%
ITH	(IDAR/256) *num -10%	(IDAR/256) *num	(IDAR/256) *num +10%
IVI1	-(IDAR*1.2/16) *num -10%	-(IDAR*1.2/16) *num	-(IDAR*1.2/16) *num +10%

Num is the value loaded into the DAC register

3.2.26. Timing Specifications

Many timing specifications will only be determined after chips are fabricated and characterized. Some requirements which can be specified now are as follows:

Table 3.2.26a: Clock Timing Specifications

Parameter	Minimum	Typical	Maximum
clk duty cycle	TBD	50%	TBD
clk rising edge to com rising edge	TBD		TBD
com high time	TBD		clk period
clk rising edge to datain rising edge	TBD		TBD
clk rising edge to tokenin rising edge	TBD		TBD
clk rising edge to datalink rising edge	TBD		TBD
clk rising edge to dataout rising edge	TBD		TBD
clk rising edge to tokenout rising edge	TBD		TBD

Table 3.2.26b: Calibration Output Timing Specifications

Parameter	Minimum	Typical	Maximum
CALSP/CALSN strobe width	125 ns		
CALSP/CALSN strobe edge delay after rising clk edge of command receipt (Strobe Delay Reg = 0)	0 ns		
Step size of Strobe Delay Reg	0.6 ns	1.1 ns	1.6 ns
CALSP/CALSN risetime (differential)			4 ns
CALSP/CALSN delay after transition of CALD0, CALD1 (determined by command control)	250 ns		
Off interval between consecutive CALSP/CALSN pulses (determined by command control)	250 ns		

3.2.27. Physical Layout

The digitized area of the chip has dimensions 5.450 mm x 5.800 mm. The spacing on the reticle for wafer printing is 5.700 mm x 6.100 mm. The final cut die size is dependent upon the saw cut but should have approximate dimensions 5.670 mm x 6.070 mm with an uncertainty of $\pm$20 µm in each dimension.

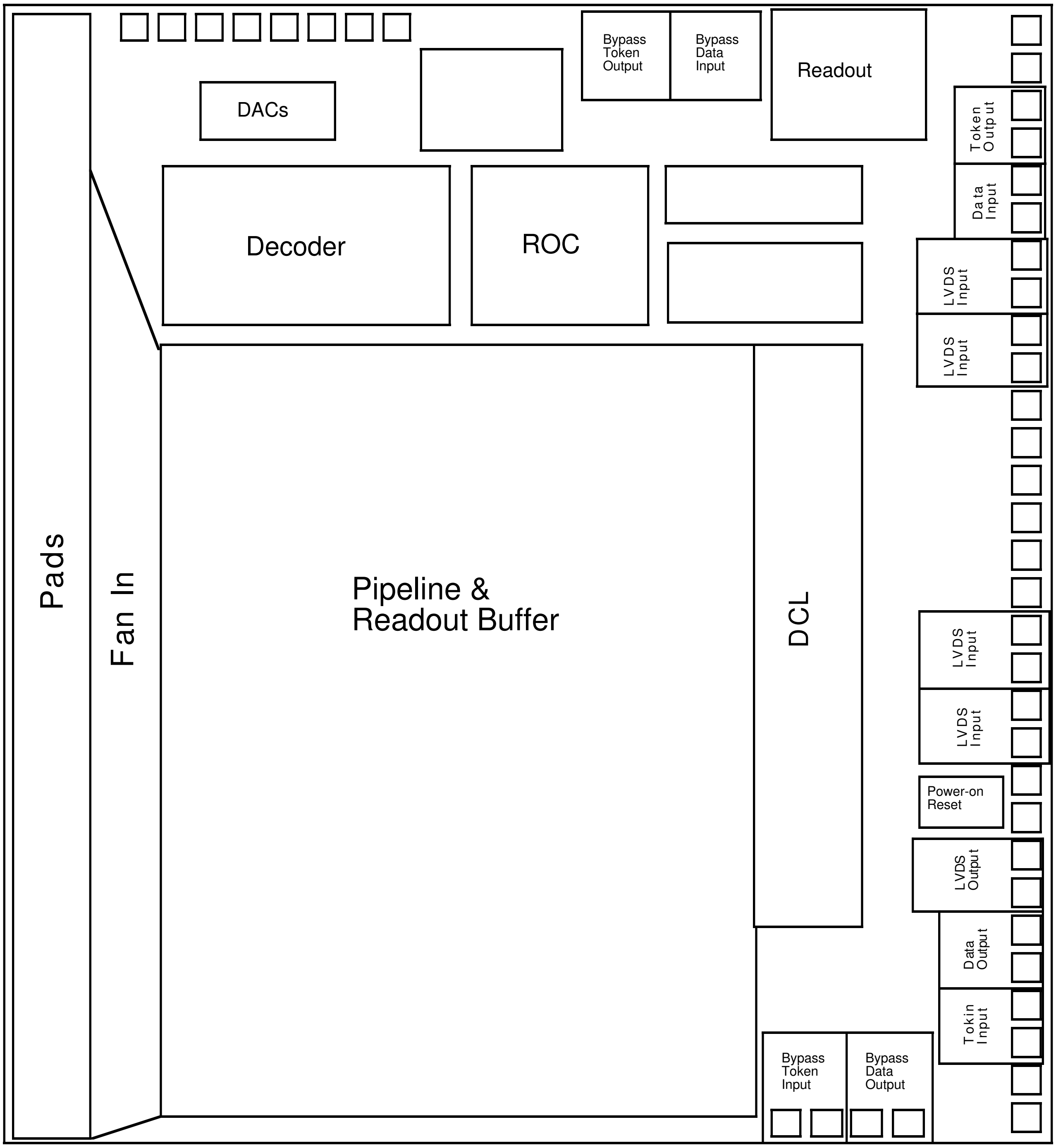

Figure 3.2.27a: Chip Layout

Note Channel 0 is at the lower edge of this figure. The other channels, addressed 1 through 127, are located consecutively from bottom to top. This numbering convention affects which channels are tested by the binary encoded channel address lines, calmode(1:0), to the Input Level Translators (See Section 3.2.1.) and the channel addresses which become part of the Physics Data reported by the chip (See Section 3.2.17.). This also corresponds to the CAFE-P pad layout.

3.2.27.1. Bond Pad Arrangement

The bond pad arrangement of the ABC is shown in the figure and table below. Not all of the test pads are shown in the figure. The pads on the left edge of the chip have been arranged on a pitch which enables the ABC chip to be wire bonded directly to the CAFE-P chip. All pads critical to chip functionality are ≥150 µm wide to accommodate double bond wires for greater reliability. The chip dimensions shown in the figure are for the digitized area, not the final cut die size.

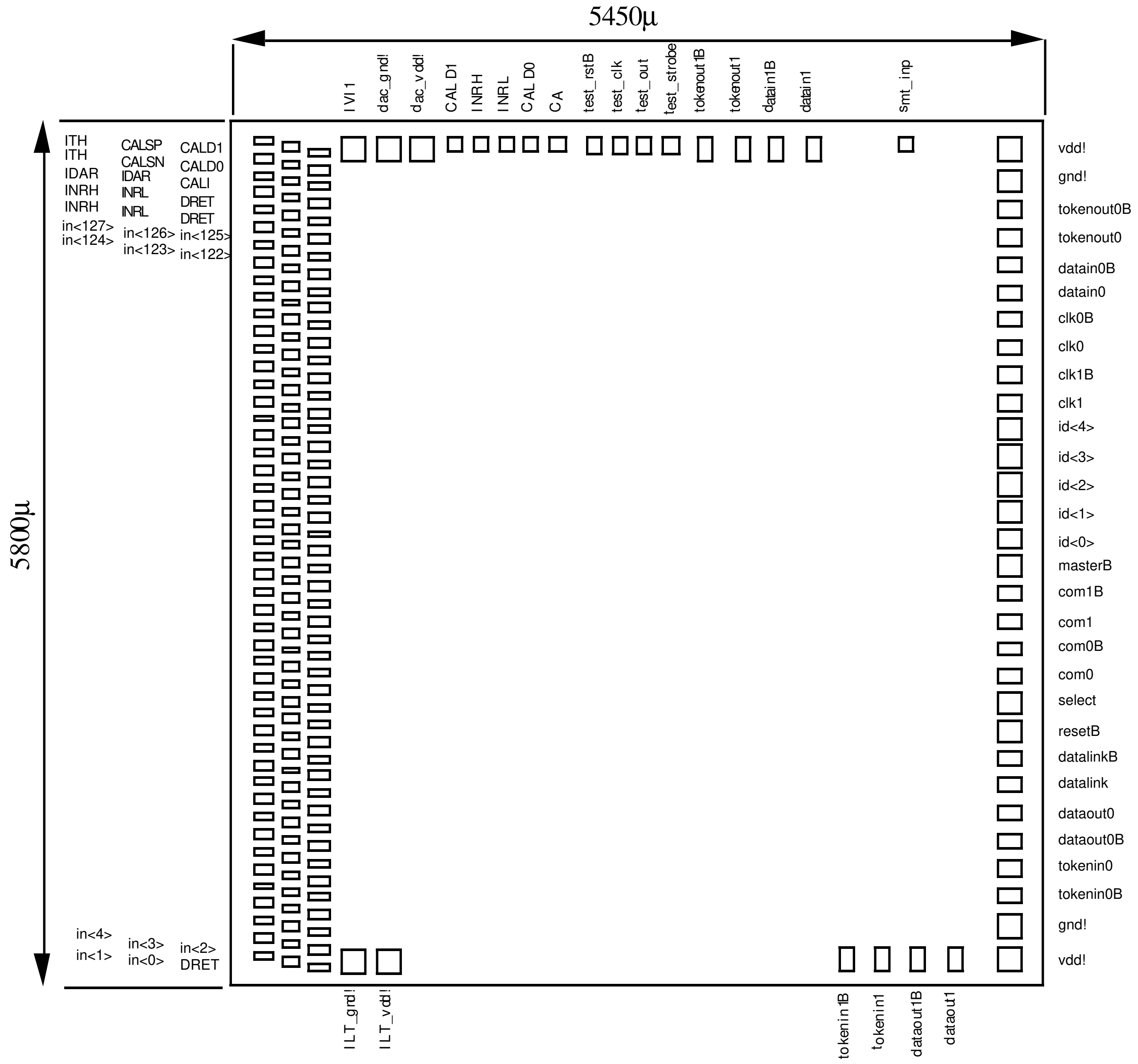

Figure 3.2.27b: Chip Pad Layout

Table 3.2.27: Bond Pad Coordinates
Coordinates at centre of each pad are from lower left corner of digitized area as seen in Figure 3.2.27b. Sizes are for pad openings. Metal areas of pads are slightly larger.

Left Edge	1st row					**Left Edge**	2nd row			
Pad Name	**Centre (x)**	**Centre (y)**	**Size (x)**	**Size (y)**		**Pad Name**	**Centre (x)**	**Centre (y)**	**Size (x)**	**Size (y)**
in<1>	78	118	140	60		in<0>	278	78	140	60
in<4>	78	238	140	60		in<3>	278	198	140	60
in<7>	78	358	140	60		in<6>	278	318	140	60
in<10>	78	478	140	60		in<9>	278	438	140	60
in<13>	78	598	140	60		in<12>	278	558	140	60
in<16>	78	718	140	60		in<15>	278	678	140	60
in<19>	78	838	140	60		in<18>	278	798	140	60
in<22>	78	958	140	60		in<21>	278	918	140	60
in<25>	78	1078	140	60		in<24>	278	1038	140	60
in<28>	78	1198	140	60		in<27>	278	1158	140	60
in<31>	78	1318	140	60		in<30>	278	1278	140	60
in<34>	78	1438	140	60		in<33>	278	1398	140	60
in<37>	78	1558	140	60		in<36>	278	1518	140	60
in<40>	78	1678	140	60		in<39>	278	1638	140	60
in<43>	78	1798	140	60		in<42>	278	1758	140	60
in<46>	78	1918	140	60		in<45>	278	1878	140	60
in<49>	78	2038	140	60		in<48>	278	1998	140	60
in<52>	78	2158	140	60		in<51>	278	2118	140	60
in<55>	78	2278	140	60		in<54>	278	2238	140	60
in<58>	78	2398	140	60		in<57>	278	2358	140	60
in<61>	78	2518	140	60		in<60>	278	2478	140	60
in<64>	78	2638	140	60		in<63>	278	2598	140	60
in<67>	78	2758	140	60		in<66>	278	2718	140	60
in<70>	78	2878	140	60		in<69>	278	2838	140	60
in<73>	78	2998	140	60		in<72>	278	2958	140	60
in<76>	78	3118	140	60		in<75>	278	3078	140	60
in<79>	78	3238	140	60		in<78>	278	3198	140	60
in<82>	78	3358	140	60		in<81>	278	3318	140	60
in<85>	78	3478	140	60		in<84>	278	3438	140	60
in<88>	78	3598	140	60		in<87>	278	3558	140	60
in<91>	78	3718	140	60		in<90>	278	3678	140	60
in<94>	78	3838	140	60		in<93>	278	3798	140	60
in<97>	78	3958	140	60		in<96>	278	3918	140	60
in<100>	78	4078	140	60		in<99>	278	4038	140	60
in<103>	78	4198	140	60		in<102>	278	4158	140	60
in<106>	78	4318	140	60		in<105>	278	4278	140	60
in<109>	78	4438	140	60		in<108>	278	4398	140	60
in<112>	78	4558	140	60		in<111>	278	4518	140	60
in<115>	78	4678	140	60		in<114>	278	4638	140	60
in<118>	78	4798	140	60		in<117>	278	4758	140	60
in<121>	78	4918	140	60		in<120>	278	4878	140	60
in<124>	78	5038	140	60		in<123>	278	4998	140	60
in<127>	78	5158	140	60		in<126>	278	5118	140	60
INRH	78	5276	140	60		INRL	278	5236	140	60
INRH	78	5396	140	60		INRL	278	5356	140	60
IDAR	78	5518	140	60		IDAR	278	5478	140	60
ITH	78	5638	140	60		CALSN	278	5598	140	60
ITH	78	5758	140	60		CALSP	278	5718	140	60

Left Edge	3rd row					**Top Edge**				
Pad Name	**Centre (x)**	**Centre (y)**	**Size (x)**	**Size (y)**		**Pad Name**	**Centre (x)**	**Centre (y)**	**Size (x)**	**Size (y)**
DRET	478	38	140	60		IVI1	809	5717	160	150
in<2>	478	158	140	60		dac_gnd!	1009	5717	160	150
in<5>	478	278	140	60		dac_vdd!	1209	5717	160	150
in<8>	478	398	140	60		tokenout1B	3192	5712	100	160
in<11>	478	518	140	60		tokenout1	3442	5712	100	160
in<14>	478	638	140	60		datain1B	3692	5712	100	160
in<17>	478	758	140	60		datain1	3942	5712	100	160
in<20>	478	878	140	60						
in<23>	478	998	140	60		**Right Edge**				
in<26>	478	1118	140	60		**Pad Name**	**Centre**	**Centre**	**Size**	**Size**
in<29>	478	1238	140	60		vdd!	5362	88	160	160
in<32>	478	1358	140	60		gnd!	5362	308	160	160
in<35>	478	1478	140	60		tokenin0B	5362	525	160	100
in<38>	478	1598	140	60		tokenin0	5362	715	160	100
in<41>	478	1718	140	60		dataout0B	5362	905	160	100
in<44>	478	1838	140	60		dataout0	5362	1095	160	100
in<47>	478	1958	140	60		datalink	5362	1285	160	100
in<50>	478	2078	140	60		datalinkB	5362	1475	160	100
in<53>	478	2198	140	60		resetB	5362	1665	160	150
in<56>	478	2318	140	60		select	5362	1855	160	150
in<59>	478	2438	140	60		com0	5362	2045	160	100
in<62>	478	2558	140	60		com0B	5362	2235	160	100
in<65>	478	2678	140	60		com1	5362	2425	160	100
in<68>	478	2798	140	60		com1B	5362	2615	160	100
in<71>	478	2918	140	60		masterB	5362	2805	160	150
in<74>	478	3038	140	60		id<0>	5362	2995	160	150
in<77>	478	3158	140	60		id<1>	5362	3185	160	150
in<80>	478	3278	140	60		id<2>	5362	3375	160	150
in<83>	478	3398	140	60		id<3>	5362	3565	160	150
in<86>	478	3518	140	60		id<4>	5362	3755	160	150
in<89>	478	3638	140	60		clk1	5362	3945	160	100
in<92>	478	3758	140	60		clk1B	5362	4135	160	100
in<95>	478	3878	140	60		clk0	5362	4325	160	100
in<98>	478	3998	140	60		clk0B	5362	4515	160	100
in<101>	478	4118	140	60		datain0	5362	4705	160	100
in<104>	478	4238	140	60		datain0B	5362	4895	160	100
in<107>	478	4358	140	60		tokenout0	5362	5085	160	100
in<110>	478	4478	140	60		tokenout0B	5362	5275	160	100
in<113>	478	4598	140	60		gnd!	5362	5492	160	160
in<116>	478	4718	140	60		vdd!	5362	5712	160	160
in<119>	478	4838	140	60						
in<122>	478	4958	140	60		**Bottom Edge**				
in<125>	478	5078	140	60		**Pad Name**	**Centre**	**Centre**	**Size**	**Size**
DRET	478	5198	140	60		ILT_gnd!	708	83	160	150
DRET	478	5318	140	60		ILT_vdd!	908	83	160	150
CALI	478	5438	140	60		tokenin1B	4242	88	100	160
CALD0	478	5558	140	60		tokenin1	4492	88	100	160
CALD1	478	5678	140	60		dataout1B	4742	88	100	160
						dataout1	4992	88	100	160

Top Edge	Intended for wafer probe					**Misc. Locations**	Intended for Diagnostics			
Pad Name	**Centre (x)**	**Centre (y)**	**Size (x)**	**Size (y)**		**Pad Name**	**Centre (x)**	**Centre (y)**	**Size (x)**	**Size (y)**
CALD1	1409	5740	100	100		IDAR	673	5344	20	20
INRH	1609	5740	100	100		ITH	708	5570	20	20
INRL	1809	5740	100	100		CALSP	1460	5629	20	20
CALD0	2009	5740	100	100		CALSN	1526	5629	20	20
CA	2209	5740	100	100		ndrain1p2	882	283	60	100
						pdrain5	882	458	60	100
Top Edge	Intended for Diagnostics					ndrain0p8	1002	258	60	100
Pad Name	**Centre**	**Centre**	**Size**	**Size**		pdrain2	1002	458	60	100
						ndrain2	1122	58	60	100
test_rstB	2482	5742	100	100		ngate	1122	258	60	100
test_clk	2662	5742	100	100		pdrain1p2	1122	458	60	100
test_out	2842	5742	100	100		ndrain5	1242	58	60	100
test_strobe	3022	5742	100	100		psource	1242	258	60	100
tokenBackB	4460	5596	30	30		pdrain0p8	1242	458	60	100
datainB	4460	5686	30	30		nsource	1362	58	60	100
poweron_rst	4460	5776	30	30		pvdd	1362	258	60	100
smt_inp	4624	5741	100	100		pgate	1362	458	60	100
						gnd!	1758	258	60	100
						token_startB	4253	684	30	30
						data_validB	4370	684	30	30
						tokenin	4769	1046	30	30
						dataoutB	4769	1146	30	30
						com<1>	4769	1903	30	30
						datalink_test	4769	3136	30	30
						clk<1>	4769	3423	30	30
						ILT_out<11>	1029	1069	20	20
						ILT_out<26>	1029	1443	20	20
						ILT_out<41>	1029	1813	20	20
						ILT_out<56>	1029	2187	20	20
						ILT_out<71>	1029	2557	20	20
The next two pads have no passivation cut.						ILT_out<86>	1029	2931	20	20
smt_out	4765	5738	20	20		ILT_out<91>	1029	3301	20	20
vdiode	4752	5658	20	20		ILT_out<116>	1029	3675	20	20