The Semiconductor Tracker Detector Control System Requirements Document

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1. Introduction

This document is planned to become an appendix to the "ATLAS Detector Control System User Requirement Document"[1]. The requirements are written in the same format as the main document. This document is the result of discussions on the ATLAS SCT DCS held the 18. October 1996 at CERN. There may be requirements that will be removed from this document because the part they describe is not part of the DCS. There will probably be new requirements added to the document.

2. Definitions

Module = A unit consisting of silicon sensors, a hybrid and readout electronics.

Stave = A unit consisting of several modules (10-12) with an independent cooling circuit.

The user requirements are qualified with the following attributes:

Need: Level of importance
- **essential:** must be implemented
- **desirable:** should be implemented if not too difficult
- **optional:** would be nice to have

Priority: for incremental delivery of DCS
- **Phase I:** stand-alone operation with reduced functionality
- **Phase II:** Final system with integrated operation

Stability: indicates whether the requirement is expected to change
- **stable:** is not expected to change
- **tbc:** to be confirmed, might not be needed

Source: who has asked for this requirement
- **general:** needed by most users
- **DCS:** requested by DCS
- **SCT:** requested by SCT

3. Requirements

3.1 Control and monitoring of low voltages:

SCT-LV1 Every module shall have independent low voltage supplies.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-LV2 The low voltage levels shall be controlled to a precision better than 5% at the module.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-LV3 The low voltage levels shall be known at the module to a precision better than 1%.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-LV4 The status of the low voltage supplies shall be monitored. (ON/OFF/TRIP/INTERLOCK).
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-LV5 The low voltage supplies shall activate an interlock signal when switched off which will act on the high voltage supplies of the same module.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-LV6 It is desirable to know the low voltage interlock configuration which act on the high voltage.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-LV7 The resolution of the monitoring of the low voltages shall be better than 1% of the full range.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-LV8 Overcurrent trip level for low voltage supplies shall be adjustable.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-LV9 The overcurrent limit should have a time setting.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

3.2 Control and monitoring for high voltages:

SCT-HV1 Every module shall have independent high voltage supplies.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV2 High voltage levels shall be controlled at the module to a precision better than 5%.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV3 High voltage levels shall be monitored at the module with a precision better than 1%.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV4 The high voltage supplies shall be individually interlocked.
Need desirable ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV5 The high voltage supplies for a module shall be interlocked if the low voltage for that module is interlocked or switched off.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV6 The status of the high voltage supplies shall be monitored.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV7 The current in the high voltage supplies should be monitored in multirange with higher absolute precision at low current than for high currents.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-HV8 The high voltage supplies shall trip if the current exceed a preset value.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV9 The current trip level for the high voltage supplies should be programmable by computer.
Need desirable ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-HV10 The ramp-up speed of the high voltage supplies should be programmable by computer.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-HV11 The ramp down speed of the high voltage supplies shall be hard-wired.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

3.3 Temperature monitoring

SCT-TMP1 The temperature shall be monitored on every module.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-TMP2 Two independent temperature values shall be monitored inside SCT on every stave.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-TMP3 The air temperature inside SCT shall be monitored.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-TMP4 The temperature in the cable bundle bringing power to the SCT inside the TRT should be monitored.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-TMP5 The relative precision of the temperature measurement shall be better than 0.3 deg.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-TMP6 The absolute precision of the temperature measurement shall be better than 1 deg.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-TMP7 The temperature monitoring shall be functional after the power is cut in the experiment.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-TMP8 The interlock signal generated by the temperature monitoring of a staves shall be hardwired to the power supplies for the modules mounted on the stave generating an interlock.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-TMP9 The trip temperature shall be individually adjustable for every stave.
Need essential ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-TMP10 The trip temperature should be hardwired and adjustable.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

3.4 Pressure monitoring

SCT-PRE1 The air pressure should be monitored inside the SCT.
Need desirable ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-PRE2 The air pressure should be measured with a precision better than 1mbar.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-PRE3 The air pressure should be measured over a range from 960mbar - 1060mbar.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

3.5 Humidity monitoring

SCT-HUM1 The humidity should be measured inside the SCT.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-HUM2 The humidity should be measured with a precision better than 1%.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

SCT-HUM3 The humidity should be measured over a range from 0% - 100%.
Need desirable ; **Priority** Phase II ; **Stability** tbc ; **Source** SCT

3.6 Status monitoring

SCT-STA1 The status of the valves regulating the flow of coolant in the stave should be monitored.
Need desirable ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

3.7 Data logging

SCT-DAT1 All the information available from the control and monitoring shall be kept for minimum a week.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

SCT-DAT2 The data from the control and monitoring shall be kept in compressed format after a week.
Need essential ; **Priority** Phase II ; **Stability** stable ; **Source** SCT

References

[1] ATLAS Detector Control System User Requirement Document, PSS05-ATLAS-DCS-URD, 15 August 1995