Project Specification
Project Name: Atlas **S**CT **H**V Power Supply (**ASH)**
Version: V2.04

Project History

Version	Description	Group	Date
	Primary requirements for n-on-n detectors. Voltage range 50 - 300V. Max. current 4 mA. Channels with common ground.		1995 SCT - Munich meeting
1.03	First design and prototype of 300 V, 5 mA 24 fully isolated channels	P.Bartkiewicz, E.Górnicki, S.Koperny, B.Madeyski	July 1997
2.0	New requirements for the p-on-n detectors ...		
2.02	New design and second prototype of HV card for VME with 4 fully isolated channels providing voltage range 0 - 410V and maximum current of 5 mA	E.Górnicki, S.Koperny, B.Madeyski, P.Malecki	July 1999
2.03	Prototype of HV card/ 8 channels, common HV&LV special crate, crate controller, CANbus interface to DCS	E.Górnicki, S.Koperny, P.Malecki	
2.04	Prototype of HV card/ 8 channels, 0-500V, common HV&LV special crate, crate controller, CANbus interface to DCS	E.Górnicki, S.Koperny, P.Malecki	February 2001

1. Scope

The aim of this project is to develop multi-channel power supplies providing stabilized regulated bias voltage (HV) for micro strip silicon detectors of the LHC ATLAS semi-conductor tracker (SCT).

The modular structure of this power supply follows the structure of the SCT detector. This project is closely related to the project of low voltage (LV) multi-channel power supplies providing various voltages for front-end electronics of the SCT detector. LV power supplies are described in a separate specification.

Both, LV and HV power supplies are integrated to form a common SCT Power Supply System. This integration is on the level of crate. Cards with equal number of LV and HV channels are located in a common crate and serviced by the common crate controller, common crate power supply and crate control software. The crate specification is documented separately.

2. Related projects and documents

2.1. Prague Group Low Voltage Power Supplies for SCT FE Electronics SCT Week, 9-13 March 1998

2.2. Project Specification for CAFE-P, Version V4.01 13-Jan99

2.3. Project Specification for ATLAS Binary Chip (ABC). Version V5.01 21 Jul-99

2.4. Project Specification for Digital Opto-Receiver Integrated Circuit (DORIC4), A Front End Clock and L1 Distribution Chip. Version 1.02

2.5. ABCD Spec (Version 2.1 10-Apr-99)

2.6. Project Specification for VDC, a dual VCSEL Driver Circuit. Version 1.00.

2.7. The Semiconductor Tracker Detector Control System Requirements Document by Richard Brenner

2.8. Specifications for ATLAS Silicon Microstrip Detectors for the ATLAS Final Design Review (ATLAS SCT/Detector FDR/99-2)

3. Requirements

3.1. Modularity

This multi-channel HV power supply system has modular structure. All channels are independent, fully floating. Certain fixed number of channels are mounted on a single board. This number should be chosen in such a way that HV and corresponding LV boards servicing the same detector channels are easily identified.

3.2. Voltage

- Nominal value in range 0 - 500 V. Floating, controlled with an accuracy better then 2 %.
- Nominal voltage setting by a digital input with a precision of 500 mV.
- Voltage level monitored at each channel with an accuracy better than 2%.
- Channel reaction time to the new voltage setting (to start ramping procedure) - 20 ms.
- The ramp-up and ramp-down speed programmable in range 5 – 50 V/s.
- Allowable noise level 40 mV peak.
- Hard-wired over-voltage trip level programmable by computer.
- No remote sensing and feedback control.

3.3. Current

- Current measurement range 40 nA - 5 mA.
- Current monitoring accuracy - multirange, with the precision corresponding to the 10-bit ADC at each range.
- Hard-wired over-current trip with the trip level programmable by computer
- Absolute over-current limit protection at the 5.2 mA

3.4. Control

- Every channel is equipped with a status register latching the trip cause.
- A logical status of each channel is monitored and reporting :
  - ON/OFF state,
  - TRIP reason (overcurrent or overvoltage)
  - Channel switched off by INTERLOCK
  - Channel switched off by crate OVERTEMPERATURE
- All channels are set to 0 V on power-up reset.
- Previous settings can only be restored by a software action.

3.5. Interlocks

All interlocks call equal or alike actions for low voltage and high voltage power supplies:

- interlock initiated by the DCS switches off the HV channel and equivalent LV channel and sends its status information to the DCS.
- interlock initiated by an internal over-temperature crate control switches off the whole HV/ LV crate and sends its status to the DCS.

4. Specification of deliverables

4.1. General Structure

6U-220 Europe-standard card provide 8 fully floating power supply output lines - channels. The output of every channel can be set to the voltage from the range of 0 to 500V and can provide 5 mA maximum current. Each channel comprises one microprocessor which controls all functions of the channel. All these channel microprocessors communicate with the common card controller through optical couplers.

The crate controller, common for LV and HV boards integrated in a given crate, provides an external communication via CAN bus protocol and internal communication with card controllers located on each board (one per board). Details of this control are described in the separate specification. Card controller communicates, on the other hand, with channel controllers servicing channels located on a given

board. Functions of card and channel controllers are specified in following sections.
All HV cards in the crate have common supplies: AC 58V, 48kHz for HV channels (max 1A per card) and DC 5V for common digital part of the card (max.0.5A per card).

All components are not qualified as radiation hard, not even radiation tolerant devices. It is assumed that all power supply crates are situated far from the detector.

Guaranted working temperature is 0°C - 60°C and it is determined on temperature range of used components.

4.2. HV Channel

Block diagram of the HV channel is shown on Fig.1

4.2.1. AC/DC Converter

AC input 58 V, 48 kHz comes from main crate power supply located at the rear of the crate. It is common for all channels in the crate. AC/DC converter will produce isolated 600 V for each channel and also +6V and -6V to supply all chips and microprocessor of the channel.

4.2.2. Rectifier and filter

High speed diodes UF4007 are used as rectifying diodes before voltage doubler stage. Next, to reduce ripple noise, the high voltage RC filter is applied.

4.2.3. Regulator

The high voltage MOSFET power transistor IRF 820 is used as the series regulator.

4.2.4. Over-current protection

Absolute over current protection is set to 5.2 mA. If the current exceeds this value the voltage is automatically reduced. In such a case, the software will trip this channel.
The reaction time is below 1 ms.

4.2.5. Over-current level setting

It is possible to set the over-current level to desirable value from the range of 0.5 uA - 5mA. If the current exceeds the value set for the given channel then it is detected during the nearest cycle of the current reading. Consequently, the control circuits will cut-off the serial regulator on this channel and the output voltage will go to 0V. Maximum reaction time is 1ms.

4.2.6. Over voltage level setting

When the voltage readout value exceeds the value set for the channel by more than 5 % then the control circuit cuts-off the voltage on this channel and, similarly to the case of the over current, the voltage should go to 0 V. If, however, the voltage readout detects still some voltage on the output, the card processor will shut-down the channel definitively by cutting the power for this channel.

For switching this channel on again the special procedure is used which will detect whether the channel is properly reset or will detect persistent hardware error.

4.2.7. Voltage setting

Microprocessor can set the voltage to the required value by starting ramp-up or ramp-down procedure. This will set the 10 bit serial DAC on. Ramp-up and down rates are to be chosen from several preset values. It may happen that the ramp-down rate will be determined by the time constant of the circuit rather then by the controller. Preset values are 5 V/s, 10 V/s, 20 V/s, 50 V/s.

4.2.8. Voltage readout

The channel microcontroller continuously reads the voltage and output current. One measurement cycle takes about 20 msec. The voltage readout accuracy is determined by the factor proportional to the nominal value (0.5%) and by two least significant bits of the 12 bits ADC.

4.2.9. Current readout

Every channel is equipped with the multi-range current read-out system. Actually, one of the following four ranges are selected automatically to provide an accurate current measurement. These ranges partially overlapping. Their limiting values are:

FUNCTION	**RANGE**	**ACCURACY**	**RESOLUTION**
Voltage	0 – 500 V	+/- (0.1% of rdg. + 2 digits)	1 dgt = 125 mV
Current	42.0µA 209.2µA 1.029mA 5.2mA	+/- (1% of rdg. + 2 digits)	1 dgt = 10.24nA 1 dgt = 51.07nA 1 dgt = 251.4nA 1 dgt = 1.451µA

4.3. Control

4.3.1. Microprocessor

AT89C2051 microprocessor is used as the channel controller. It runs a control programme loaded into processor's 2kB flush program memory. Main functions of this programme are:

- load DAC with the setting for the required value of the bias voltage,
- read the output bias voltage and compare with the required value,
- read the output current and compare with the preset trip limit,
- react to interrupts from the card controller which may inquest the channel status information, voltage and current readings and/or change the channel settings,
- self-consistency and calibration tests.

The channel microcontroller is "passive" in communication with the card controller. It runs its endless lowest layer channel control programme and communicates with the higher system layer only when such contact is initiated by the card controller.

4.3.2. Control Circuit

Control circuit fulfills all control functions in the channel. Adjusts the voltage on the base of a serial regulator, cuts-off the serial regulator in case of the over-current or over-voltage.

4.3.3. Card Controller

AT80C52 microprocessor is used as the card controller. The main functions of this system layer are:

- pass the new channel parameters (nominal voltage setting, over current trip limit, ramp-up and ramp-down rates) to the channel controller,
- query the channel state,
- query channel controllers for the measurement of the current bias voltage and current,
- various diagnostic and consistency tests.

The card micro-controller is "passive" in communication with the crate controller. It runs its endless card control programme and communicates with the higher system layer only when such contact is initiated by the crate controller.

4.3.4. Crate controller

The crate controller based on SAB80C517N processor communicates with DCS host computer via CANbus interface (open CANbus protocol). It communicates with LV and HV card controllers via parallell interface with custom defined protocol and data, address and control lines included in the backplane wiring. It sends voltage settings and ramping parameters to card microcontrollers and receives data on voltages and currents and also card microcontroller and channel status words. It stores the last

settings and the last received data and status. Controller will include battery backup so that it can communicate with DCS computer in case of power failure.

Physicaly, the connector for CANbus comunication with DCS will be placed at the front panel of the crate controller.

4.3.5. Addressing

The addresses of HV and LV cards are defined by the crate slots and compared with higher bits of addreses received from the crate controller.

4.3.6. Cable connection

Eight connectors for conventional cables are placed on the backplane and situated in columns between LV and HV cards. Wire lines on the backplane connect LV and HV cards to the cable connectors. Cables come out to the back and then down along the walls of the rack

4.3.7. Front panel lights

For every HV channel:

- Green light if ON (even if 0V is set at the output)
- Red light if OFF (channel cut off by card controller or any interlock)

4.4. Interlocks

4.4.1. Hardwired interlock

The interlock signals shall be TTL levels with active (HV channel OFF) = low and inactive (HV channel ON) =high. Each HV card is connected to hardwired interlock bus distributed through the crate backplane. There is one slot in the crate providing connection to the external hardwired interlock bus (not yet specified in details).

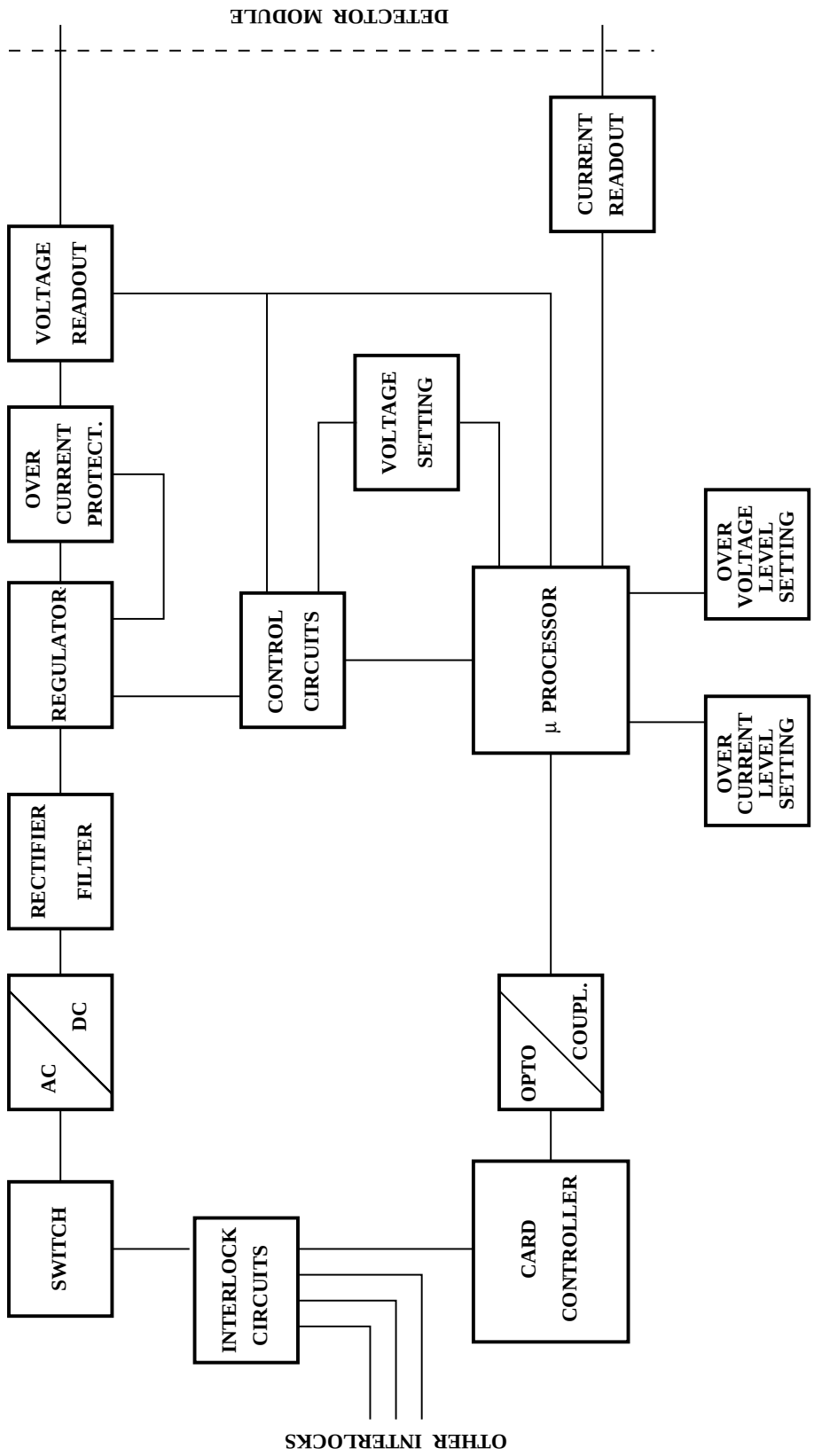

Figure 1: Block Diagram of HV Channel