Project Specification
Project Name: ATLAS SCT Low Voltage Power Supply
Version: V2.2

Project History

Version	Description	Date
1.0	Analog Voltage, Digital Voltage, PIN voltage, Two RETURNS	1996 SCT Munich meet.
1.1	VI1 control voltage, remote sensing, two control lines, Iddmax=240mA, output power 6.4W/channel	March 97
1.2	New VCSEL0 and VCSEL1 control voltages, Three RETURNS	Sep 97
1.3	Increase of digital current from 240mA to ~800mA,	Sep 98-May 99
1.4	Increase of the analog and digital output voltages from 6.0V to 9.5V, output power 22.5W/channel	June 99
2.0	LV card/4 channels, common HV&LV special crate, crate controller, CAN bus interface to DCS Detector temperature readout with two current sources	June 2000
2.1	ABCD3T: Increase of the analog current from 0.98A to 1.3A,	Sep 2000
2.2	Temperature readout of two thermistors, VCSEL hardwired interlock	Feb 2001

Reference

Version   Draft 2.2
Created on   December 5, 1999
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1. Scope

This document describes the requirements and target design specifications for the **L**ow **V**oltage **P**ower **S**upply **S**ystem (LV PSS) providing a set of voltages and logical signals for on-detector readout electronics of SCT modules. This document is closely related to the HV Power Supply System Specifications and the common HV&LV crate specifications which are described in separate documents.

Following the "groundless" scheme adopted by the ATLAS SCT, the modularity of LV Power Supplies corresponds with the structure of the detector. Thus, 4088 individual fully floating LV Power Modules and power tapes serve the Barrel and the End Cap detector modules.

Detector Control System controls and monitors the set of voltages, currents and logical signals of LV PSS. Due to safety reasons, the power supplies are wire-linked to another SCT control systems to ensure the interlock of a part of or the whole LV PSS.

The requirements to the LV PSS are determined by the specifications for front -end electronics, on-detector opto-packages, power tapes and routing of services which are at present time still under development. In the specifications written below, where appropriate, we include parallel specifications covering the different technologies. In a later version of this document we will then delete the irrelevant discussions.

2. Reference Documents

The Silicon Strip Detector Power Supplies and Distribution Requirements Document. Draft 1.1, 10th December 1996

Inner Detector Technical Design Report, Volume 2. CERN/LHCC/97-17, 30th April 1997

Project Specification for ATLAS Binary Chip (ABC). Version 5.01, 21st July 1999

Project Specification for CAFÉ-P. Version 4.01, 13th January 1999

Project Specification for ABCD3T ASIC. Version 1.2, 24th July 2000

Project Specification for VDC (Links VCSEL driver chip). Version 1.0, RAL221

Project Specification for DORIC4. Version 1.02, RAL220

The Semiconductor Tracker DCS Requirements Document. Version 1.4, ATL-IS-ES-0011, 8th April 1999

ATLAS SCT/Pixel Grounding Shielding Note. 22nd November 1999

3. Requirements

The multi-channel LV PSS has modular structure. The LV power supply module is designed as a multi-voltage supply for the FE on-detector electronics and opto-packages providing the set of five different voltages for 12 chips ABCD3T (analog voltage for amplifier/discriminator and digital voltage for the pipeline), DORIC4 chip (FE clock and L1 trigger) and VDC chip (a dual VCSEL driver circuit), VCSEL control voltages and the bias voltage for PIN photo-diode. In addition, two digital signal lines RESET and clock SELECT and four sense wire-lines for the remote sensing of the analog and the digital voltages on the detector module are required. Each LV Power Module will also contain the detector temperature readout with two independent current sources. Nominal voltages and currents are specified in Table 1. The voltage setting and monitoring resolutions and other required basic parameter values are summarized in Table 2.

Table 1

Voltage Name	Electronic circuit	Nominal voltage [V]	Nominal/Maximum current [mA]
Analog Vcc	ABCD3T	3.5 +/-0.2	900/1300 per 12 chips
Digital Vdd	ABCD3T DORIC4 VDC	4.0 +/-0.2 4.0 +/-0.2 4.0 +/-0.2	472/840 per 12 chips 75/106 24/54
VCSEL0 Contr. Voltage	VDC	1.6-6.6	3.5/5.3
VCSEL1 Contr. Voltage	VDC	1.6-6.6	3.5/5.3
PIN Bias	Photo-diode	10.0	0.5/1.1
RESET	HIGH/LOW Negative logic	Vdd/-0.7V	-0.4/-0.42 per module
SELECT	HIGH/LOW	Vdd/-0.7V	1.3/1.4 per module
Current source 0	NTC thermistor	Vmax=8V	80µA
Current source 1	NTC thermistor	Vmax=8V	80µA

Note: The necessary margin on irradiation and occupancy of ABCD3T: Icc=?%, Idd=?%, Vcc, Vdd

Table 2

Voltage	Analog Vcc	Digital Vdd	VCSEL0/1	PIN Bias
Remote sensing control	Yes	Yes	No	No
Monitoring	V/I	V/I	V	V/I
Programmable current limit	Yes	Yes	No	Yes
Setting/Monitoring resolution	1% of max	1% of max	1% of max	1% of max
Power Return Line	AG	DG	DG	DG

4. Specification of Deliverables

4.1 General structure

LV power card is the basic unit of LV PSS and is designed as 6U Europe-standard card for 19" Euro crate. Power card provides four fully floating multi-voltage power modules supplying four SCT detector modules. There are 18 cards, 12 LV cards and 6 HV cards in the crate providing power for 48 detector modules.

The crate controller, common for LV and HV power supplies, provides communication through CAN bus interface with DCS and through the crate bus, it communicates with the master card controllers located on each board. Each LV power module is equipped with two micro-controllers which operate the analog and digital parts of power supplies and communicate with the card controller.

4.2 LV Power Module

4.2.1 Electrical Specifications

The LV power module consists of two fully separated floating and multi-voltage supplies, one for analog and another for digital voltages. Both supplies are insulated from ground, i.e. from the crate power supply by HF transformers and from the card controller, by a communication transformer. The analog and digital supplies are controlled individually by own micro-controllers which communicate with the card controller.
The micro-controller (80C552) controls the switching regulator (IRF9Z34) for the main voltage and linear regulators (TLC472) for control voltages. The switching frequency of the regulator is 100kHz.
Each sub-channel contains the LC filters for depression of the output ripple and the common mode noise.
Individual on-detector loads are powered by separate wire lines (positive) for each voltage and two returns (one for analog and another for digital voltages). Each voltage channel contains hardware protection against over-current and over-voltage events.
 Block diagram of LV power module is shown in Fig.1.

The specifications for the output voltages at power supply have been estimated for the maximum currents of $I_{cc}=1.3A$ and $I_{dd}=1.0A$ and for a present design of the low mass tapes and conventional cables and supposing that the location of power supplies will be in USA15 cavern. The basic characteristics of LV power module are summarized in Table3 and Table 4.

Table 3

Voltage	Analog Vcc	Digital Vdd	VCSEL0/1 Control voltages	PIN Bias
Nominal voltage at hybrid	3.325-3.675 V	3.8-4.2 V	1.6-6.6 V	10.0 V
Maximum voltage at PS	9.0V	9.0 V	9.6 V	13.0 V
Allowable noise level *)	5mVpp	5mVpp	6mVpp	6mVpp
Noise frequency range	0-2MHz	0-2MHz	0-2MHz	0-2MHz
Ripple level	5mV	5mV	7mV	7mV
HW over-voltage trip/limit	Trip (8.9+/-0.1) V	Trip (8.9+/-0.1)V	Limit (9.6+/-0.1) V	Limit (13.0+/-0.1)V
HW over-voltage trip reaction time	100μs	100μs	-	-
Nominal/Maximum current	0.90/1.30 A	0.542/1.00A	3.5/5.3 mA	0.5/1.1 mA
HW over-current trip/limit	Trip (1.30+/-.05)A	Trip (1.00+/.05)A	Limit (8+/-1) mA	Limit (1.5+/-.1) mA
HW over-current trip reaction time	2ms	2ms	-	-
Programmable current limit range	0.5-1.30 A	0.5-1.0 A	-	0.6-1.5mA
Programmable over-current reaction time range, same for all voltages	2ms-510ms	Step 2ms		
Setting/Monitoring resolution	10mV/6.25mA	10mV/6.25mA	40mV/0.1mA	40mV
Voltage start/stop ramping and adjustment reaction time	5-10ms	5-10ms	5-10ms	5-10ms
Hardwired Interlock reaction time with the modularity of four SCT modules	0.1ms	0.1ms	0.1ms	0.1ms
Hardwired VCSEL Interlock reaction time with the modularity of one crate**)	-	-	0.1ms	-
DCS interlock reaction time; modularity is one SCT module	2ms	2ms	2ms	2ms
HIGH/LOW levels for RESET and clock SELECT		Vdd/-0.7V		
Power Return Line	AG	DG	DG	DG

*) It is supposed that the Ferrite Common-mode Chokes will be used at the end of conventional cables at PP3 for all voltages as well as at the output of PS.

**) Both VCSELs control voltages are set to zero and other voltages of the module are ON.

Table 4

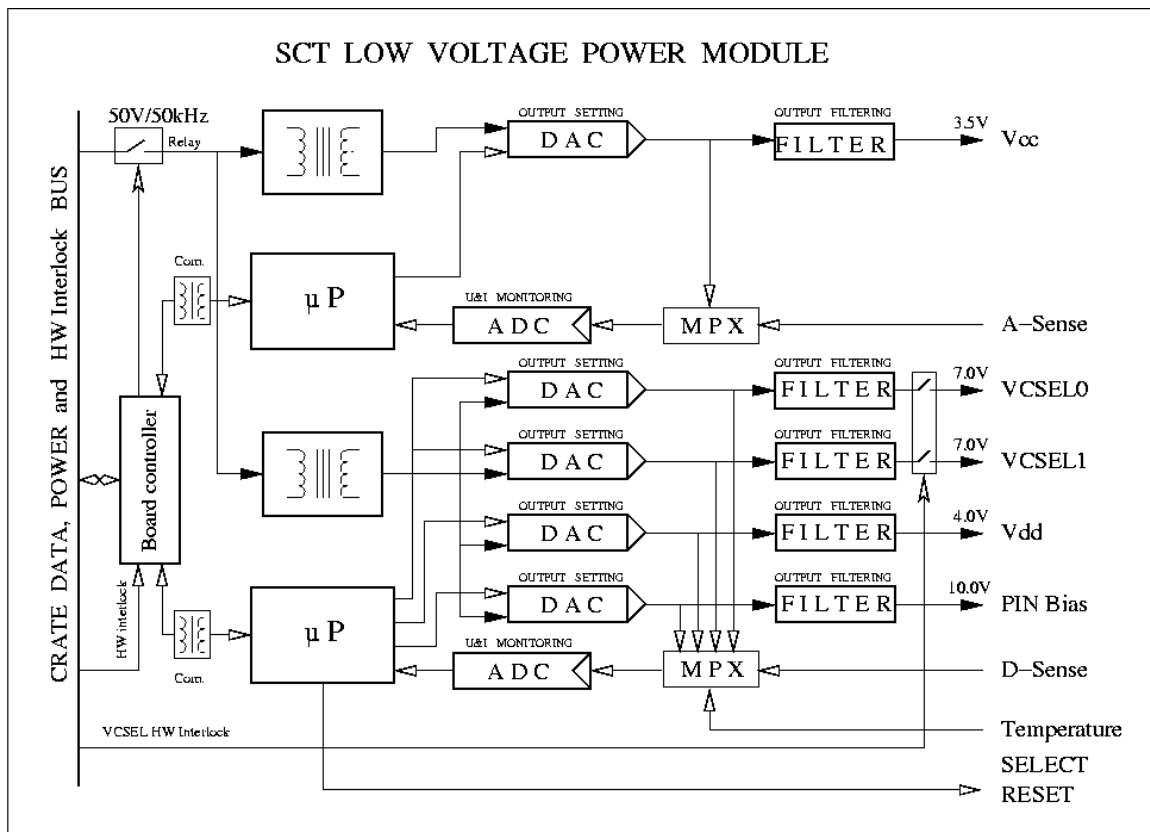| Control Signal	High/Low Level	Min/Max Load / Terminating	Min/Max Rise-time	Min/Max Fall-time	Min/Max Duration
SELECT	DG/Vdd sense potential	200Ω /3kΩ&0.5μF pull-down	0/1 ms	0/1 ms	DC level
RESET	Vdd/DG sense potential	200Ω /10kΩ&0.5μF pull-up	80/120μs	80/120μs	10/20μs

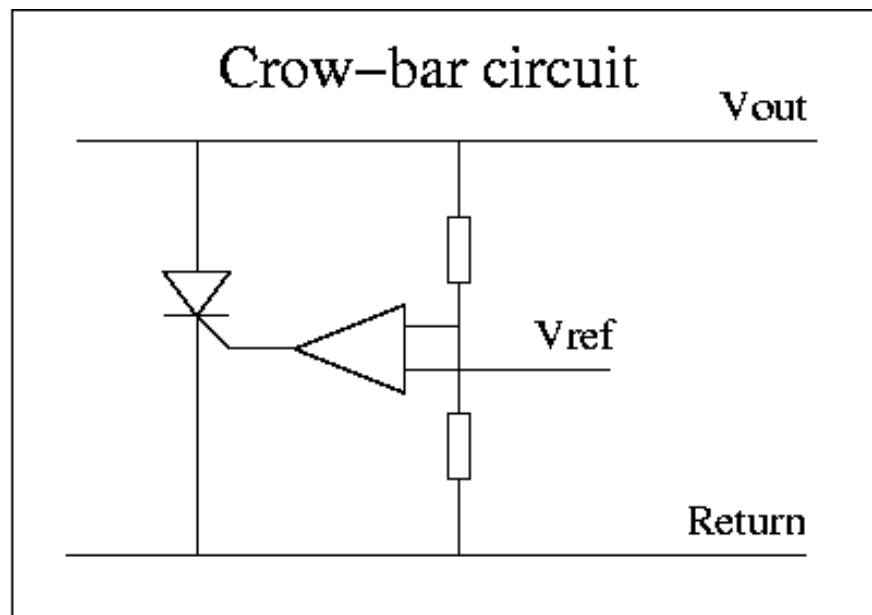## SCT LOW VOLTAGE POWER MODULE

Fig.1

Fig.2

4.2.2 Hardware and Software protection

Each voltage channel contains the hardware protection which limits a maximum output current. Respective limits are given in Table 3.
There is a hardware over-current trip for analog and digital voltages. If the current exceeds this value the voltage is automatically reduced. In such a case, the software will trip LV power module within 2ms.

The analog and digital voltages are protected by the hardware "crow-bar" against an over-voltage with the 100μs trip reaction time. Hardware logic will trip LV power module (see Fig.2)

The VCSEL0/1 control voltages, PIN bias and logical signals RESET and clock SELECT are limited by hardware to values given in Table 3 and Table 4.

The current limits are programmable for all voltages with the exception of PIN bias.
The programmable over-current trip reaction time in the range 2ms - 510ms with the 2ms setting resolution is the same for all channels.

4.2.3 Remote sensing

The analog and the digital voltages at hybrid are controlled by two pairs of sense wires.

In the case of disconnection of any sense wire, the voltage values on the hybrid may not change more than on +/-5% of the previous value. Any disconnection of a sense wire is monitored and there are two options for this case which are selectable by program:

1. LV power module will be turned OFF.

2. The output voltage will be adjusted by LV card controller by using the monitored values of respective current and programmable resistance of the power line.

4.2.4 Detector temperature readout

There are two current sources on each LV power module for two temperature sensors, NTC thermistor with R0=10kΩ at 25°C, B=3435K, placed on SCT detector module: Inom=80uA,Vmax=8V.
Temperature readout is performed by 10-bit/5mV ADC in the range from -15 to 50°C with resolution 1°C.
The LV unit will monitor the detector module temperature also before powering this module (LV module is ON but Vcc=Vdd=0V).
Temperature limit for over-temperature trip is programmable.

4.2.5 Control functions

Micro-controllers of the analog and the digital parts of the LV power module run control a program and they are passive in communication with the card controller. They provide following control functions:

Logical status: ON/OFF/TRIP/INTERLOCK

          TRIP: over-voltage, over-current, over-temperature of the detector module
          INTERLOCK: sent by DCS
                    VCSEL hard-wired interlock

Warning messages: Any sense wire is disconnected.
                    Any temperature sense wire or thermistor is broken

Setting of desirable voltages and the current limits as given in Table 2

Monitoring of present voltages and currents as given in Table 2 is done regularly each ~2ms, values are stored in respective controller memory and they are available by the card controller.

4.2.6 Conventional cable lines

There is one conventional cable for each LV and HV power module. It will contain 17 wire lines and the shielding mesh which are specified in Table 5. The shielding mesh is connected to the crate ground.

Table 5

1	Analog voltage Vcc	11	Analog sense ground
2	Analog ground RETURN1	12	Digital sense positive
3	Digital voltage Vdd	13	Digital sense ground
4	Digital ground RETURN2	14	HV detector bias *)
5	Control VCSEL0 voltage	15	HV bias return *)
6	Control VCSEL1 voltage	16	Temp 0
7	PIN Bias	17	Temp 1
8	Logical signal RESET		Shielding mesh
9	Logical signal clock SELECT		
10	Analog sense positive		

Note: *) These lines are supplied over the crate back plane from the HV PSS card.

4.2.7 Long term stability

The estimated long term stability should be better then 1000 ppm/year. It will be reached by the choice of the voltage reference (TL431) and precise voltage dividers.

4.3 LV Power Supply Card

4.3.1 Description

The LV power card is designed as a 6U four layer PCB having sizes 234x220mm2 (234x280mm2 as a maximum). LV power card consists of four LV power supply modules, the master card controller, a temperature sensor and a hardwired interlock circuit.

4.3.2 Control functions

The card controller communicates with the higher system layer only when such contact is initiated by the crate controller and provides an interface to all power module controllers for control commands:

ON/OFF/INTERLOCK/RESET/MONITORING

Card controller ensures control and monitoring functions:

Logical status: ON/OFF/TRIP/INTERLOCK

TRIPS: SOFTWARE and OVERHEATING of the LV card
INTERLOCK: Hard-wired interlock

When a loss of communication with any power module micro-controller is recognized then the power module is switched off and it is signaled as SOFTWARE TRIP.

Command RESET together with commands to set voltages and current limits must be used after an over-voltage and over-current trips and after the software trip of power module.

Temperature at the card is monitored.

4.3.3 Cable connection

 Connectors CONEC 24W7 for conventional cables are placed on the crate back plane and each four of them are situated in one column between HV and LV cards. Wire lines on the back plane connect LV and HV module through the card connectors to the cable connector.

4.3.4 Powering

AC 50V/2.5A, 50kHz
DC 5V/100mA, 12V/50mA
Cards are supplied by the crate power bus which is located on the back plane via two 96-pin 603-2-IEC-C096 connectors.

4.3.5 Working temperature

Temperature range: 10°-60°C
In the case of over-heating (70°C), a powering of LV card (i.e. of all four LV modules) is turned OFF by hardware logic. Temperature is monitored.

4.3.6 Hardwired interlock

The interlock signals shall be TTL levels with active (LV PSS disabled)= low and inactive (LV PSS enabled) = high. If the high TTL level is missing (connection is broken) then LV PSS will be disabled.
Each LV card is connected to hardwired interlock bus distributed through the crate back plane. There is a one slot PCB in the crate providing conversion between protected RS422 external hardwired interlock inputs and internal TTL interlock bus.
Input connector (25-pin D-SUB male) is mounted on the back plane.
One input for the interlock of all VCSELs in the crate has an extra connector.
SCT hardwired interlock card is described in separate document.

4.3.7 DCS and trip interlocks

Every LV power module will have a bi-directional wire line connection to corresponding HV power module via back plane for sending out and receiving interlocks. Bi-directional line connection ensures that any trip (switching OFF) of either HV or LV module will turn OFF both HV and LV modules.

4.3.8 Addressing

The number of LV card is unambiguously given by a slot position in the crate and defines higher bits of addresses of all four LV modules in a memory of the crate controller (Local Work Station?).

4.3.9 Interface to crate controller

LV card communicates with a crate controller through the crate bus:
1. Protocol for crate bus commands is a subject of other document.
2. Communication is parallel, 1 byte.
3. Electrical signals: TTL
4. Connector: DIN 41612

4.3.10 Front panel signaling

1. Input power ON (green/no light)
2. Output power ON (green/no light)
3. Output power OFF/Interlock (red/no light)

4.3.11 Reliability and maintenance requirements

The equipment is designed for the long term operation. The minimum life time should be 10 years. After this time should be refreshed nonvolatile memories and gauged voltage dividers.

4.3.12 Expected lifetime cost

Here will be 5% spare parts for the replacement. All parts are simply changeable, without special tools. The defective parts will be repaired at the Institute of Physics, Prague AS.

4.4 Common HV&LV crate

4.4.1 Basic characteristics

19" Euro crate of special construction is envisaged for housing of 12 LV cards, 6 HV cards, fast intelligent crate controller and one PCB with hardwired interlock logic.

The crate communication bus protocol and details of construction are described in separate document.

Schematics of slot assignment

HW INTERLOCK	CONTROLLER	LV 1	HV 1	LV 2	LV 3	HV 2	LV 4	LV 5	HV 3	LV 6	LV 7	HV 4	LV 8	LV 9	HV 5	LV 10	LV 11	HV 6	LV 12	EMPTY SLOT

4.4.2 Crate power pack

The crate power pack provides DC and AC voltages for the crate back plane.
Power input is 3x400V/230V, 3 x 3.2A, 50Hz and outputs are +5V for logic, +12V for relays control and 50V, 48kHz for channels AC/DC converter. Total input power is 2.2kW maximum. The crate controller monitors output power and working temperature of the power pack. In case of an external main interruption, the crate will turn to a trip state. Working temperature: 10 to 60°C, trip at 70°C.
SCT crate power pack is described in separate document.

4.4.3 Crate controller

The crate controller communicates with DCS through CAN bus protocol and control LV and HV power modules. It stores a set of last monitored values from power modules, temperature sensors at cards, temperature sensor and output power of the crate power supplies. Controller will include battery backup so that it can communicate with DCS (Local Work Station) at all times.
Local Work Station will provide short term statistics of monitored values for diagnostic purposes.

Physically, the connector for CAN bus communication with DCS will be placed at a front panel of the crate controller.

Control functions:
1. Crate power supply ON/OFF/INTERLOCK(?)

2. Distribution of diagnose and control commands to power cards and modules

3. RESET of the card after hardwired interlock and/or an overheating trip by using last monitored values.

Monitoring:
1. Crate power supply temperature
2. Crate power supply output power

Logical status: ON/OFF/TRIP/INTERLOCK(?)

TRIP: overheating of the crate power supply

The SCT crate controller and communication protocol with DCS are described in separate document.

Note

All electrical components used for construction of LV cards are not qualified as radiation hard or tolerant devices. It is supposed that all power supply crates are situated far from radiation environments reaching total fluences greater than 5.E10 neutrons/cm2 during a 10 year operation of LHC.
Magnetic field greater than several tens of Gauss is dangerous for correct functionality of power supplies.