Specification

Crate Controller

for SCT LV&HV Power Supply System

Functional description

A commercial product miniCON-537 made by Phytec Meßtechnik GmbH based on 8-bit CMOS processor SAB80C517N from the well-known industry standard – 8051 family is used as crate controller. The controller communicates with the DCS host computer via CAN-bus interface (open CAN-bus protocol) and with LV and HV card controllers via parallel interface with custom defined protocol. It receives voltage settings, ramping parameters and current limit settings from the host and transmits them to LV and HV cards. From the cards it receives data on voltages, currents and status words.

It stores the last settings and the last received data and status from each card and channel as well as last monitored values from temperature sensors at LV cards and crate power supplies. The controller will include battery backup so that it can communicate with DCS computer in case of power failure.

The host will provide short term statistics of monitored values for diagnostic purposes.

Technical description of the crate controller.

- Universal Controller Board for SAB80C537/517 controller on 100x160 mm Eurocard
- Up to 64 Kbyte EPROM and 128 Kbyte RAM
- 5 bidirectional ports
- 12 channel A/D converter with 8 bit resolution
- External reference voltage source for A/D converter
- Serial interface of RS232 standard (9-pin D-subminiature connector at the front plate)
- CAN-Bus interface (PCA82C250 bus driver, 9-pin SUB-D male connector according to CiA/DS102-1 at the front plate)
- Backplane connections via 96 pins 603-2-IEC-C096 male connector
- Real-Time Clock and RAM with external battery back-up
- Four Counter/Timer
- Two Controller-Watchdog, one remote controllable
- 14 internal/external interrupt sources with 4 interrupts levels
- Fast arithmetic unit of the controller
- Only one supply voltage of 5 V/150mA

Description of custom defined Crate Interface

1. **Control lines (TTL level):**

   1.1. **D/AD 0 – D/AD7** data/address 8bit bus

   1.2. **$\overline{\text{DS}}$** data strobe (active low)

   1.3. **$\overline{\text{AS}}$** address strobe (active low)

   1.4. **BA0 – BA4** board address defined by position in the crate

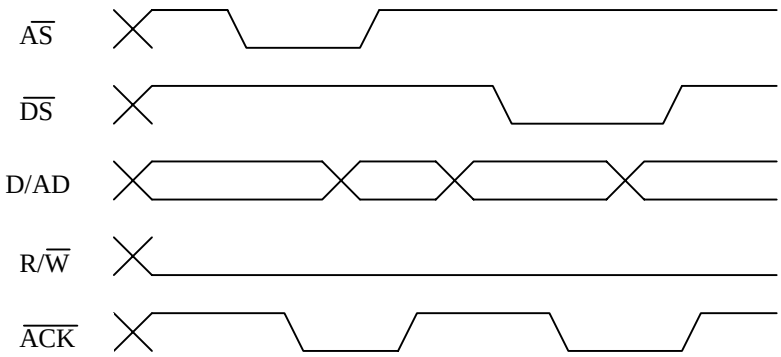
   1.5. **$\overline{\text{ACK}}$** acknowledge (active low)

   1.6. **R/$\overline{\text{W}}$** read = high, write = low

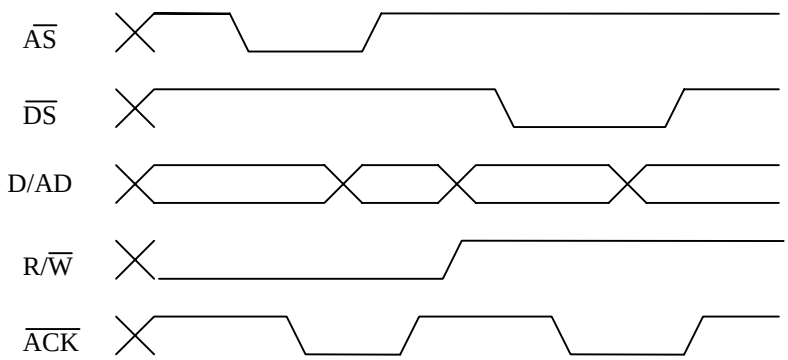
   1.7. **$\overline{\text{IRQ}}$** interrupt request (active low)

   1.8. **$\overline{\text{RESET}}$** controller generated reset

2. **Write cycle:**



3. **Read cycle:**



4. Address byte description

0x00 – 0x11	LV and HV card addresses
0x12	Interlock address
0x13 – 0x1C	not used
0x1D – 0x1F	broadcast type addresses
	0x1D – for LV boards
	0x1E - for HV boards
	0x1F – for all boards