ATLAS Specification
Name: ATLAS SCT L1 Trigger Latency Budget
Version: 1.00

Revision History

Revision	Change Description, Pages Revised	Person Responsible	Date Approved
1.00	Initial version (first drafted by A. Grillo).	J. B. Lane	15-Oct-1999

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1. SCOPE

The purpose of this specification is to identify and tabulate the contributions to the SCT L1 Trigger Latency. This then becomes a Latency Budget, which must not be exceeded in total. Each item in the budget is the responsibility of the group developing that part of the ATLAS trigger chain, which contributes that amount of time to the latency for the SCT. The groups involved have agreed to the items and any change to increase an item must be negotiated to keep the latency total fixed.

2. RELATED PROJECTS AND DOCUMENTS

On the Web via ATLAS -> Inner Detector -> SCT -> Electronics (or Off Detector, or Links):

1) J. B. Lane, SCT latency Web page at http://www.hep.ucl.ac.uk/~jbl/SCT/SCT_latency.html
2) A. Grillo, "Brief Overview of the SCT L1A Latency Budget Issue" (1999).
3) J. Troska, "Fibre routing for SCT Optical Links" (1999).
4) CAFE-P ATLAS-SCT Specification.
5) ABC ATLAS-SCT Specification.
6) ABCD ATLAS-SCT Specification.
7) DORIC ATLAS-SCT Specification.
8) BPM ATLAS-SCT Specification.
9) BOC, ROD and TIM Off-Detector Electronics documents.
10) ATLAS TDR 5, Inner Detector Technical Design Report, Vol. II, CERN/LHCC/97-17 (1997).
11) ATLAS TDR 12, Level-1 Trigger Technical Design Report, CERN/LHCC/98-14 (1998).
12) ATLAS TDR 13, Technical Co-ordination Technical Design Report, CERN/LHCC/99-01 (1999).

3. TECHNICAL ASPECTS

3.1. Requirements

The basic requirement is that the data is still available when the ATLAS Level-1 Accept trigger signal (referred to here as L1A) arrives at the pipeline on the detector. The trigger is delivered from the Central Trigger Processor (CTP) through the Timing, Trigger and Control (TTC) system to the SCT off-detector electronics where it is fanned out and transmitted to the SCT Front-end ICs (Integrated Circuits). The SCT system must take such time that the data from the beam bunch crossing associated with the trigger is at the end of the pipeline of each Front-end IC when the L1A is received at those pipelines.

The L1A will be received by the SCT along with the full TTC protocol at the electronics racks containing the SCT Readout Drivers (RODs) via the TTC-supplied TTCrx chip on a Timing Interface Module (TIM). Each crate of RODs will have a TIM that will distribute the signal via the backplane to the RODs. Each ROD will then pass the signal as an encoded serial bit stream to its Back-of-Crate (BOC) card, which will transmit the trigger via the SCT front-end optical links to all the Front-end ICs. The BOC has the capability to provide programmed delays for each front-end link to guarantee the exact arrival time of the L1A at each SCT module, so that data from the correct bunch crossing will be taken from the pipeline. However, this assumes that there is sufficient margin in the L1A arrival time to allow such synchronization.

The time delay of the trigger in the cables and fibres depends on the distance that the signal must travel, and the uncertainty in the total length is the position of the ROD racks and the routing of the fibre runs. The requirement is that the sum of the three worst-case lengths, from detector module to ROD rack, ROD rack to TTC rack, and TTC rack to CTP rack, does not exceed about 140 metres in total. This is related to the requirement that the SCT Contingency should give a safety factor of at least 4 BCs. These requirements apply to both the Barrel SCT and the Forward SCT. It is also required that the SCT respects the Level-1 Trigger contingency of 20 BCs, of which 2.2 BCs were being used at the time of its Technical Design Report.

3.2. Definition of Terms

Bunch Crossings (BCs): The unit of time between consecutive bunch crossings of the beam in the LHC machine (25 ns) which is also equivalent to the SCT main system clock period.

Pipeline Length: The number of bunch-crossings for which data is stored in the pipeline of the Front-end ICs.

SCT L1A Latency: The total elapsed time from the instant a bunch in each of the LHC rings crosses to interact, to the time that the L1A trigger signal arrives at the on-detector pipeline. It arrives at the latching circuitry at the end of the Front-end IC's pipeline to transfer the data from the pipeline into the readout buffer.

Time Delay: For each component contributing to the latency, the time delay is defined to be leading edge of input signal to leading edge of output signal. For example, the component labeled "ABC or ABCD" measures time from the leading edge of the first bit of the 3-bit L1A command to the leading edge of the internal pulse to transfer data from the pipeline to the output buffer. Any extra delay due to clock synchronization must be included in the component time delay. A ROD crate is essentially a synchronous system and in this case, the leading edge is of the clock validating the signal. The time delay for cable and fibre is 5 ns/metre.

3.3. SCT L1A Latency Budget

The SCT L1A Latency Budget is listed in Table 1. Each component of the budget is listed with its contribution given in units of Bunch Crossings (BCs) and in nanoseconds (ns). Also shown is an ATLAS group responsible for the design of the system that contributes that latency item to the budget. The budget is forced to add up to the exact value of the pipeline length with any extra time allocated to contingency. If any item in the budget must be altered, especially in the case of becoming larger, that change must be balanced by an equal but opposite change in one or more other items so that the total remains equal to the Pipeline Length.

Table 1: SCT L1A Latency Budget (last budget change on 6-Jun-1999)

Component	**Time Delay**		**Responsibility**
	BC	ns	
CTP Output (17.8 BCs contingency)	77.9	1947	ATLAS Level-1 Trigger
Fan-out	0.4	10	ATLAS TTC
Cable: CTP rack to TTC rack (8m)	1.6	40	ATLAS Technical Coordination
TTCvi module	0.1	3	ATLAS TTC
Cable (0.6m)	0.1	3	ATLAS TTC
TTC Crate or TTCvx module	0.9	22	ATLAS TTC
Fibre: TTC rack to ROD rack (32m)	6.4	160	ATLAS Technical Coordination
TTCrx chip	3.0	75	ATLAS TTC
TIM	2.0	50	SCT Off-Detector Electronics
Backplane of ROD crate	0.2	5	SCT Off-Detector Electronics
ROD	3.0	75	SCT Off-Detector Electronics
BOC card	0.5	13	SCT Off-Detector Electronics
BPM chip	2.0	50	SCT Links
Fibre: ROD rack to Detector (97m)	19.4	485	ATLAS Technical Coordination
DORIC	1.0	25	SCT Links
ABC or ABCD	7.0	175	SCT Front-end Electronics
SCT Contingency	6.5	162	SCT Electronics Coordinator
Total (= Pipeline Length)	132.0	3300	