AROW - A 128 Channel Analogue Pipeline with Wilkinson ADC and Sparsification ASIC

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Abstract

A 128 channel ASIC is being designed for the read-out of silicon strip detectors in the LHC ATLAS Experiment at CERN. The chip is based on work already done for the analogue read-out of detectors using pre-amps, shapers and capacitor arrays to form an analogue delay buffer [1,2,3,4]. In addition this chip will have a 128 channel Wilkinson ADC based on the SVX Detector design to digitise all channels in parallel and sparsify the data according to a digitally set threshold [5]. The chip will be fabricated in the AMS 1.2 micron technology by the end of 1995 to prove the architecture before being converted to a Radiation Hardened process.

I. INTRODUCTION

The AROW IC is being developed to meet the requirements for an analogue/digital solution to the read-out of front end silicon strip detectors in the LHC ATLAS experiment. The silicon tracker module will have approximately 3 million detectors and a bunch crossing rate of 40MHz. The front end electronics requirements are to amplify and shape charge generated on the silicon detectors at the bunch crossing rate and to sample and store consecutive data samples for 2.4uS on a capacitor pipeline. A level-1 trigger is sent to the front end electronics from the trigger processor to indicate that the data for a particular bunch crossing is part of an event required to be read off detector. The corresponding data samples are to be digitised for all detector channels and the data sparsified according to a digitally set threshold. This sparsified data is then to be output off the front end detector module to a data acquisition system.

The current proposal for the ATLAS Digital Scheme front end module is to have 8 groups of 128 channels of data processing electronics on a hybrid forming two data output daisy chains of 4 groups each, with one daisy chain on each side of the hybrid.

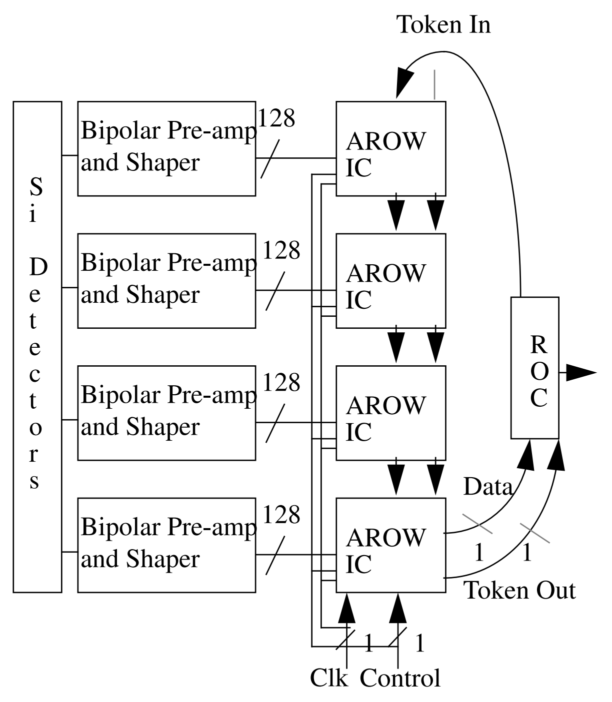

Fig.1 One Side of Hybrid - Bypassing not Shown

Silicon detector charge is to be amplified and converted to a current pulse by the bipolar CAFE chip [6]. The aim of the AROW chip is to incorporate at the front end low noise signal amplification and storage for accurate particle tracking with fast digitisation and data sparsification for reduced data transfer off detector. An 8 MIP (~22,000 e/MIP) dynamic range is required with 7 bit resolution. Read-out of the AROW data and its transfer off detector is autonomously controlled by a ROC chip. Figure 1 shows the general architecture. A bypassing scheme will be used to route data around a malfunctioning chip by sending commands to its neighbouring IC's. Read-out is initiated by a token from the ROC to the first IC. Data is output to the ROC through the remaining IC's. The token is clocked through the remaining IC's and eventually back to the ROC.

II. FEATURES

The following is a summary of the features of the AROW chip.

•Current to voltage converter front-end. The gain of the CAFE chip is ~ 2.5uA/fC, giving a combined gain of approximately 100mV/MIP.

•Analogue storage capacitor pipeline with differential read-out. Uses optional dummy channel as reference level to reject common mode.

•Input data is stored with a 25nS sample period. Level-1 Trigger allows selection of stored data to be read out with Programmable Trigger Latency up to 2.4uS (with column masking disabled this increases to 2.7uS). There must be >2 bunch crossings between triggers. Up to 16 L-1's can be stored at any one time. Requires 128 cell pipeline (16 for buffer storage, 12 for column mask (optional), four for L1 decode delay and 96 for data buffer).

•Column to Column Pedestal Subtraction (optional procedure allowing evaluation of method).

•Programmable Channel to Channel Offset removal, for channel offset normalisation.

•Bad Analogue Pipeline Column Masking (max 12 columns)

•Bad Channel Masking.

•Digitizes data stored on analogue pipeline to 7 bits.

•Digitisation Time < 2.5uSec.

•Dynamic Range of 8 MIP's (<=>8 x 100mV @ pipeline output, dependant on bipolar front end chip etc.).

•Externally Adjustable Range ADC for normal signal and noise measuring. Includes adjustable reference voltage.

•~1/16MIP (~6.25mV) ADC Resolution in normal range

•Digitally set threshold for sparsification. Resolution of Threshold Setting is 1 LSB of ADC resolution (~6.25mV)

•O/P Data Buffer to allow concurrent digitisation & read out. Read-out time is dependent on occupancy.

•Multiple IC's can be daisy-chained for data output. Read-out of each IC is controlled by a token generated by a ROC and then passed chip to chip. Programmable chip bypassing by having normal and bypass data paths per chip.

•There are three alternative criteria for selecting data for output during sparsification. *Overthreshold* requests only data above the programmed threshold is to be output. *Neighbours* requests all Overthreshold Data plus their nearest channel neighbours is to be output. *All* requests that the digitised data for all channels is to be output. Reading neighbour channels between IC's is not available.

•On chip programmable current and voltage bias generator to alleviate need for external biasing.

•Pin Programmable chip ID - 4bits.

•Provides chip/channel ID + ADC value as output data.

•Two modes of operation: Initialisation and Normal Data Acquisition.

•When internal L1 buffer overflows continuous error data is output until next reset. (Depending on timescales an overflow recovery circuit may be included, requiring no resets for continuous operation).

•Capable of producing calibration pulses to the CAFE IC on command.

•On chip test features:
Test buffers on one channel to allow signal measurement, Generate ID command - outputs TBD status packet (e.g. readback of programmable registers). Functional test features to allow rapid production line testing (test signal injection at frontend, spypads).

•50um Channel to Channel pitch - 128 channels

•Separate 0V,4V power supplies for digital and analogue. Separate analogue 2 V reference. The power consumption is predicted to be less than 1mW/channel.

The chip is to be initialised and controlled (including sending level 1 triggers) via a clock and a control input. A well defined protocol has been developed which allows control of the AROW and other IC's that share the same control lines. The control protocol is made up of fast and slow commands. The following list is a summary of the control commands available

Fast Commands:
- Send L1 trigger
- Soft reset
- Send bipolar chip calibration pulse

Slow Commands:
- Hard reset
- Generate I.D. - returns IC status information
- Chip initialisation
- Set internal bias lines
- Set trigger latency
- Set sparsification threshold
- Select test output signals

Read-out of the AROW chip is initiated when it receives a read-out token. In the system sequencing of the read-out token is performed autonomously by the ROC. The following protocol has been developed for the read-out of data from the AROW IC.

The ROC will have the following data output format:

<Preamble><Header><Data><Trailer>

The <Preamble>,<Header> and <Trailer> will be generated by the ROC. <Data> is transmitted from the AROW IC upon receipt of a read-out token.

The release of the read-out token will be correctly sequenced such that the data that is output from the AROW IC will concatenate correctly with the ROC data output format defined above.

There are four <Data> formats that the AROW IC can produce. The first is normal digitised data for a level-1 triggered event. Error data is generated for two cases. When the buffer overflows an error data sequence will be output every time a read-out token is received until reset. Also when the IC receives a read-out token yet there is no data available for output an error data sequence is output. When the generate ID command is received a yet to be defined data packet of implementation specific status data will be output on receipt of the next read-out token.

<NormalData>:
M * (N* (<01><IC/ChanAddr><1><P.H.><1><P.H.><1><P.H.>))

<Buffer Overflow Error Data>: <00><1><Chip ID><Err Code1><1>

<L1 Not Present Error Data>: <00><1><Chip ID><Err Code2><1>

<Generate ID Data>: To be defined

where:

M = Number of chips in a read-out chain. (normally 4)

N = Number of Nearest Neighbour groups (or single channel hits).

IC/Chan Addr - 11 bits

P.H. = 7 bits of digitised pulse height data

Chip ID = 4 bits

Err Code1: “000”: 3 bits

Err Code2: “101”: 3 Bits

III. Circuit Description

The chip will consist of 128 channels of analogue storage, processing and digitisation with some common control and read-out circuitry. A dummy 129th channel is implemented to provide a DC reference for optional common mode rejection features. Figure 2 shows a high level block diagram representation of a channel plus the common circuitry. The following paragraphs give an overview of the circuits operation.

The current output from the bipolar front end will be converted to a voltage. The proposed circuit is a direct current to voltage converter in CMOS, which translates the current waveform from the bipolar chip to a voltage waveform with the same timing characteristics, i.e. a gaussian shape with approximately 25ns rise and fall time.

The voltage levels from the front end are written at 25nS intervals to a 128 stage capacitor pipeline. These stored values will either be cyclically overwritten by new values or if tagged by a level-1 trigger they will be stored until requested for digitisation and read-out. Read-out is performed differentially with either an internally generated reference or a reference taken from the output of a dummy channel. This will be programmable. Column to column pedestal removal will be attempted by initially sampling the output of the storage capacitor after a signal has been written, then writing to the same capacitor but with no signal. In this way any capacitor dependent offsets should be removed. The resulting value is then presented to the input of the ADC. Writing and reading of the storage cells will be controlled by a version of the Pipeline Control Logic (PCL) already validated for the APV5/ADAM chips.

Storage locations that are tagged by a level-1 trigger (in the PCL) are presented to the input of a Wilkinson ADC. This ADC is based on the one developed for the SVXII chip. The digitisation is performed in parallel for all channels with each channel having some of its own ADC circuitry, and with some of the ADC circuitry being common to all channels.

The ADC has an analogue comparator per channel. The signal level to be digitised is applied to one of its inputs while the output of a common ramp generator is applied to the other input. As the ramp generator output is released a counter is set counting upwards. When the ramp generator signal level exceeds the sample level the analogue comparator output switches. This edge (ignoring the delay line for now) is used to load the current counter value into a latch. The magnitude of this latched value is proportional to the magnitude of the sampled value.

Channel dependent offset removal is achieved using a clocked programmable delay line at the output of the analogue comparator. This introduces a variable delay between when the analogue comparator fires and when the counter value is latched. This can subtract offset variations of approximately 1⁄2 MIP.

A digital comparator is used to flag when the counter has exceeded the set digital threshold. When a channel latches the counter value a “data valid” flag is also latched, thus determining if the above threshold condition is met for that channel. When the counter reaches its maximum value all remaining channels are latched regardless of the state of the analogue comparator. When digitisation is complete all the latched counter data is loaded into a shadow register. This allows digitisation to go on concurrently with sparsification and read-out. The sequencing and control required by the ADC and data transfer processes are all implemented on the chip.

The data valid flag is used when sparsifying the channel data according to the Overthreshold/Neighbours/All option set. Read-out involves sending out IC/channel address and data information upon receipt of a read-out token. Essentially a sparsification token (not related to the externally applied read-out token) passing ring is used to search for channels which have their data valid flags set. This information is clocked out in a serial format.

A shift register based circuit is used to deconstruct the command words from the control input pin and set the various options and the threshold etc. This control input decoder will also be responsible for deconstructing the L1 trigger. Depending on the received control code the circuit provides sequencing etc. for the setting of all options and internal registers.

The APV5-BG chip bias generator design is incorporated into this design and is used to provide required reference voltages and bias currents.

The IC is being designed on the AMS 1.2 micron non radiation hard CMOS process. For the digital section both full custom and standard cells are used where appropriate. A provisional floorplan of the AROW chip is given in figure 3.

It is expected that the chip will return from manufacture in the first quarter of 1996, and that a radiation hard version will be submitted in the 3rd quarter of 1996.

IV. CONCLUSIONS

A 128 channel processing chip for the digitised read-out of silicon strip detectors will be submitted for manufacture in the last quarter of 1995. The chip benefits by interfacing with a bipolar pre-amp and shaper chip while providing CMOS analogue data storage for 2.4uS. The chip digitises the 128 channels to 7 bit resolution in less than 2.5uS, and

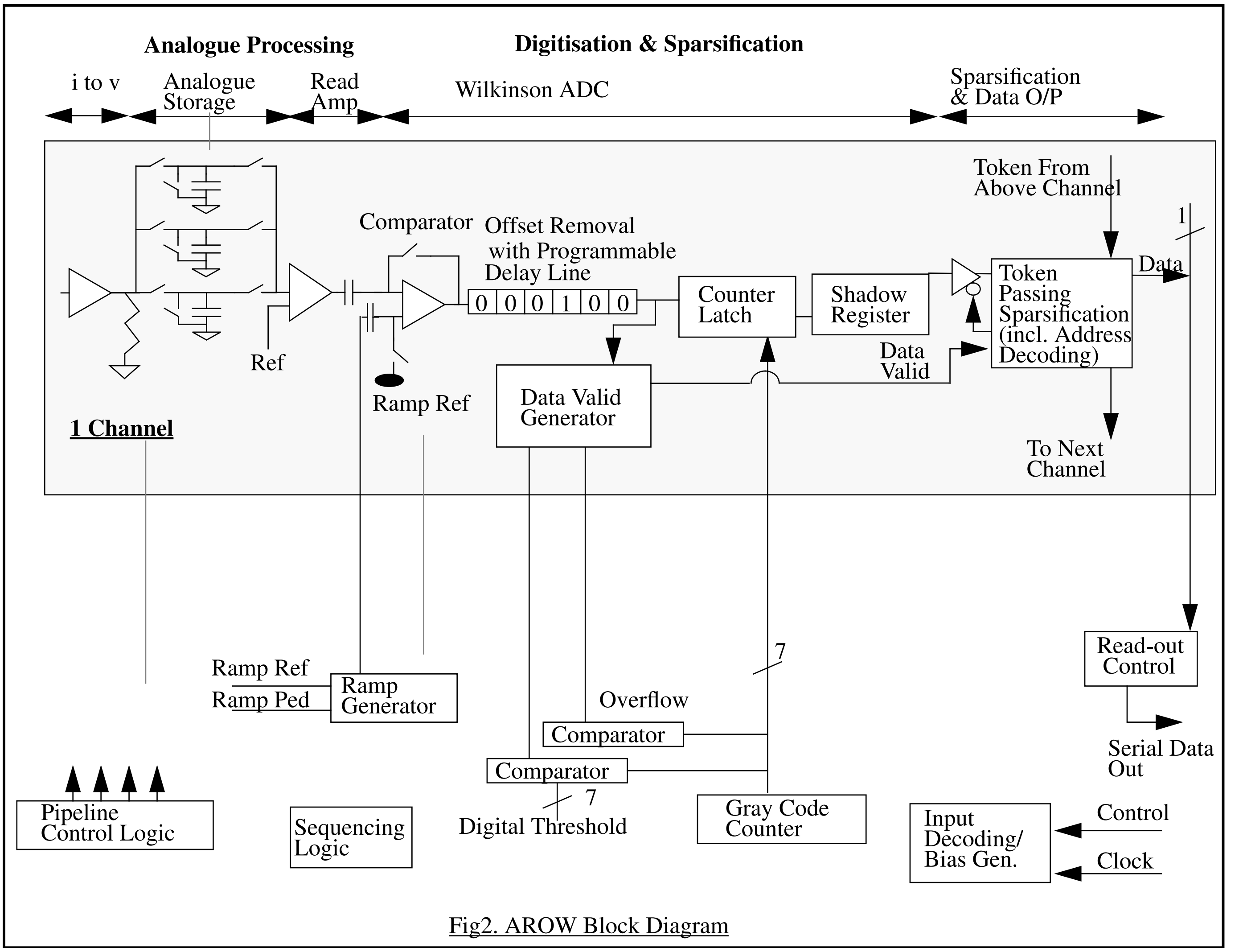

Fig2. AROW Block Diagram

provides on chip data sparsification for reduced data transfer off detector. A complete digital Control and Read-out protocol has been implemented so that the chip can be easily integrated with other ATLAS electronics. It is anticipated that the chip will be submitted for beam tests at CERN in Summer 1996 with a radiation hard version of AROW being submitted in the 3rd quarter of 1996.

V. References

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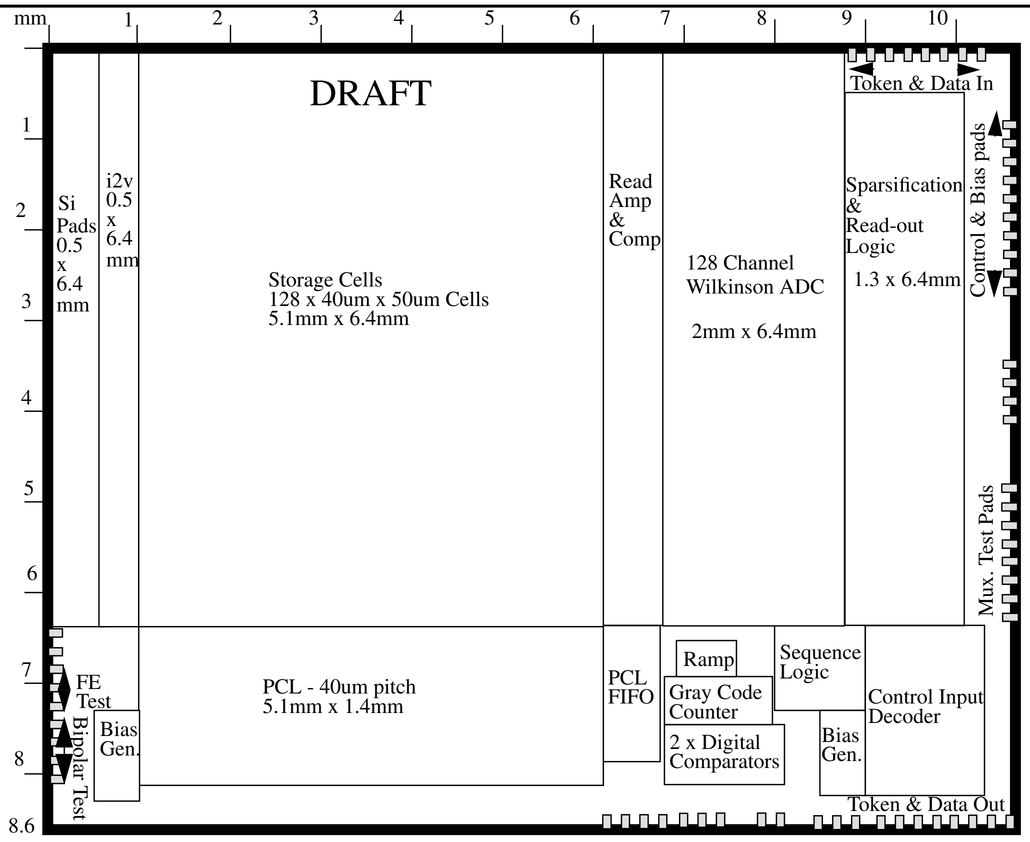

Figure 3. AROW Draft Floorplan