Project Change Order

Serial Number:- 1

Project Name:- RAL220/DORIC4

Description of change:

During test and evaluation of the first few DORIC4s some small problems were found. Making small changes to the design could rectify these problems. These changes will be prototyped on the next AMS MPW run as DORIC4a.

1) The internal delay control range to accommodate component tolerances was found to be too great. Under some conditions the circuit could lock on to half the design frequency. The value of two resistors will be changed to reduce the control range.
2) Input offset threshold was applied to avoid triggering on noise. For low input signal levels this threshold causes timing differences between the two phases of the signal. Timing will be improved by using hysteresis instead of offset.
3) The bias filter resistance will be increased in value from 3k to 6k to improve the effectiveness of the filter.
4) Large metal areas on the layout will be broken up by means of slots or a grid structure for better adhesion to the substrate.
5) The test output pad was found to be rather sensitive to external noise. Resistance in series with this output will be increased in value to minimise noise injection.
6) Current reduction in LVDS output stage. The resistors used to set the pull down current will be increased in value. This reduces current consumption by 2mA per output stage with no loss of performance.
7) Pull down resistors on select inputs will be increased in value from 10k to 20k to minimise loading on the select line drivers.

Customer approval when required (sign, date)

Change implemented. Project Manager (sign, date)

D. J. White 15/04/1999