Project Specification

Project Name: RALxxx / DRX

Version: 1.02

Approval:

	name	signature	date
Project Manager	**D. J. White**		

Distribution for all updates:

Project Manager: D. J. White.
Customer: A. R. Weidberg.
Group Leader responsible for the project: M. J. French.
Project Managers of related projects: M. Goodrick.
Account Manager: W. J. Haynes.

1.0 Scope

To design a data receiver integrated circuit (DRX). This will be initially a 4 channel device which will detect the output of an array of PIN photodiodes receiving signals from a multiple optical fibre link. Signals on the optical fibres will be produced by vertical cavity surface emitting lasers (VCSELs) driven by VCSEL driver chips (VDCs).

2.0 Related projects and documents

ABC (Atlas Binary Chip) Project Specification, D. A. Campbell, RAL.
VDC Project Specification, D. J. White, RAL.
MITEL PIN diode package, description and specifications.
A prototype LED/PIN diode optical data link for the ATLAS semiconductor tracker,
A. Rudge et al, NIM, A 399 (1997) 119-128.
Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI). Draft 1.3 IEEE P1596.3-1995.

3.0 Technical Aspects

3.1 Requirements

3.1.1 General Description

DRX will have initially 4 channels on each chip with good electrical isolation between channels to minimise crosstalk. Each channel will have an input comparator with individual threshold control and an LVDS output driver.

3.1.2 Input Requirements

Inputs will be current signals from the anodes of a common-cathode PIN photodiode array. The signal data format will be non-return-to-zero (NRZ) at 40Mbit/s. Signal currents will range from approximately 500µA maximum at beginning of life with high output VCSELs, good coupling, no irradiation losses in fibre, to 45µA minimum at end of life with low output VCSELs, poor coupling and irradiation losses in fibre. See power budget calculations, Appendix 1. DRX must function with an input signal down to 20µA for extra safety margin. Maximum difference in input levels between channels on a chip 3:1, not the full signal dynamic range. Crosstalk between channels must be very small to keep the bit-error-rate (BER) low. Best efforts, aiming for less than 2% channel-to-channel crosstalk.
Odd and even channel test inputs may be provided to make probe testing easier.
An internal bias filter may be provided if space is available on chip. If the required PIN bias is greater than 10V it must be filtered by external components.
Each channel will have an individual threshold control voltage input, nominally 0 to 2.55V giving an input signal threshold control range from 0 to 255µA, (1µA per LSB if driven by an external 8-bit DAC).

3.1.2 Output Requirements

Output signals to be LVDS compatible. Output jitter <250ps rms at 20μA input, <100ps rms for 45μA or larger input (assuming the signals are stable in amplitude with variation of duty cycle and pulse properties). Variation of propagation delay to be minimised over signal, temperature and nominal supply voltage ranges.

3.1.3 General Requirements

DRX will be required to operate at ambient temperatures from 0°C to 70°C. Supply voltage nominally 3.3V ± 0.3V. DRX must function correctly over the specified temperature and nominal supply voltage ranges and withstand an overvoltage of at least 1V without damage.
All bond pads to be made as well protected against electrostatic discharge (ESD) as possible. It may not be possible to achieve a high degree of protection on all bond pads for reasons of noise or capacitance loading. Careful handling may be needed to prevent damage to sensitive pads during assembly.

3.1.4 Physical Requirements

Signal input pads must be placed suitably for connection to the PIN photodiode array, with total lead length as short as possible. Signal inputs at one end of chip, signal outputs at the other end. Power, bias and threshold control signals along chip edges or at output end. Packaging to be considered, chip-on-board, surface mount, leaded package, ease of wiring, etc. as other details become clearer.

3.2 Specification of deliverables

3.2.1 Functional description and application advice

The PIN photodiode array has common cathodes so the anode signals will go to single ended inputs on DRX. These inputs will be more sensitive than differential inputs so very short input connections must be used. The common cathodes need to be well decoupled to ground close to DRX and series resistance added to filter noise from the photodiode bias supply. An internal filter will have smaller capacitance but may work well for low-noise supplies.
Outputs are low voltage and differential but much larger than inputs so they must be routed well away from inputs.
Treat the devices as ESD sensitive and use appropriate handling procedures until they have been assembled on to the final circuit boards.

3.2.2 Floor plan

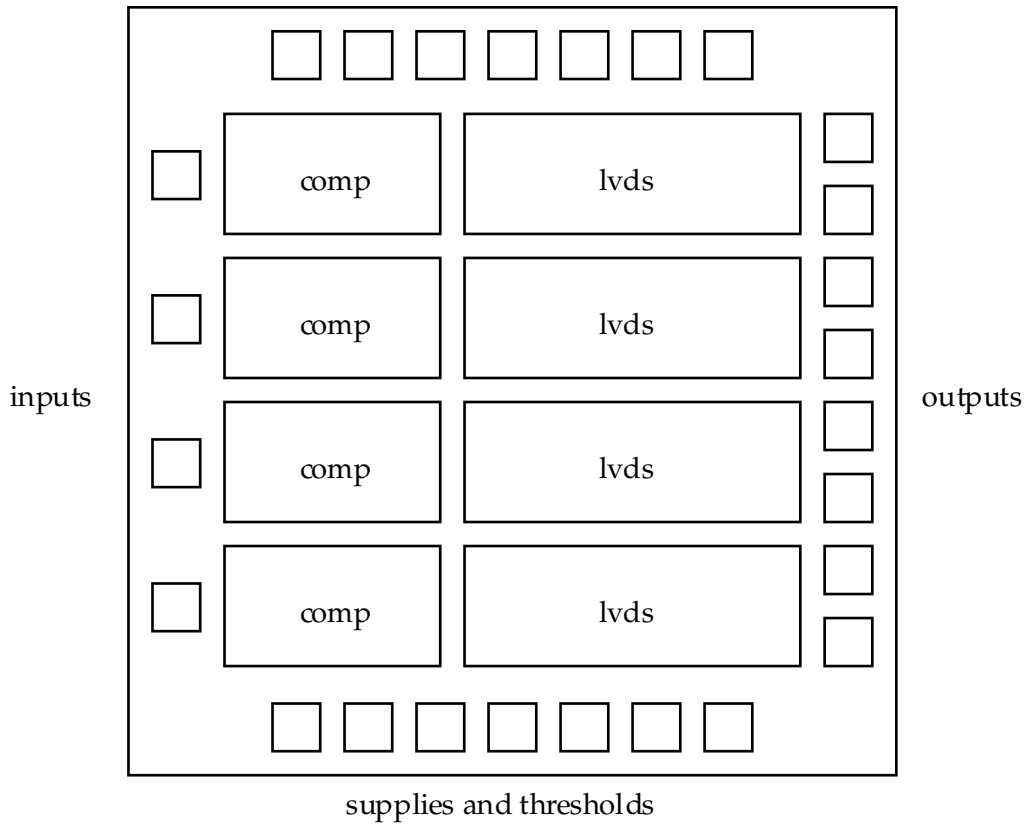

Figure 1. Estimate of floor plan showing pad layout.

3.2.3 Pad Numbering and Names

Pads are numbered in an anticlockwise direction.....

3.3 Manufacturing

The circuitry will be designed using AMS 0.8µm BICMOS models and design rules for fabrication on an AMS MPW run. Submission date ~February 1999.

3.4 Testing and product control

Test requirements will be discussed at IDR. A test plan will be written.
Route Cards will be used to record operations such as probe test, packaging, irradiation etc. and to account for the number of chips used, lost, damaged or shipped at each operation.

3.5 Shipping and installation

The customer will personally collect all of the deliverables.

3.6 Maintenance and further orders

All documentation and test equipment will be kept for a period to be determined at Maintenance Review to facilitate maintenance and further orders.

4.0 Project Management

4.1 Personnel

Project manager:	D. J. White	david.white@rl.ac.uk
Project engineer:	D. J. White	david.white@rl.ac.uk
Engineer:	D. J. White	david.white@rl.ac.uk
Customer:	A. R. Weidberg	t.weidberg1@physics.ox.ac.uk

4.2 Deliverables

Project documentation. Test results. Application notes. Tested and untested die.

4.3 Project plan

Milestones, schedule, see 4.4.
Design and layout will be started after PDR.
AMS 0.8µm BICMOS MPW submission, Feb 1999 (dates to be found for 1999 MPW runs).
Testing to be discussed at IDR, test fixtures to be built for April 1999.
Tested die required for use by June 1999.

4.4 Design Reviews

Preliminary Design Review (PDR) to confirm Project Specification, held 23rd October 1998.
Interim Design Review (IDR) to review project progress and test requirements, November/December 1998.
Final Design Review (FDR) to confirm the devices as designed meet requirements of Project Specification, including any change orders, January 1999.
Concluding Review (CR) and Maintenance Review (MR) after delivery and test.

4.5 Training

Minimal training requirements.

4.6 CAE and test equipment

Workstation, software, support, to suit selected process.
Probe card and test equipment as defined in test plan.

4.7 Costs and finance

Based on previous quotes from AMS, cost for 20 minimum area prototype chips is ~£2400. An extra 80 may be ordered for ~£1500. Packaged chips at extra cost.
Probe card and test components unlikely to cost more than £2k.
All requisitions to be authorised by M Edwards for items on which VAT may be recovered.

4.8 IPR and confidentiality

Technology Department owns the layout and schematic databases. Any masks or phototools will be procured by the Department. None of these items will be released unless the appropriate protective agreements are in place.

4.9 Safety

Low voltage, low power circuitry, no particular hazards associated with this project.

4.10 Environmental impact

Very little from final product. Small amounts of inert substance which may be safely disposed of as landfill.

Appendix 1

Power Budget

Minimum coupled power into 50/125µ fibre for MITEL VCSEL in GEC package = 300µW.

Losses in the transmission are given below:

Effect	Loss (dB)
Operating temperature of VCSEL	-0.8
Attenuation of 90m fibre	0.22
Radiation damage Fujikura fibre	0.2
Radiation damage Plasma fibre	0.3
MT PPB1/PPF1	0.8
MT PPB2/PPF2	3.0
Total attenuation	3.72

Minimum optical signal = 127µW

Minimum PIN responsivity = 0.35 A/W

Minimum signal current = 45µA

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