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Updated Dead Time Calculations for the SCT Binary Readout Architecture

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This note presents results on the calculations of the required size of the overflow counter. and updated results on calculations of the dead time of the Binary readout system as a function of occupancy and buffer depth.

1. Dead Time Results

The dead time versus occupancy for different buffer depths are shown in Figure 1 below for the case of 3 bit "binary" data assuming a Poisson distribution of hits in a chip.

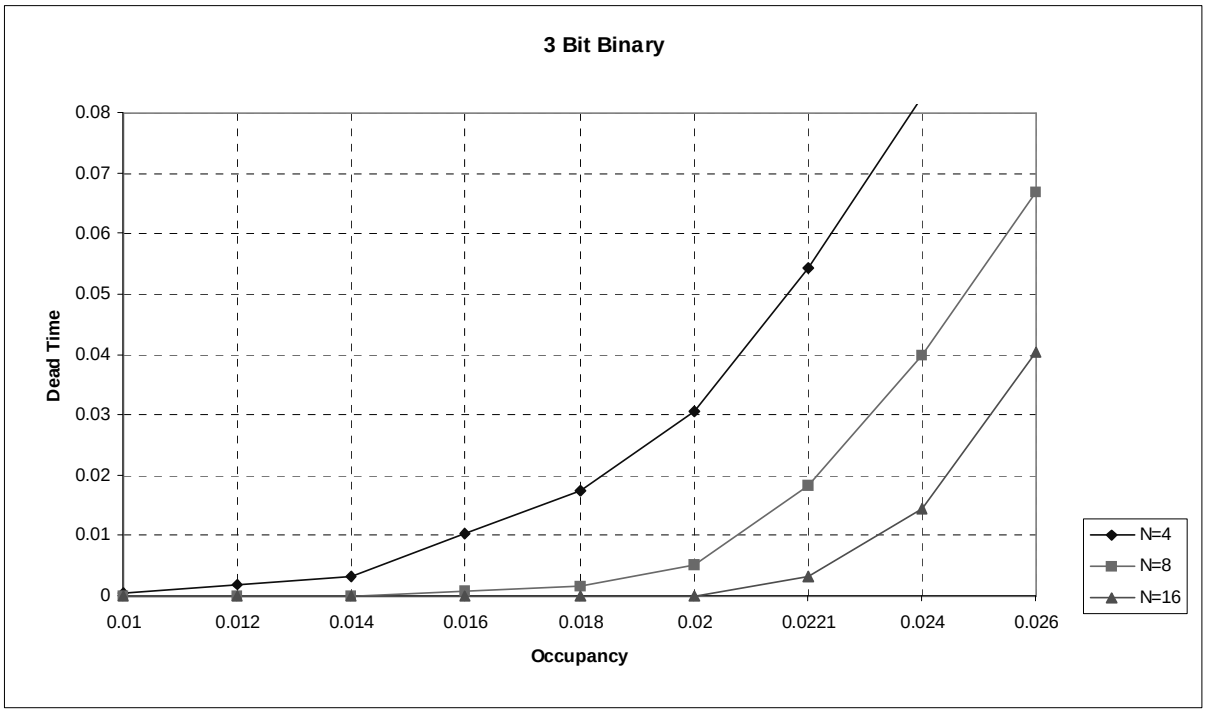

Figure 1 Dead time versus occupancy for 3 bit binary data assuming a Poisson distribution for the hit multiplicity. The curves labelled with different values of N refer to the depth of the derandomising buffer.

The results show larger dead time than those given in ref. [1] due to an improved description of the system. The results for the similar calculation assuming 1 bit "pure binary" data are shown in Figure 2 below. The calculation for 3 bit binary data was repeated assuming a distribution for the number of hits in a chip taken from a GEANT calculation and results are shown in Figure 3 below.

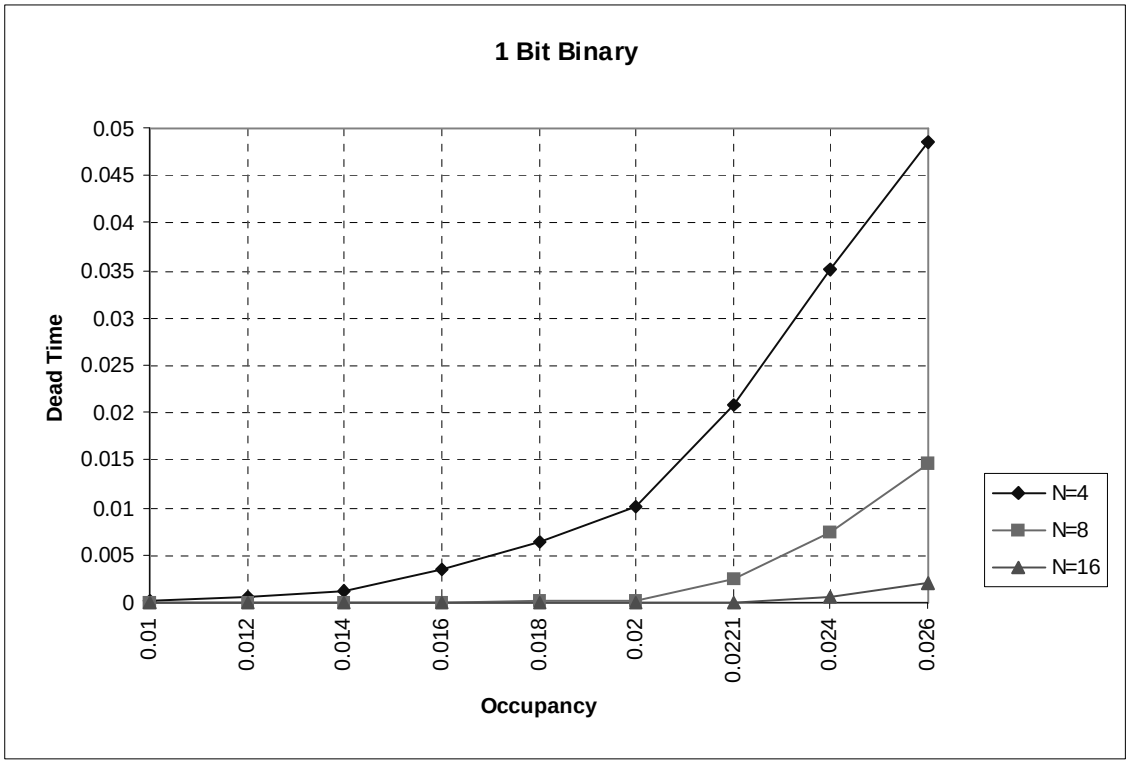

Figure 2 Dead time versus occupancy for 1 bit binary data assuming a Poisson distribution for the hit multiplicity. The curves labelled with different values of N refer to the depth of the derandomising buffer

The results are summarised in Table 1 below where the worst case occupancies for the binary system to maintain a dead time less than 1% are given for the two assumptions about the distribution of hits in a chip.

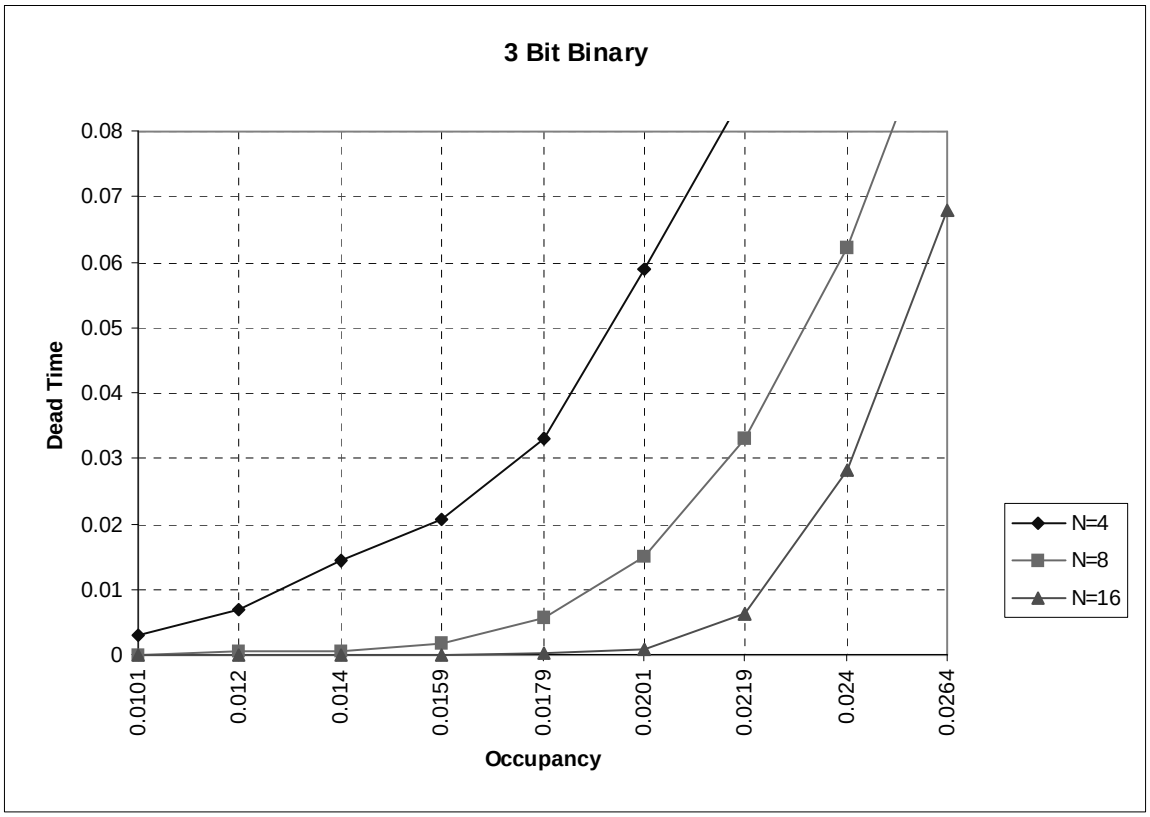

Figure 3 Dead time versus occupancy for 3 bit binary data assuming a hit distribution taken from a GEANT calculation. The curves labelled with different values of N refer to the depth of the derandomising buffer.

Table 1 Strip occupancies (in %) corresponding to a 1% dead time for different buffer depths assuming a mulitplicity distribution from Poisson or GEANT.

Buffer Depth	Poisson	GEANT
4	1.6	1.3
8	2.1	1.9
16	2.3	2.2

2. Overflow Counter Depth

If the derandomising buffer becomes full then dead time will be incurred and there will be a resulting loss of data. When this occurs the data must be flagged as lost for the appropriate events. It is also essential to ensure that the data from a chip can never lose event synchronisation with the rest of the system. In the simplest scheme when the buffer becomes full, the chip sends no further data until a rest is issued (in lieu of the data it sends

an error flag). This is unattractive because it imposes requirements on the reset frequency. The scheme proposed for the binary system is based on the use of an overflow counter. If the buffer is full, when a L1 is received the overflow counter is incremented by one and the new event overwrites the data for the oldest event in the buffer. When an event is read out from the buffer, the overflow counter is decrement by one if it is greater than zero. If the overflow counter is greater than zero when the chip has to read out data, an error flag is transmitted in place of the lost data. If the overflow counter itself overflows then the chip can not process any further data until it receives a reset, in which case it sends error flags until reset in lieu of data.

The predicted count value of the overflow counter is shown in Figure 4 below. The lower value of the occupancy corresponds to a dead time of 1% and the high value to a dead time of abut 5% which can be taken as the highest value of the dead time for which the data would be useful. From these distributions it can be seen that a 4 bit overflow counter will be sufficient.

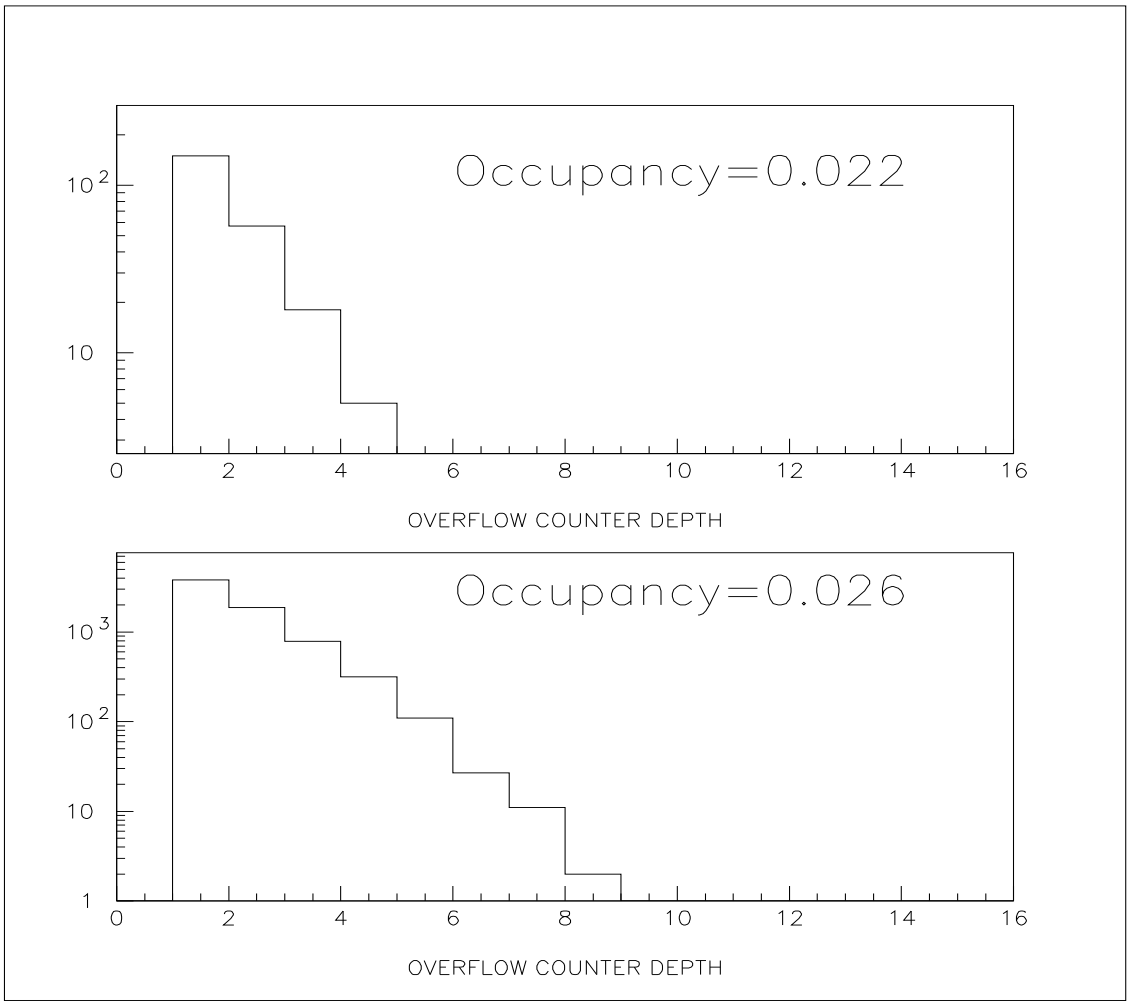

Figure 4 Distribution of the count value for the overflow counter for two different assumed values of the occupancy.

3. Conclusions

The dead time calculations presented in ref.[1] have been repeated with an improved description of the system. Although the predicted dead times are higher than before they are still comfortably within the ATLAS specifications.

The depth of the overflow counter has been studied and it has been shown that a 4 bit counter will be sufficient.

[1] Dead Time Calculations for SCT Readout Architectures, A.R. Weidberg, ATLAS INDET-NO-124