Manual for the BaBar SVT Data Transmission System

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September 15th, 1998
1st DRAFT

1 Introduction

This note provides a brief manual for the SVT Data Transmission System. The Data Transmission System (DAT) comprises essentially all components between the Kapton Tail at the detector front–end to the optical fibers that link the SVT to the DAQ system. A certain familiarity with the DAT system is assumed in this note, for a more general description please refer to [1]. Figure 1 shows a sketch of the whole DAT system plus the HDI and power supplies.

The DAT System consists of the Matching Cards at the detector front–end, the Front Cables that connect the Matching Cards to the MUX Crates, and the HDI Link Cards and DAQ Link Cards that comprise the MUX.

Incidentally, we have a perfect divide-by-two system in the cards count: 2 detector sides (1 HDI) connects to one Matching Card. Two Matching Cards are serviced by one HDI Link Card. Two HDI Link Cards connect via the custom midplane in the MUX crates to one DAQ Link Card. And the DAQ Rom Modules have two optical input/output channels and thus talk to two DAQ Link Cards.

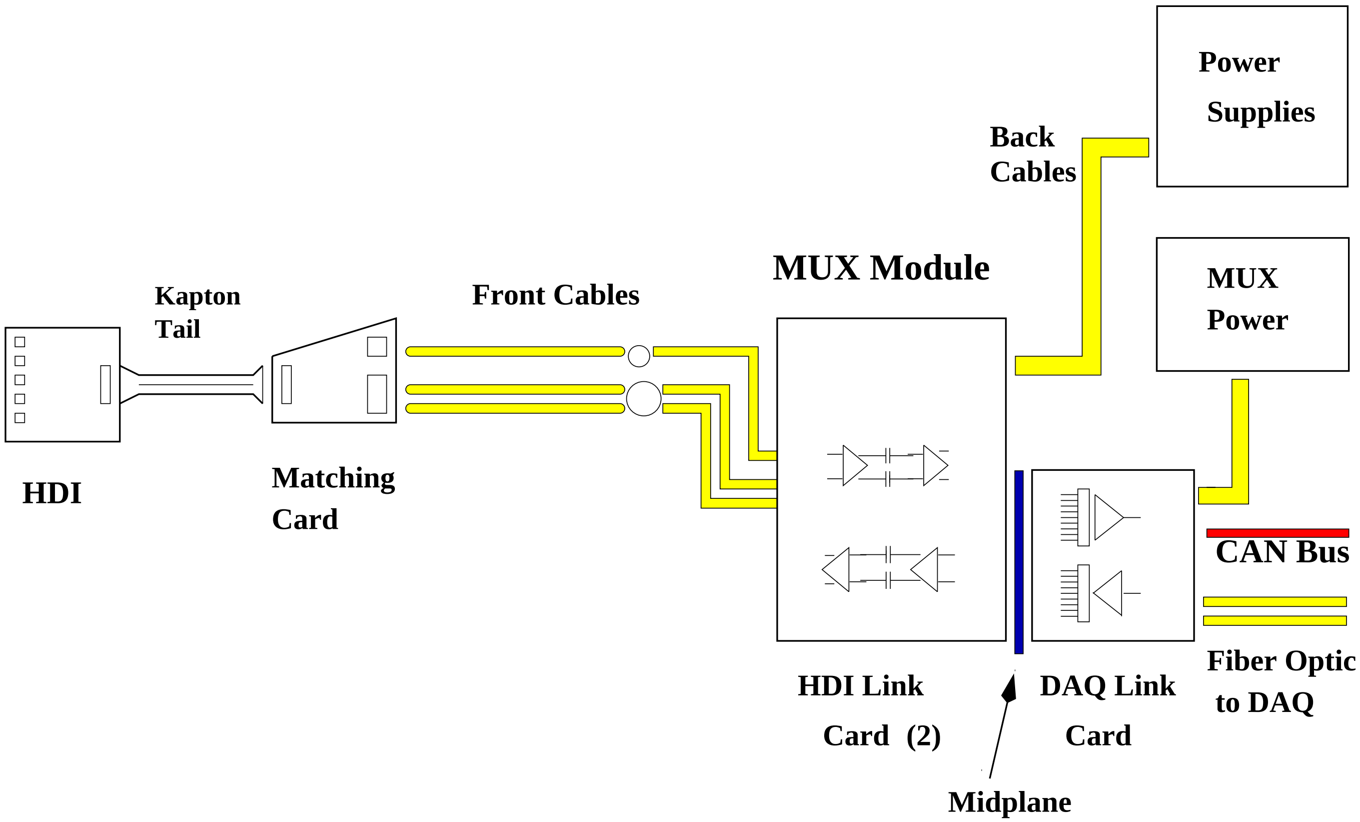

Figure 1: Overview of the SVT Data Transmission System

Total count for the DAT PC boards:

	forward	backward
Matching Cards	52	52
HDI Link Cards	26	26
DAQ Link Cards	14	14
MUX Midplanes	4	4

A MUX module consists of 1 DAQ Link Card + 2 HDI Link Cards. Thus, we have 28 MUX Modules, 4 of which are only "half modules", i.e. 1 DAQ Link Card + 1 HDI Link Card.

The schematics and layout files of all PCBs as well as all the cable pinout information can be found on the SVT DAT web page `http://scipp.ucsc.edu/groups/babar/DAT.html`.

2 How to connect the DAT system

All the outside world connections to the DAT are indicated in fig. 1. From the inside out: Connect the tails of n– and p–side to the respective side on the Matching Card. Each Matching card connects to one set of power and signal cable. Figure 2 shows the layout scheme of the HDI Link Card. Be careful to always connect the signal and power cables of one HDI to the same channel on the HDI Link Card.

The DAQ Link Card and HDI Link Card interconnect via the midplane in the MUX crate. As seen from the DAQ Link Card side of the crate, of the 4 HDI channels serviced by it, channels 1 and 2 are routed to the HDI Link Card offset to the left side, channels 3 and 4 are routed to the right side. The multisource power cables (carrying D5/D0n, A5/A0n etc.) plug into the back of the HDI Link Card, again channel 1 is the connector on top.

External connections to the DAQ Link Card are the optical fiber cables (that should have a little plastic holder making the orientation of transmitter/receiver obvious) and the MUX power cables, providing the power for the DAQ Link Card at ECL level (**DAQ_VEE** 0V/-5.2V) and TTL level (**DAQ_VDD** +5V/0V) and for the circuitry on the HDI Link Card that runs on "system ground" ECL level (**HDI_VEE** 0 V, -5.2 V), i.e. is not voltage translated to the detector bias voltage. Each MUX Module is powered separately. The CAN Bus can be accessed via a Front Panel DB–9 connector.

All connectors are keyed, and all cables are of different sex on both ends, so it should be fairly hard to misconnect cables disastrously wrong. However, good bookkeeping is required to connect always the right HDI channel.

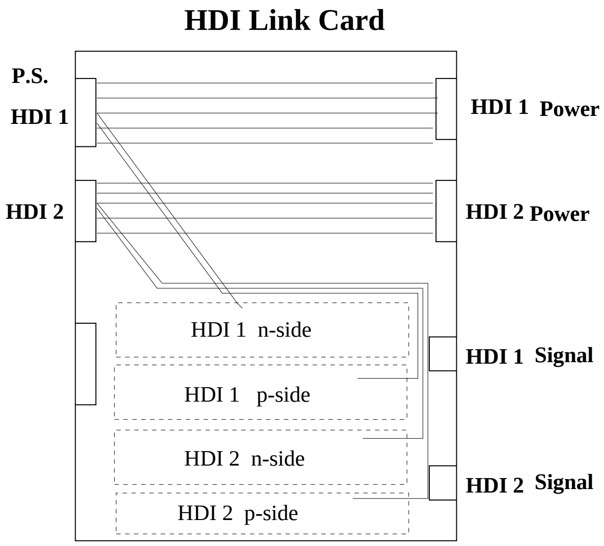

Figure 2: Layout scheme of the HDI Link Card

2.1 MUX Crates

We have 8 MUX Crates in the SVT, 4 each for forward and backward direction. A MUX crate consists of a standard 21 slot VME 6U crate bolted back–to–back to a 12U crate for the large HDI Link Cards. The midplane routes power and signals between the two, and also busses the Shield, Earth and System Common between all modules. Heavy metal lugs are provided at the edges of the midplanes to allow for low–impedance braids to be run inbetween different crates.

In addition to the MUX Modules, PC boards used for temperature and radition monitoring will be housed in the MUX crates, next to the DAQ Link Cards. The temperature lines are collected from the various HDI Link Cards at the midplane and routed to the Temp Modules.

3 Matching Cards

Connections to the Matching Cards are pretty straightforward. The shield of the power cables connects to a pin on the Matching Card, but in the signal cables no free pin is available, so the shield is accesible via a single pin disconnect that should be attached to the pin next to the boardmount connectors.

Default grounding and shielding options realized on the Matching Cards are:

—The cable shield is connected to the cage shield.
—The cable shield is connected via 0.1 μF capacitors
to the A2N and A2P voltages.
—SVT Common is connected to the shield.

4 HDI Link Card

The two basic functionalities of the HDI Link Card are passing and filtering the necessary power to the HDIs, and providing the signal path for clock and commands, and returning data respectively. Because of the floating electronics, all signals are voltage translated from the System Common and referenced to their respective bias voltage.

Voltage translation is done via capacitive coupling of the differential signals. The signal driver circuitry consists of a differential pair of high power transistors. The drivers can be disabled, in the sense that the outputs are frozen in a defined high or low state, and the drive current is substantially reduced.

Disabling the drivers is either via setting the bitmask (see DAQ Link Card) to 0 for the respective channel (`clk_a, clk_b, cmd_a or cmd_b`), or automatically on power–up as long as D5N/P is below a certain threshold (4.25V) to allow the AToM chips to go through their reset sequence.

Various testpoints have been implemented where you can trace the incoming and outgoing signals. The are labelled on the silk screen and it should be fairly obvious to find them. A good spot to look for the clk and cmd signals before they leave the card and get send down to the chips is on the metal can of the driver transistors which are labelled, too. Please always keep in mind that at this point these signals are offset by ± 30 V, so do not ground your scope probe and AC couple it.

Voltages can be probed in the top half of the board where test points are provided. The board has also overvoltage protection circuitry (crowbars) on D5, A5, A2, L5 power lines (for n– and p–side). The idea is that as soon as the voltage goes above a set threshold, the power rail is shorted to its return via a SCR. Due to the high current draw, especially on D5, and thus a considerable voltage drop in the Front Cables, the voltages on the HDI Link Card are much higher than the voltage actually measured at the HDIs. And since we did not want to have different HDI Link Card settings for different HDIs (for example a higher setting for Layer 3 HDIs with 10 chips), the crowbar trip voltage settings have to be high enough to accomodate a 10 chip hybrid with some overhead margin.

The numbers we got from Mark Nyman for the trip voltages are 7 V for D5 and A5 and

5 V for A2. L5 is set to 6 V trip voltage and is uncritical, since there is no further voltage drop in the front cables. These settings might actually turn out to be too low, and if you experience trouble in powering up module, refer to the crowbar section in the Troubleshooting section on how to change the setting or disable the crowbars.

5 DAQ Link Card

The DAQ Link Card is the most complicated Card within the DAT system. Its main circuitry blocks are the G-Link Block, the FPGA circuitry and the CAN Bus.

This manual will not cover the CAN Bus, please refer to Juerg's note, available on the web from the DAT webpage.

Due to the change in nominal clock speed of the AToM chip to 30 MHz, and the BaBar general clock being 60 MHz, the G–Link runs in a mode where commands are received at 60 MHz, and data is sent back at 30 MHz. The FPGA is taking over the task of "stretching" the command bit stream to 30 MHz, and since the length of the commands can vary, it actively decodes commands in order to know when to start looking for the next command start bit again. Also, the FPGA provides the 30 MHz clock that is fanned out and sent down to the AToM chips. For a description of the FPGA functionality, please refer to David's write–up, also accessible from the DAT webpage.

The G–Link part consists of the Finisar optical transceiver and the G–Link transmitter and receiver chips. These multiplex and de–multiplex, repectively, 16 parallel channels into a serial high speed signals. The receiver derives the clock frequency from the incoming data frames. In this duplex mode, the G–Links undergo a start–up handshake procedure with the G–Links on the other side of the link (DAQ ROM), and will be ready to send and receive data once both sides have achieved lock.

9 commands are sent down to the DAQ Link Card, 8 for the 4 HDIs and the so–called 9th channel, that contains information for the DAQ Link Card, for example on how to choose the bitmask settings.

Since the transmitter sends the data to the ROM at 30 MHz, the clock between the Rx and Tx is divided–by–two in frequency. This is a separate clock path than the 30 MHz clock provided by the FPGA that is eventually sent to the chips, since the AToM clock can possibly change its phase by 180 degrees upon receipt of a *Sync* command. This would cause the G–Links to momentarily lose lock, which is clearly undesirable. This different clock path leads to a fairly constrained timing on the data coming back: The Tx latches its inputs on the rising edge of the Tx clock and needs a setup time of 6 ns, with no hold time required. The phase between the returning data and the Tx clock is first of all arbitrary, depending on cable lengths etc. Moreover, since the AToM clock might change phase, the setting between the data and the Tx clock has to be in a way that allows both clock phases to give valid data transmission.

Tx DIP Switch setting The TX clock and data phasing should be adjusted in the following way: Measure the data (at the termination resistors close to the Tx inputs and the Tx clock (at the capacitor C133). Change the clock delay by toggling the dip switches (U41) so that the edge of the data is **6–11 ns** before ANY edge of the clock, it does not matter which one. The delay is a 4 bit delay with 1 ns steps, so you can change the clock propagation time by 16 ns, enough to bring one of the clock edges in the accepted window range.

Clk/Cmd Switch Setting The AToM chip is not very picky about the phase between clock and commands, but the setting should be such that the command edges are at least 6 ns before the rising edge of the clock. It would be best to measure the phase between the two at the HDI Link Card drivers (on the metal cans of the transistors, remember the voltage offset). Adjust the command register clock (and thus the phasing between the AToM clock and the commands by changing the settings on the DIP switch close to the FPGA (U1). It's a 4 bit delay with 2 ns steps, covering the full range of the 30 Mhz signals.

Bitmask settings The DIP switches on the front panel of the DAQ Link Card let you set the bitmask for the signal drivers on the HDI Link Card. You can independently select to enable/disable A or B. The sequence of bitmask bits is from the top of the card down: HDI1_Nside_A, HDI1_Nside_B, HDI1_Pside_A, HDI1_Pside_B,.... HDI4_Pside_B. The last switch is the "Master" switch that tells the FPGA if it should take the bitmask from the DIP switches or by decoding the 9th command channel. To enable a channel, flip the DIP switch to the OFF position. **Note:** The DIP switch settings are only read in when the FPGA is reset, so when you want to change bitmask setting during running, you have to reset the FPGA by power–cycling.

6 Troubleshooting

6.1 Trouble powering the MUX or detector modules

If you experience problems on powering up the modules, i.e. the power supply goes into compliance at maximum current, the most likely candidate is on of the crowbars. We have experienced repeatedly crowbars firing on the DAQ Link Card when using bench top supplies, that tend to have voltage spikes when you turn them on. An easy fix is to ramp the voltage up by hand.

If one of the detector voltages does not come up because of a crowbar firing (easy to tell, they get *really* hot, most likely the HDI draws a lot of current, and the voltage rating for the crow bars is not sufficiently high. In that case, one fix is to change the voltage by adjusting the threshold voltage or by disabling the crowbar altogether. The crowbar is gated by a MC3423 voltage sensor chip whose input it connected to a voltage divider. The resistor values in that divider determine the trip voltage. To set the trip voltage to a higher value, either increase the resistor value of the resistor between the positive power rail and the input (Pin 2), or decrease the resistance between the input and the power return. If you are fed up with crowbars, you can disable it easily by taking the respective resistor between the positive rail and the input off.

In any case, once the crowbar has fired, you have to turn off the voltage completely. In some cases we saw the problem that even after powering down, on the next power up try the crowbar would fire at a very low voltage (around 2V). This is due to the problem that sometimes it might charge up. One way to discharge it is to short the two outer legs of the crowbar with tweezers, for example. We will look into providing a high-ohmic discharge path in case there are a lot of problems with firing crowbars.

6.2 The DAQ ROM and the DAQ Link Card G–Links don't lock

. First of all, check if the voltages provided to the DAQ Link Card are what they are supposed to be (DAQ_VEE -5.2V and DAQ_VDD +5V). I have seen that the G–Links seem to be very sensitive to not having the right voltage.

Second, check that all settings on the DAQ Link Card are right. You should have gotten the card with one pin–header jumper set, JMP22 should have pins 2 and 3 connected. No other jumper should be connected within the G–Link Area. Is the DIV setting for the G–Link Tx correct, i.e. is R200 (close to the Tx and Finisar) loaded with a 0 Ohm surface mount jumper ?

Does the Rx recognize the 60 MHz clock? Does the Tx get a 30 MHz clock. Are the STAT0 and STAT1 bits stable?

In most cases, if you don't get the G–Links to lock with the correct voltage setting, the correct jumper settings and a working optical fiber (worth checking), it's time to send the card to UCSC for a thorough debugging...

6.3 No data, or flaky data back

It is worth checking if you are really sending out commands and clock as you think you are. Check on the HDI Link Card drivers that you see commands and clock actually being sent to the chips. Maybe the bitmask settings are wrong and disable the drivers. If no commands and clock are sent out, try to check at the input of the HDI Link Card (labelled test points are provided) whether the signals get stuck on the HDI Link or DAQ Link Cards. On the DAQ Link Card, you can check easily the command stream before and after the FPGA (TTL level) on the pin–headers. If commands/clock get stuck somewhere inbetween there, time to ask UCSC.

More likely, however, is that cmd/clk are sent down to the chips, but either no data comes back, or it is somehow scrambled. If you see no data at the HDI Link Card inputs, then either the chips are in fact not responding, or you may have a bad connection downstream. You might want to check the phasing between clk/cmd. If something arrives at the HDI Link Card, but it does not seem to make sense, check whether the Tx timing between data and Tx clock is optimally adjusted. You might for instance have one data channel arriving at a slightly different time than the others. If your Tx timing was right at the edge, the data of this channel might be latched one clock cycle too early or late. If the Tx timing looks okay, check if you see problems with the G–Links, like occasional loss of lock, by probing the STAT1 and STAT0 bits at the resistors R148 and R147.

References

[1] A. Eisner et al., *The Data Transmission System for the SVT*, BaBar Note, to be released