The Data Transmission System for the SVT

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Abstract

This note provides a system description of the data transmission system for the BaBar Silicon Vertex Tracker.

Contents

1 Functional Overview

The BaBar Silicon Vertex Tracker (SVT) consists of 5 layers of double sided AC–coupled silicon strips, read out by a custom-designed integrated circuit (AToM chip) that provides digitization, buffering and sparsification. Hence, the signal communication between the readout ICs and the Data Aquisition System (DAQ) is purely digital. The task of the Data Transmission System (DAT) is to provide the signal information exchange between the readout ICs and the DAQ as well as the necessary power to the readout chips in a reliable and low noise fashion.

The basic strategy of the SVT Data Transmission System is to transport information within the detector volume as electrical signals and to convert to high speed optical signals immediately outside the detector. These optical signals can then interconnect to the DAQ outside of the interaction hall. The electrical signals will be fully differential to minimize noise disturbance to the front-end electronics. Furthermore, the electrical signals will be referenced to the digital common potential of the Readout Section to which they connect, in order to minimize the voltage across the AC coupling capacitance at the silicon strips. One goal of this strategy is to minimize the number of active components inside the detector volume to improve reliability.

The major components of the Data Transmission System are shown in fig. 1. Starting at the SVT Readout Section, signals and power are transmitted through a custom kapton cable called the tail between the HDI (High Density Interconnect), which contains the front-end ICs, and the Matching Card, located between the B1 and Q1 magnets but still inside the support tube. The Kapton Tail design is constrained to fit in the extremely limited space available in this region. The Matching Card forms the transition point from the Kapton Tail to a more conventional cable bundle called the Front Cables. It is constrained to thread through the gap between the Q1 magnet and the outer shell of the support tube and runs through the remaining length of the support tube exiting at the end between Q1 and Q2. At the end of the Support Tube, a break must be made in the cables to accommodate the detector assembly plans. From this connector the cables will make their way out of the detector and connect to the MUX Module located in a crate just outside of the BaBar detector.

The MUX Module serves several functions. Its principal one is to multiplex data signals from four HDIs into one fiber optic channel running to the DAQ cards, and to distribute clock and command signals brought in on one fiber optic channel from the DAQ card to four HDIs. One MUX Module consists physically of three PC boards. The DAQ Link Card provides the connection to the DAQ system and translates the optical to electric signals and vice versa. The DAQ Link Card and the two (identical) HDI Link Cards will be connected through a VME backplane. At the HDI Link Card the SVT Power Cables (in the following refered to as the Back Cables) are brought

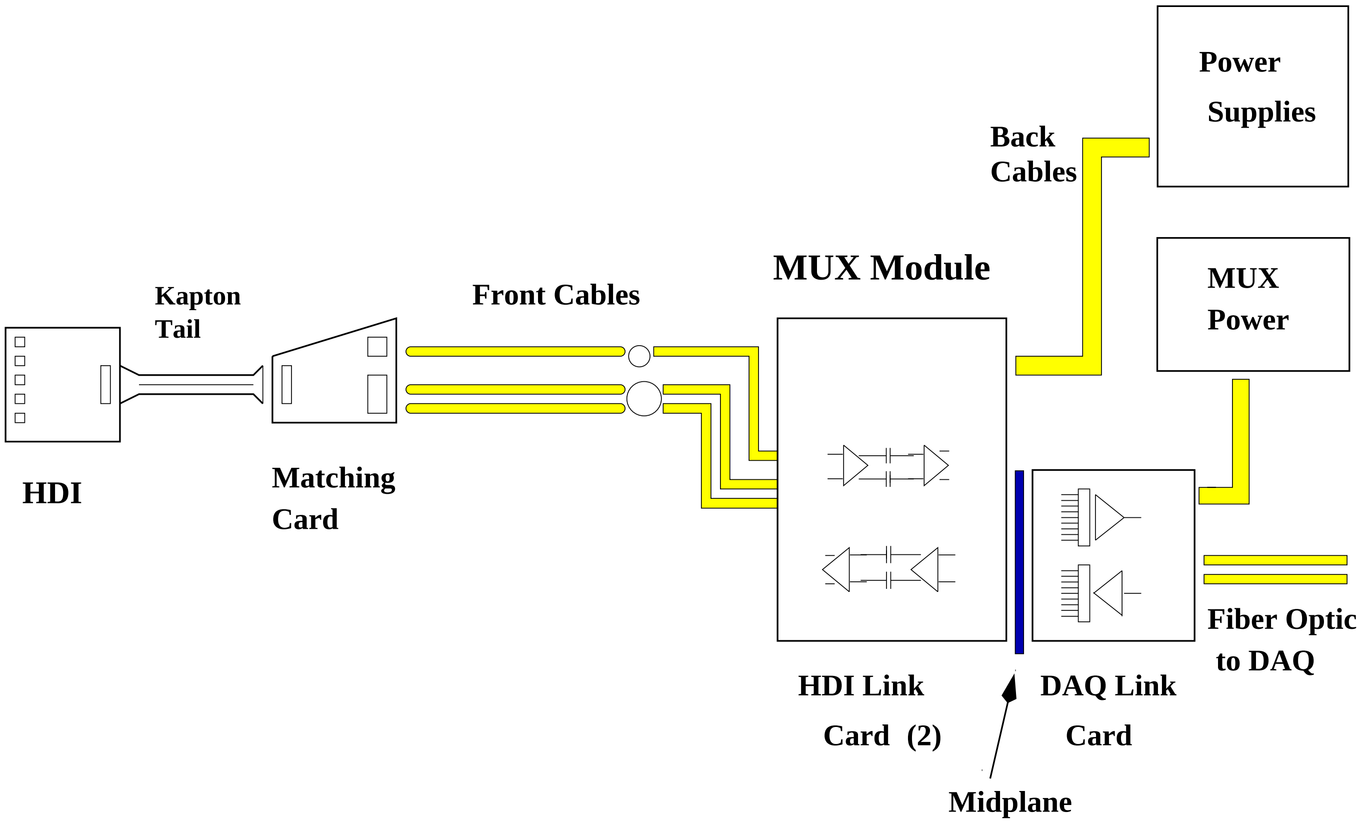

Figure 1: Overview of the SVT Data Transmission System

in as separate bundles from the power supplies. On the HDI Link Card the electrical signals are referenced to the Digital Common Potential of their respective HDI. Power and signal cables are bundled together as the Front Cables mentioned above. The power for the MUX Modules is brought in by a different set of cables.

The following summarizes the different signal and power lines that are needed to service one HDI side (either n– or p–side):

- **Power lines:**
  - Analog 2V and corresponding sense lines
  - Analog 5V and corresponding sense lines
  - Digital 5V and corresponding sense lines
  - BiasRing N/BiasRing P (for n–side) or
    EdgeGuard P/BiasRing N (p–side)

  The nominal bias voltage for the SVT is $\pm$ 30 V. Note that all the voltages for the front–end IC are referenced to this bias voltage, i.e. the voltages on the n– and p–sides are offset by 60 V.

  In addition, the temperature monitoring lines will be brought to the MUX Modules together with the power lines.

- **Signal lines:**
  To the front–end ICs:
  - 2 Clock lines, `clk_a` and `clk_b` (for redundancy)
  - 2 Command lines, `cmd_a` and `cmd_b`

  From the front–end ICs:
  - 2 Data lines, `data_left` and `data_right`

The 5 SVT layers contain a total of 104 HDIs.

In the following, the different parts of the Data Transmission System, i.e. the Matching Card, and the different boards comprising the MUX Module, and the different cables will be described in detail.

2 Matching Card

The Matching Card forms the transition point between the Kapton Tail and the Support Tube Cable. In addition to providing a simple mechanical connection point for these two dissimilar cables, the Matching Card will provide two electrical functions. First, impedance matching between the Kapton Tail and the Support Tube Cable, and second, extra bypassing between all the DC lines. The need for extra bypassing is due to the fact that space on the HDI is extremely limited. The length of the Kapton Tail is short enough that extra capacitance on the Matching Card will provide lower impedance supplies to the Front-end ICs. Since this card sits inside the support tube, repair work requires a significant down period to open the detector and remove the support tube. Thus, to maximize reliability the Matching Card contains only passive components.

Impedance matching between the Kapton Tail and the Support Cable is achieved via a resistor placed in parallel across the pair of leads for each differential signal.

The bypassing circuitry on the Matching Card mirrors the circuitry on the HDI, a mere 50 cm apart. Additional bypassing between the power lines and their respective returns is accomplished by a series of ceramic capacitors in parallel. The new MuRata caps, rated at 10 V, with a capacitance of 4.7 μF have been chosen, polarized electrolytic caps have been avoided for reliability reasons. Bypassing between the n– and p–sides is done with ceramic 0.1 μF capacitors. The Matching Card incorporates the possibility to couple the A2N and A2P lines capacitively to the shield of the SVT.

The sense lines for the power supplies will be RC terminated on the Matching Card to damp reflections in the transmission cables. Also, each sense line will be connected to its respective power line through a large resistor (10 kΩ) in order to provide a voltage reference close to the load in case of the loss of a sense line connection on the tail or the HDI.

The Support Tube Cable will be attached to the Matching Card with the Millipacs connector described above. The Kapton Tail will be connected to the Matching Card via a surface mount Berg connector.

The forward and backward Matching Cards are electrically identical but differ in geometrical shape due to the differences in space requirements.

Specifications for the matching card:

- Channels per card: 1 double-sided HDI
- Quantity: 104 (52 at each end of the detector)
- 8 layer PCB

3 MUX Module

The MUX Modules will be housed in four racks outside but near the detector, two on each end. Each rack will have 2 crates with a total of 7 MUX Modules per rack.

As previously mentioned, one MUX Module services 4 HDIs and consists physically of one DAQ Link Card and two HDI Link Cards (serving 2 channels each). DAQ and HDI Link Cards are interconnected through a custom midplane. The DAQ Link Card will sit in a 6U VME card frame that is back–to–back to the frame housing the HDI Link Cards. The Back power cables will be connected to the upper half on the back of the HDI Link card which has twice the physical height than the DAQ Link card (12U). The MUX power cables will connect to the front panel of the DAQ Link Card and the power for the HDI Link Card be passed through the midplane.

The main functionality of the DAQ Link Card is to demultiplex and transform into electrical signals the control signals (clock and commands) that arrive from the DAQ via a serial optical link. Vice versa, the 16 data lines with the data of the 4 HDIs will be multiplexed 16-to-1 and will be sent back to the DAQ via optical fiber. The signals are sent to and received from the HDI Link Cards through VME connectors as differential ECL logic signals. In addition, the DAQ Link Card incorporates control functions of the clock duty cycle and bitmask settings. Monitoring of these settings and other status information from the card is accomplished through a CAN bus interface that will connect to the Slow Control System. For a more detailed description of the circuitry please refer to sec. 3.1.

The main function of the HDI Link card is to reference the electrical signals running between the HDIs and the DAQ Link card to the digital common of the respective HDI side. Both sides of one HDI have a different digital common, the difference corresponding to the detector bias voltage. Therefore, the transmitting and receiving circuitry on the HDI Link card must operate referenced to this offset potential. And since each HDI will have its own power supply that may be turned on or off independently of every other HDI, the Digital Common for each side of each HDI must be supplied to the HDI Link card and that potential used to reference the driver and receiver circuitry.

The MUX Module will be powered by 3 separate power supplies that will provide +5V/0V and 0V/-5V for the DAQ Link and 0V/-5V for the HDI Link Cards. In addition, the driver and receiver circuitry on the HDI Link Card runs off the offset voltage referenced to the digital common at the HDI (Local_5V).

It should be noted that all the MUX Modules will be built identical, independent of the specific HDIs they will service. The data signals will be sent back to the DAQ always in they same way, e.g. first the data from the p-side. As for layers 4 and 5 the z- and phi-strips have reversed polarity than for the inner 3 layers, the z and phi information for the outer 2 layers will be sent to the DAQ in reversed order. It is the responsibility

of the DAQ to take this into account.
Specifications for the MUX Module:

- Channels per Module: 4 double-sided HDI
- One Module = 1 DAQ Link + 2 HDI Link Cards
- Quantity: 28 Modules, 24 full and 4 "half modules", consisting of 1 DAQ Link and 1 HDI Link Card.

Power consumption (worst case estimates):

DAQ Link Card:	+5V/0V	400 mA
	0V/-5V	4.2 A
HDI Link Card (2x):	0V/-5V	2.3 A

3.1 DAQ Link Card

The DAQ Link Card is connected to the DAQ through the two optical fibers, to the HDI Link Cards via the midplane and to the CAN bus system by a special CAN Bus connector.

The DAQ Link Card is powered by two different supplies that are offset with respect to each other. The optical transceiver and the CAN bus system will be powered by a +5V/GND power supply, the rest of the circuitry by a GND/-5V supply. Due to this split supplies signal transfer between blocks requires voltage translation or change of logic family.

All dynamic board control settings will be received through a dedicated command channel on the G–Link receiver and decoded by a XILINX chip. We will include the possibility of overriding the remote setting via front panel DIP switches. The CAN bus will be used to readback the status of the board, including all the programmable settings and status control bits of the G–Link and Finisar chips.

The major circuit blocks of the DAQ Link Card are the Optical Transceiver, the G–Link circuitry, the CAN bus interface, and the Board Control Command decoder.

3.1.1 The Finisar Optical Transceiver

The card will support 2 optical fibers connected to a Finisar transceiver chip FTR–8510. The electrical input/output is differential ECL at 1.2 Gbit rates. Due to this high speed, the Finisar chip has very stringent requirements on the power supply stability, ripples etc. It is powered by +5V/GND as recommended by the manufacturer.

The Finisar has a CMOS communication protocol that will be serviced by the CAN Microprocessor. Five CMOS signals are needed between the Finisar and the μProc. The

DAQ Link Card will be self–initializing, and this protocol will only be used to determine the Finisar status.

3.1.2 G–Link Circuitry

The Hewlett–Packard G–Link Chipset (HDMP–1012 transmitter and HDMP–1014 receiver) will be configured in standard full duplex mode. Multiplexing and demultiplexing will be performed 16:1 and vice versa. From the receiver data, the 8 command signals for the 8 HDI sides will be reconstructed as well as the 60 MHz master clock. Since 8 of the 16 available data lines on the receiver are nor used, it was chosen to dedicate the 9th channel for sending commands to the board in order to remotely set the bitmask and duty cycle adjust. The front-end ICs on the HDIs have been designed to accommodate a primary and secondary clock input and command input. The secondary clock and command inputs can be used as spare inputs should the primary channels malfunction. The Bitmask Controller determines which driver circuits are actually activated on the HDI Link card by providing it with 16 bits single-ended (negative) CMOS signals (8 x 2 bits for clock/cmd-a and clock/cmd-b). Measurements on the first AToM prototypes indicated a fair sensitivity to the duty cycle of the clock, especially after irradiation. Hence the DAQ Link Card incorporates in its design the possibility to tune the clock duty cycle using a 6–bit delay chip, Elmec PDH6200, with 200 ps steps and a total available delay of 12.4 ns, allowing for any needed clock duty cycle for the AToM chips.

The outputs of the G–Link receiver are single–ended ECL and will be buffered as close as possible to the chip and moved on differentially. The clock signal is fanned out, one differential signal being duty cycle tuned and then consequentially fanned out (x8) and passed to the HDI Link Card. The 8 command signals will pass through latches that are clocked by an adjustably (via DIP switches) delayed master clock to allow for a phase adjustment between commands and the clock signals.

The second clock path drives the G–Link transmitter. The 16 data lines are latched into the G-Link by a clock signal suitably delayed by another 4–bit delay chip to match the phase of the incoming data signals. Testing shows an accepted data window of 9 ns for proper latching. The clock signal driving the transmitter chip will be further conditioned via a phase locked loop.

The design will include the possibility of loop–back testing on the G–Links independent of the optical transceiver.

3.1.3 Command decoder

A FPGA chip (XILINX XC3064A), clocked by the 60 MHz master clock will be deployed to decode the command stream sent on the 9th command channel. One op code for the DAQ Link Card will be used followed by 20 bits of data. The 20 bits will include a register code and up to 16 bits of data. The 9th receiver line will drive a ECL to (negative) TTL converter which drives the XILINX chip TTL configured fast data inputs. Manual input of the bitmask can be selected by a manual tristate control switch. In case of manual control, the FPGA will only readback the status of the set bits. A similar arrangement is used for the setting of the clock duty cycle.

XILINX bidirectional pins:	16 bit mask 6 bit clock duty cycle
XILINX output pins:	8 bit port state (connected to CAN μProc)
XILINX input pins:	6 bit G–Link status 2 bit manual override status (bitmask and duty cycle) 3 bit port state byte select 4 bit command latch clock delay 4 bit G–Link transmitter clock delay Master clock G–Link receiver 9th data channel.

3.1.4 CAN Bus

The CAN bus is a multiwire cable which includes a power supply wire. This power has to be sourced from a module in the CAN VME crate, and will power an on–board CAN bus transceiver and optoisolators. The optoisolators connect to the Microprocessor (Motorola 68HC7805). The CAN bus will be used for monitoring the status of DAQ Link Card settings but will not modify them. (One possible exception being a reset command for the XILINX chip.)

The Microprocessor has 32 I/O ports. 8 of these have internal ADCs tapped to them, so these will be reserved for monitoring voltages and temperatures on the cards. We will monitor the Finisar Optical Power pin, the +5V supply and a voltage reference to calibrate the ADC.

3 ports will be used for the register select function. 8 ports will read the port state byte of the XILINX chip.

The CAN buss will be at +5V, since the isolation of its slow different clock is more convenient. The link to the Finisar will be direct. The CMOS 3 bit port select from the MicroProcessor to the XILINX as well as the 8 bit port byte need simple level shifts (in opposite directions).

3.1.5 General Layout considerations

The primary layout objective is to limit jitter on the 60 MHz clock signal from the G–Link receiver to the G–Link transmitter. Within each G–Link chip, the clock is multiplied up to 1.2 GHz. The 60 MHz clock edge needs to have jitter below 50 ps to provide low error rates on the G–Link system.

Ground(0V) is the only potential used as an AC power plane across the board. The other potentials of 5V and -5V will be layed out as “islands”. A power island will have a series ferrite bead, $\frac{1}{2}$” long, from the general power bus, and a 10 μF tantalum and 0.01 μF NPO chip capacitor bypassing to 0V. All of the transient power used by a chip is sourced out of its own bypass capacitor set. Chip–to–chip crosstalk through the power supplies will be very small, since each group will have its own ferrite filter and capacitor set on its power island. Chips with large transient currents will not disturb other chip functions.

The Finisar and G–Link chip, including the connecting clock conditioning, receive special ground plane treatment. The ground plane will be partially cut around this group, forming “a moat with the drawbridge down”. The drawbridge will be approximately 1 $\frac{1}{2}$” wide. This cut will reduce current flow in the ground plane around this sensitive chip group.

3.2 HDI Link Card

One HDI Link Card services two double–sided HDIs. Its large physical size (12U) is mainly due to the need of board egde space to accomodate all the necessary connections. The HDI Link Card connects to the DAQ Link Card through a VME connector. The power cables from the supplies are brought in from the back of the card, whereas the signal and power cables for two HDIs connect to the front edge of the card. The HDI Link Card is powered in part through the MUX power routed through the DAQ Link Card. The part of the circuitry referenced to the offset detector bias is powered through the power cables of the respective HDI.

3.2.1 Power Filtering

Most of the power filtering on the HDI Link Card is optional. The Card will incorporate the possibility to put all power lines through inductors as well as additional bypassing options. Crowbars (not yet specified) are included in the design for overvoltage protection.

3.2.2 Voltage level shifting

The main design issue on the HDI Link Card has been the decision on the scheme for the necessary voltage translation of the signals to and from the HDIs. Several alternatives have been considered, circuits using transistors, LEDs, Optocouplers or capacitive coupling.

The adopted scheme uses capacitive coupling of the signals and meets our requirements concerning safety for the front–end electronics as well as reliability and performance. The signals, differential ECL logic, are sent by a line driver/receiver chip through two capacitors in series (for safety reasons) to another receiver chip with positive feedback on both its inputs. Hence, the output stages of the second chip are bi–stable and switch polarity only upon receipt of positive/negative input signals. The circuitry for clock/command signals and data signals coming back is essentially identical with the exception that for the data receiver path three receiver stages in series are used and an additional buffer to drive the data to the DAQ Link Card. The latter improves common mode noise immunity, the former guarantees that the data signals are registered by the receivers even if the drivers of the AToM chip are set to low. When the circuit is powered up and no signals are provided on the input lines, the output state of the 10114 is undefined. In order to avoid the the system coming up in a logic high state, the lines are reset to logic low on power up by a transistor steered by the power–sensing circuitry (cf. next section). The transistor on the inverting line just serves the purpose of applying the same load on both lines.

Not only the command and clock signals going to the HDI and the data signals coming back from the HDI have to be voltage translated, but also the (negative) CMOS level bitmask which (de-)activates the drivers. This is conveniently performed with CMOS optocoupler chips.

3.2.3 Signal driver circuitry

Upon power–up the front-end ICs perform some reset sequence and during that time (roughly for 200 ms after the digital voltage exceeds 3 V) clock and command signals should be frozen. We monitor the digital voltage applied to the AToM ICs on the HDI Link Card with a voltage sensing chip from MAXIM which has an user-defined threshold below which it asserts a reset signal. This signal is then delayed by an adjustable counter chip. When the power is below the set threshold, the clock and command drivers described below are disabled and frozen in a defined logic state.

The voltage translated clock and command signals are duplicated into channels a and b by a dual D-latch and sent to the actual driver circuit. The D-latches serve as buffers and in addition offer the possibility to freeze the signals in a well defined state via the assertion of a reset signal. The driver circuits consist of a differential npn-transistor pair and sinks a constant net current (60 mA nominal). The tail consists of a large resistor in parallel with a smaller resistor and a MOSFET. The MOSFET is switched on or off via the selected bitmask and/or the power-up requirement. So if for example clk/cmd-a are chosen, the driver for clk/cmd-b only sinks a small current. In addition, to keep the driver in a defined state, a reset signal is applied to the above mentioned D-latch.

3.2.4 Layout description

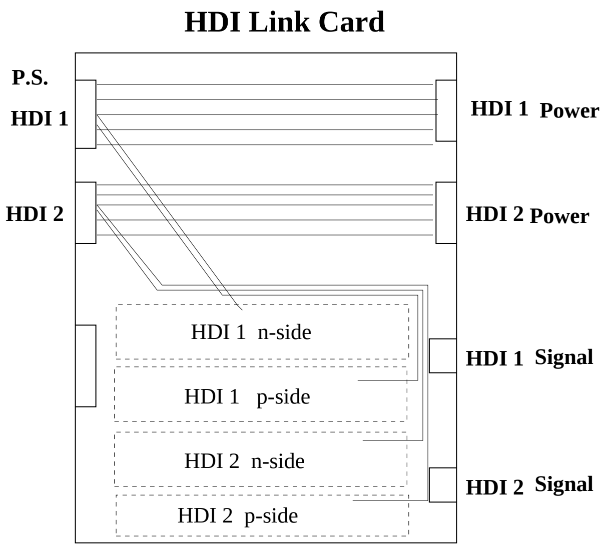

Figure 2: Layout scheme of the HDI Link Card

The HDI Link Card is a 8 layer PCB. As shown in fig. 2, the board is divided into two sections, the upper half being dedicated to routing the HDI power lines through the board to the front edge power connectors and the lower half containing all digital circuitry. The 4 digital cells for the 4 HDI sides are identical. The only connection between the power routing part and the digital circuitry is the routing of the Local_5V/0V and the Digital_5V/0V (that is sensed by the power–up block) to the respective digital cell.

The main layout objective is clearly to keep the analog power lines as insulated from the digital circuitry as possible. To accomplish this, a shield layer will run beneath the power routing section of the board and the front–end connector part, but will not run beneath the digital circuitry. A separate shield runs beneath the power connectors to the power supplies, this shield layer may be strapped directly or through ferrites to the shield plane beneath the power routing section.

The board will have one uncut metal plane dedicated to GND and running through the entire board. Though most likely this is uncritical, the analog power lines will be shielded from it by the shield layer. It should be noted that all digital signals are moved differentially, no large unbalanced currents occur at any point in the circuitry.

3.2.5 Experiences with the first prototype

The above described HDI Link Card has been prototyped as an 8 layer PCB and tested together with the whole readout chain at the testbench setup in Santa Barbara as well as the CERN beam tests.

Up to now, the Readout Module for the DAQ System did not incorporate the G–Link and optical circuitry but communicated via electrical signals (TTL logic) with the MUX Module. Thus, a temporary DAQ Link card has been designed that differs considerably from the final design described above as it is built to provide only logic translation from TTL to ECL and does not include any of the control functions the final DAQ Link Card will include.

Essentially, the tests in Santa Barbara and CERN proved the functionality of the HDI Link Card design. However, an increased sensitivity to noise levels was observed with the PCB prototype compared to a first wire–wrap version (that also had a different voltage shifting scheme). This sensitivity could be tracked down mainly to the more intimate connection to the single–ended TTL on the temporary DAQ Link Card wrt to the wire-wrap boards, a problem that will not be existent in the final DAQ Link Card version.

In summary, the results of our tests showed that the design and layout of the HDI Link Card are functional and working.

Nevertheless, a few improvements/changes w.r.t. the prototype will be incorporated:

- The main changes are in the choice of connectors and connector pinouts.
- The routing of the Local_5V and Local_0V was done in a way that the two traces sandwiched analog power planes. This will be avoided.
- Improved bypassing of the Local_5V to Local_0V (47 μF).
- The voltage sensing chip has now an adjustable threshold.
- The data receivers have been changed and are now more similar to the clock/command paths. The first prototype used AD9696 TTL comparators to receive the data signals. To avoid any potential problems the large voltage swing of the TTL chip may cause, also the data receivers are now purely differential ECL devices. The AD9696 oscillates when its inputs are unconnected, this is not the case for the now used 10114 chips.

- The overvoltage protection crowbars were not included in the first prototype version.

All these changes are reflected in the schematics.

3.3 Midplane Design

The Midplane will be custom–designed. The DAQ Link Card will connect to the Midplane through 2 VME connectors, the HDI Link Cards via 1 VME connector. All signals (clock, commands, data and the bitmask settings will be routed from the DAQ Link to the HDI Link Card. In addition, the Midplane will bus MUX_Common, Shield and Earth through the crate.

Each Midplane will be designed to accomodate 4 MUX Modules and also provide connections for the monitoring modules.

3.3.1 Interface to Monitoring

Each MUX crate will have one Temperature Module that collects the temperature information from the thermistors on the HDIs. The lines are brought to the HDI Link Card in the power cable and routed via the Midplane to the Temperature Module.

The upper crate of each MUX rack will be loaded with 4 MUX Modules and the Temperature Module. The lower rack houses only 3 MUX Modules, and in addition to the Temperature Module possibly a second Temperature Module (connected via its front panel to the first Temp Module), a radiation monitor module and an abort module that –if present– takes the place of the fourth MUX Module.

4 SVT Cables and Cable Connectors

To minimize noise pickup on the cables, all cables have twisted pairs and are individually shielded. The whole cable assembly consists of the power cables between the power supplies and the MUX Module (cf. sec. 4.3), the signal and power cables running between the MUX Modules and the Matching Card (cf. sec. 4.1) and fiber optics cables that connect the MUX Modules to the DAQ system.

4.1 Front Cables inside the detector volume

The Front Cables carry power and electrical signals from the Matching Card to the MUX Module racks located just outside the detector in the forward and backward direction. The total length of the cables is 16 m, with a robust connection at the end of the support tube (3.3 m from the Matching Card), required for installation and to provide access to the forward calorimeter (the portion of the cable between Matching Card and the end of the support tube is called Support Tube Cable, the rest of the cable running to the MUX Module Exit Cable). Figure 3 shows a sketch of the Front Cable connections.

4.1.1 Signal Cables

Per HDI 12 signal pairs are required (4 clock lines, 4 command lines and 4 data lines). The chosen cable is a plenum–rated cable manufactured by Belden. It consists of 12 $\frac{1}{2}$ pairs of stranded conductors, 24 AWG (7x32), with an overall Aluminum/Polypropylene shield and Halar insulation.

- Belden part # 82512
- 12 1/2 pairs, 24 AWG
- Overall diameter: 7.06 mm
- Maximal continous current: 1.5 A
- DC resistance: 0.07644 Ω/m
- Capacitance between adjacent conductors: 75 pF/m
  and between conductor and shield: 138 pF/m
- Nominal inductance: 0.558 μH/m
- Length: 3.3 m + 12 m
- Quantity: 104

The cable can stand up to 10 MRad and showed satisfactory signal transmission characteristics in tests performed at LBL and UCSC (see section 4.6).

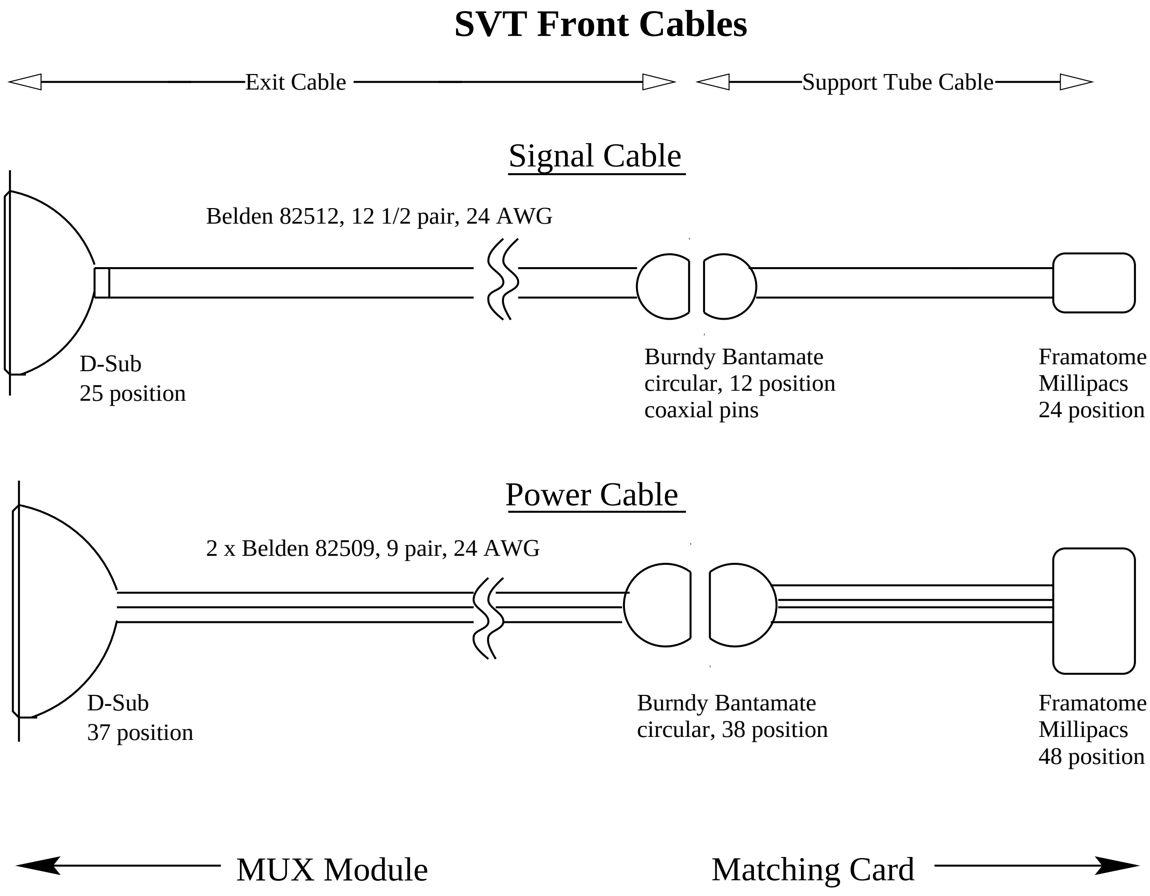

Figure 3: Scheme of the SVT Front Cables

4.1.2 Power Cables

For the Power Cables the same type of Belden cable will be used as for the Signal cables, but instead of 12-1/2 pairs two 9 pair cables are chosen.

- Belden part # 82509
- 9 pairs, 24 AWG
- Overall diameter: 6.25 mm
- Electrical specifications as above
- Quantity: 208

The pairs in the two power cables will be allocated as described in table 1.

p–side	# pairs	n–side	# of pairs
Analog 2V	1	Analog 2V	1
Analog 5V	1	Analog 5V	1
Digital 5V	2	Digital 5V	2
Analog 2V Sense	1	Analog 2V Sense	1
Analog 5V Sense	1	Analog 5V Sense	1
Digital 5V Sense	1	Digital 5V Sense	1
EdgeGuard P/BiasRing N	1	BiasRing N/BiasRing P	1
SVT Common	1	Temperature	1

Table 1: Pair assignment for the Front Power Cables

4.2 Front Cable Connectors

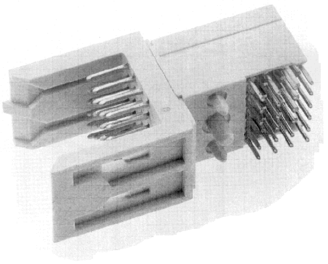

Figure 4: Framatome Millipacs board-mount connector.

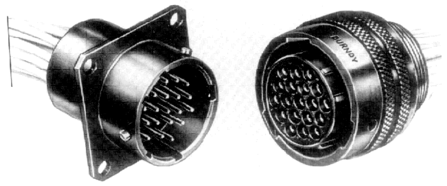

Figure 5: Burndy Bantamate circular connector.

The signal and power cables will be connected to the Matching Card via Framatome Millipacs (24 and 48 positions, respectively). These are 4 row connectors with 2 mm grids (see fig. 4). The shields of both cables will be connected to the Matching Card through a single pin drain wire PCB Jumper.

The cable–to–cable connectors at the end of the support tube are 12 position Burndy Bantamate connectors with coaxial pins for the signal cables and 38 position Burndy Bantamate connectors with single pins for the power cables (both cables fit into one connector). Figure 5 shows the circular connectors.

At the MUX Module, the cables will connect to the the HDI Link Card via dual row D-Sub AMP connectors (37 pins for power, 25 for signal).

	Connector	Part Number	count
Matching Card			
Signal	Framatome Millipacs, 24 position, Right Angle Boardmount, Pin Header	HM1L41AAP000H6	104
	Framatome Millipacs, 24 position, Female cable connector	HM1C01D2C010N9	104
Power	Framatome Millipacs, 48 position, Right Angle Boardmount, Pin Header	HM1L42AAP000H6	104
	Framatome Millipacs, 48 position, Female cable connector	HM1C02D2C010N9	104
Shield	Single position drain wire PCB jumper for shield	WP221B	104
Cable–to–Cable			
Signal (Det. side)	Burndy Bantamate, 12 pos. circular Straight Plug, 27.74 mm diameter	G6F1492PNH	104
	Monocrimp coaxial pins	RMDX60-19D28	1248
(MUX side)	Burndy Bantamate, 12 pos. circular Receptacle, 31.75 mm diameter	G1F1492SNH	104
	Monocrimp coaxial sockets	RCDX60-19D28	1248
Power (Det. side)	Burndy Bantamate, 38 pos. circular Straight Plug, 40.44 mm diameter	G6F2238PNH	104
	Contact pins, 24 AWG	SM24M-1S6	3952
(MUX side)	Burndy Bantamate, 38 pos. circular Receptacle, 42.88 mm diameter	G1F2238SNH	104
	Contact sockets, 24 AWG	SC24M-1S6	3952
MUX Module			
Signal	AMP D–Sub HD–20, dual row, 25 pos. Right Angle Boardmount, Pin header	745436–8	104
	AMP D–Sub HDP–20, dual row, 25 pos. Female Cable Connector	205207–1	104
Power	AMP D–Sub HD-20, dual row, 37 pos. Right Angle Boardmount, Pin header	745437–8	104
	AMP D–Sub HDP–20, dual row, 37 pos. Female Cable Connector	205209–1	104

Table 2: Connectors for the Front Cable assembly

4.3 Back Cables

The power supplies for the SVT will be located at the top of the electronics house outside the shielded area. The Back Cables will bring the power from the power supplies to the MUX racks over a distance of ca. 40 m.
The Back Cables pass through large covered cable trays and are not required to be plenum–rated.

The cable will be tray–rated cable manufactured by Belden. It consists of 24 pairs of stranded conductors, 18 AWG (7x26), with an overall beldfoil shield and PVC insulation.

- Belden part # 1068A
- 24 pairs, 18 AWG
- Overall diameter: 24.44 mm
- DC resistance: 0.01923 Ω/m
- Capacitance: $\approx$ 131 pF/m
- Inductance: 0.623 μH/m
- Length: 40 m
- Quantity: 104

Note: This cable is rated at 600 V. Belden also manufactures a 300 V rated cable, 18 AWG, part # 1471A that may fulfill our requirements and is slightly less expensive. This will be investigated.

In addition to the power lines continuing through the Front Cables, the Back Cables also provide the power to the MUX Module circuitry parts that are running referenced to the respective offset voltages. The pair allocation in the back cables is given in table 3.

	# pairs		# of pairs
Analog 2V P	2	Analog 2V N	2
Analog 5V P	1	Analog 5V N	1
Digital 5V P	2	Digital 5V N	2
Analog 2V Sense P	1	Analog 2V Sense N	1
Analog 5V Sense P	1	Analog 5V Sense N	1
Digital 5V Sense P	1	Digital 5V Sense N	1
Local 5V P	1	Local 5V N	1
Local 5V Sense P	1	Local 5V Sense N	1
EdgeGuard P/BiasRing N	1	BiasRing N/BiasRing P	1
SVT Common	1	—	–

Table 3: Pair assignment for the Back Cables

4.4 Back Cable Connectors

AMP manufactures a 3 row 50 position connector that can handle 18 gage wire and comes in a right–angle boardmount version. However, the insulation on the 1068A cable is fairly thick and will not fit into the plastic housing. If a cable with thinner insulation will selected, this connector would be our prefered choice, otherwise a connector pair of Burndy Trim Trio connectors can be used that is able to handle even larger gage wire.

AMP:
- Right angle boardmount, 50 position, pin header, P/N 745355–4
- Cable connector receptacle, 50 pos., P/N 205211–1
- Crimp Pin Sockets, P/N 745230–4

Burndy:
- Right angle boardmount, 34 position, pin header, P/N MSO34MPG58E1
- Right angle boardmount, 18 position, pin header, P/N MSO18MPG58E1
- Cable connector receptacle, 34 position, P/N MS34RM57
- Cable connector receptacle, 18 position, P/N MS18RM57
- Crimp pin sockets, P/N SM16M1S6

4.5 MUX Power Cables

No final decision has been taken yet on the MUX Power Cables. The Belden cables # 1072A, 12 twisted pairs, 16 AWG or the # 1066A, also 12 pairs, 18 AWG may be suitable alternatives.

The above mentioned Burndy Trim Trio 34 position connectors will be used.

4.6 Signal Cable performance tests

The signal transmission characteristics of the chosen Belden cable has been measured at the nominal clock speed of 60 MHz. Figure 6 shows the setup used for this test. The signal drivers were built as close as possible to the ones employed on the HDI Link Card, with the nominal driver current of 60 mA. The Kapton tail has been simulated by using baby coax cables.

Figure 7(a) shows the small reflections through the transmission lines measured back at the drivers (point marked `Driver_Out` in the schematic). Figures 7(b) and (c) show the input (`Driver_Out`) and output (`Receiver_In`) signals for the clock at nominal speed

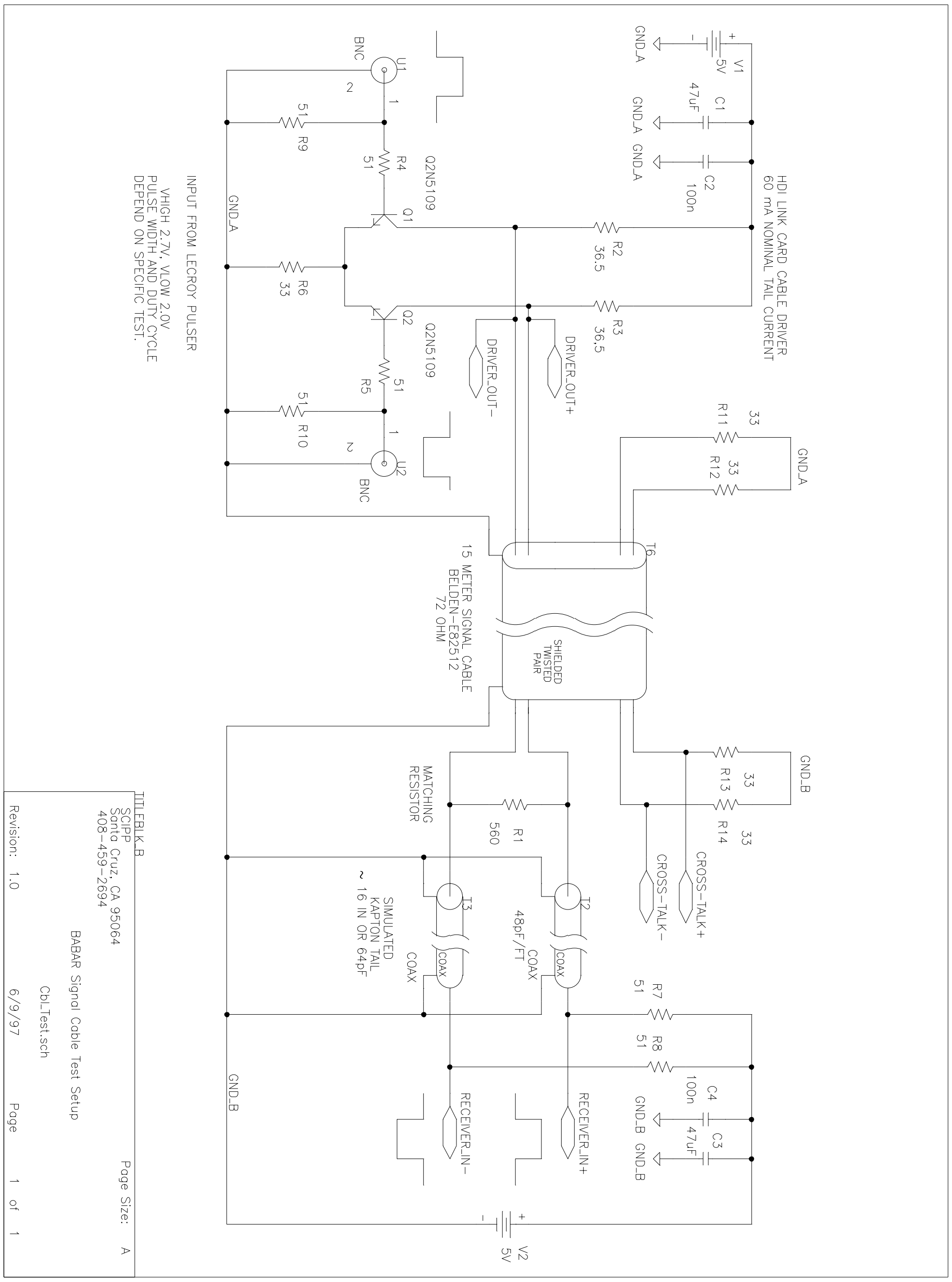

Figure 6: Setup for the cable performance measurements

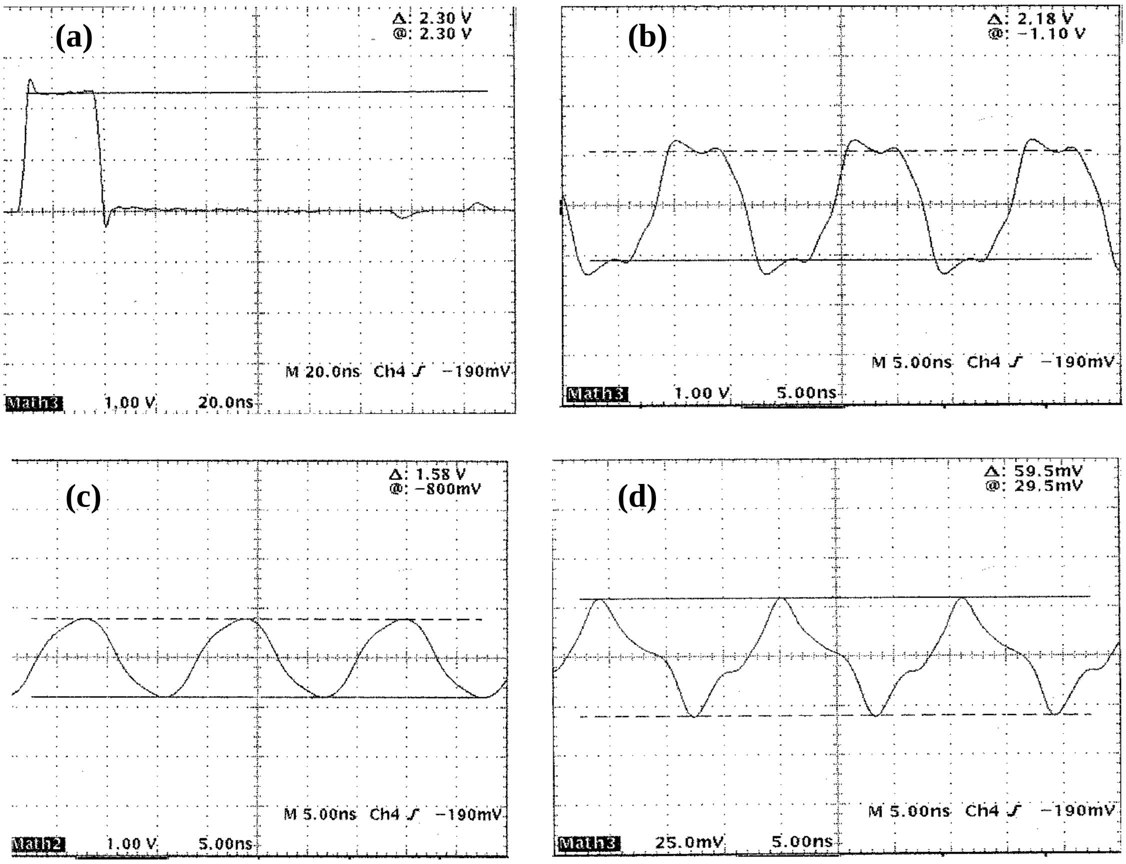

Figure 7: Signal transmission with the Belden cable # 82512. (a) Reflection measurement (b) 60 MHz clock signal measured at input, (c) and output of the cable. (d) Maximum signal observed in an unused pair (crosstalk).

(60 MHz). The attenuation of the signal is 28%. Finally, fig. 7(d) shows the maximal crosstalk signal measured on unconnected but terminated pairs (`Cross_Talk`). The amplitude of the crosstalk signal is 4% of the signal swing at the receiver end.

These results show good signal transmission performance of the Belden cable and are in fact superior to the ones obtained with the former choice of cables.

4.7 Voltage Drop Analysis

The following table contains a list of all the power and sense lines needed for one double sided HDI and shows the expected voltage drops given the lengths and resistances of the different cables and the estimated current draws. The calculation is done assuming the maximum number of 10 chips on one HDI side as will be the case for layer 3. The current estimates stem from measurements performed with the AToM chip prototypes and are assumed to be 350 mA, 250 mA and 580 mA for Analog 2V, Analog 5V and Digital 5V, respectively. This is for one HDI side with 10 chips and including the signal drivers. The calculations take into account that the analog return lines for A2 and A5 are tied together at the power supplies as well as at the front–end. As can be seen from the table, the biggest voltage drops occur in the front cables that have to have smaller gage due to the limited space requirements.

The round–trip voltage drop should be limited to an absolute maximum of 2 V, even though the power supplies are able to handle larger voltage drops. The maximum voltage drop occurs on the D5 lines with 1.27V round–trip. For A2 and A5 the values are about 1V.

Note: The assumed resistance of the Kapton tail is an old value and may have changed slightly. The cable resistances are nominal values. Some margin of error ($\approx 15\%$) should be added to the calculations.

Cable Analysis of DC Voltage Drops

			Kapton Tail		Support Tube Cable			Exit Cable			Power Cable			Total	
					Pair Count			Pair Count			Pair Count				
					24AWG			24AWG			16AWG			Vdrop(V)	Vdrop(V)
					DC Res (Ohm/km)		Length(m)	DC Res (Ohm/km)		Length(m)	DC Res (Ohm/km)		Length(m)		Round Trip
					76.444		3.30	76.444		12.70	19.23		40.00		
	Vmax(V)*	Imax(mA)*	R(Ohm)	Vdrop(V)		R(Ohm/km)	Vdrop(V)		R(Ohm/km)	Vdrop(V)		R(Ohm/km)	Vdrop(V)		
A2 n	2	350.000	0.1	0.0350	0.5	76.44	0.0883	0.5	76.44	0.3398	1.0	9.62	0.1346	0.5977	1.1619
A0 n **	0	330.363	0.1	0.0330	0.5	76.44	0.0833	0.5	76.44	0.3207	1.0	9.62	0.1271	0.5642	
A5 n	5	250.000	0.1	0.0250	0.5	76.44	0.0631	0.5	76.44	0.2427	0.5	19.23	0.1923	0.5231	1.0872
A0 n **	0	269.637	0.1	0.0270	0.5	76.44	0.0680	0.5	76.44	0.2618	0.5	19.23	0.2074	0.5642	
D5 n	5	580.000	0.1	0.0580	1.0	38.22	0.0732	1.0	38.22	0.2815	1.0	9.62	0.2231	0.6358	1.2715
D0 n	0	580.000	0.1	0.0580	1.0	38.22	0.0732	1.0	38.22	0.2815	1.0	9.62	0.2231	0.6358	
A2 sense n	2	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	0.0000
A0 sense n	0	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	
A5 sense n	5	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	0.0000
A0 sense n	0	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	
D5 sense n	5	0.001			0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	0.0000
D0 sense n	0	0.001			0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	
Bias Ring n	50	1.000	0.1	0.0001	0.5	76.44	0.0003	0.5	76.44	0.0010	0.5	19.23	0.0008	0.0021	0.0042
Bias Ring p	50	1.000	0.1	0.0001	0.5	76.44	0.0003	0.5	76.44	0.0010	0.5	19.23	0.0008	0.0021	
Temp Sensor+			4.0	4.0000	0.5	76.44	0.2523	0.5	76.44	0.9708		0.00	0.0000 :=	5.2231	10.4462
Temp Sensor-			4.0	4.0000	0.5	76.44	0.2523	0.5	76.44	0.9708		0.00	0.0000 :=	5.2231	
A2 p	2	350.000	0.1	0.0350	0.5	76.44	0.0883	0.5	76.44	0.3398	1.0	9.62	0.1346	0.5977	1.1619
A0 p **	0	330.363	0.1	0.0330	0.5	76.44	0.0833	0.5	76.44	0.3207	1.0	9.62	0.1271	0.5642	
A5 p	5	250.000	0.1	0.0250	0.5	76.44	0.0631	0.5	76.44	0.2427	0.5	19.23	0.1923	0.5231	1.0872
A0 p **	0	269.637	0.1	0.0270	0.5	76.44	0.0680	0.5	76.44	0.2618	0.5	19.23	0.2074	0.5642	
D5 p	5	580.000	0.1	0.0580	1.0	38.22	0.0732	1.0	38.22	0.2815	1.0	9.62	0.2231	0.6358	1.2715
D0 p	0	580.000	0.1	0.0580	1.0	38.22	0.0732	1.0	38.22	0.2815	1.0	9.62	0.2231	0.6358	
A2 sense p	2	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	0.0000
A0 sense p	0	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	
A5 sense p	5	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	0.0000
A0 sense p	0	0.001	4.0	0.0000	0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	
D5 sense p	5	0.001			0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	0.0000
D0 sense p	0	0.001			0.5	76.44	0.0000	0.5	76.44	0.0000	0.5	19.23	0.0000	0.0000	
Bias Ring n	50	1.000	0.1	0.0001	0.5	76.44	0.0003	0.5	76.44	0.0010	0.5	19.23	0.0008	0.0021	0.0041
Edge Guard p	50	1.000	4.0		0.5	76.44	0.0003	0.5	76.44	0.0010	0.5	19.23	0.0008	0.0020	
SVT Common					1.0			1.0			1.0				
LD5 p	5	500.000									0.5	19.23	0.3846	0.3846	0.7692
LD0 p	0	500.000									0.5	19.23	0.3846	0.3846	
LD5 n	5	500.000									0.5	19.23	0.3846	0.3846	0.7692
LD0 n	0	500.000									0.5	19.23	0.3846	0.3846	
LD5 sense p	5	0.001									0.5	19.23	0.0000	0.0000	0.0000
LD0 sense p	0	0.001									0.5	19.23	0.0000	0.0000	
LD5 sense n	5	0.001									0.5	19.23	0.0000	0.0000	0.0000
LD0 sense n	0	0.001									0.5	19.23	0.0000	0.0000	
Total Pair Counts					18.0	0.0		18.0	0.0		23.0	0.0			

* Note that, except for "Bias Ring n" and "Bias Ring p", Vmax is voltage relative to offset potential for each side of HDI. Also, note that Imax assumes that the maximum number of ICs per single side of HDI is given by MaxICs.

MaxICs = 10.000

** Note that the currents on A2 Com and A5 Com are adjusted assume they are tied at both ends.

5 Mapping of HDIs to MUX Modules

This section summarizes a proposal for the assignment of HDIs to MUX units, and hence to the DAQ Link fibers which transmit the SVT data to the readout modules. There are 104 HDI's in the system; up to four can be served by a single MUX unit.

Possible grouping motivations are listed below:

Mechanical Cabling and other space considerations dictate that the forward and backward regions are served by separate MUX units, and that the forward units are left-right split, so that 14 DAQ link cards are needed to serve the forward region, 7 in one crate on the −x side, and 7 in one crate on the +x side. For both symmetry and simplicity, this suggests that the backward region also utilize 14 DAQ link cards, rather than the 13 minimally required.

Cabling simplicity also suggests grouping relatively locally in azimuth, in order to avoid excessive crossing of cables en route to the MUX crates.

Data Flow Although estimated occupancies due to X10 beam backgrounds (primarily from lost particles) do not apparently strain the bandwidth limits of the readout module, it is still prudent to reduce the spread of expected data rates over the set of fibers, and to minimize the maximum rate.

The TDR presents some information on both fractional occupancies and the radiation dosages due to them. Dosages based upon more recent background calculations are presented in BABAR #302. A hot region near an azimuth of 180 degrees is shown, a secondary hot region near 0 degrees, and a strong decrease as a function of radius. Until limited by binomial statistics, the average number of hits in a half-module should be proportional to the average radiation dose times the area of the half-module times the z-strip enhancement factor.

Level 2 Trigger The still hypothetical Level 2 trigger might make use of SVT input data. One may ask if any choice of grouping might facilitate such use. Although the trigger group is not concerned about this issue, it seems reasonable that azimuthal grouping would be the most helpful organization; in fact, the Level 3 algorithm under development does work in azimuthal segments, using both z and phi data. Such grouping is already implied by mechanical considerations. Hence the trigger need not to be considered further.

Calibration Runs There may be an argument for grouping channels with similar AToM chip settings (gain, peaking time, threshold), to simplify both downloading of registers and interpretation of calibration data. However, we have not identified a strong motivation for this. Since the implied grouping within similar layers would conflict with the mechanical and data flow considerations, we have not taken similarity of settings into account

5.1 Proposed Organization

The mechanical considerations suggest grouping in azimuthal sectors; the main complication is that while layers 1, 2, 3 and 5 have six-fold symmetry, neither layer 4 nor the target number of MUX units (14) is commensurate with this. The data flow considerations further suggest that no MUX have more than one HDI from layers 1 and 2; and that the MUX units near 180 and 0 degrees not have more than one HDI from any of layers 1, 2 or 3. We can take advantage of the full six-fold symmetry for six MUX units, which we have chosen to fill with layers 2 and 5 (a choice which could have some utility for a Level 2 trigger). Of the 14 units, 12 are full and 2 are half-full; this saves on HDI Link cards. Finally, forward and backward readouts are mirror images; that is, the same thing happens for the same phi and layer in both.

The following is a conceptual list of the MUX assignments. The notation Layer N(j) is used to mean the jth half-module of layer N, where according to BABAR-273 this implies the same phi value for both forward and backward halves.

Layer 2(j) + 3 commensurate Layer 5,	j = 1 to 6	6 units (full)
Layer 1(j) + Layer 3(j) + 2 Layer 4,	j = 2,3,5,6	4 units (full)
Layer 2(j) + 3 Layer 4	j = 1,4	2 units (full)
Layer 1(j) + 1 Layer 4	j = 1,4	2 units (half-full)

5.2 Detailed List

We tentatively number the MUX units from 1 to 28, where 15 to 21 are in ordered slots in the forward crate near phi = 0 degrees, 22 to 28 are in the forward create near phi = 180 degrees, and 1 to 14 serve the same phi values in order as 15 to 28, but for the backward readout. We identify HDI's by notation N-jx, where the layer N can be 1 through 5, j is in the range from 1 to 18, and x is f (forward) or b (backward). Using the notation of the current layout drawing (see fig. 8), the complete mapping is:

MUX	HDI List (Readout Sections as per BABAR Note # 273 in parentheses)			
1	1- 6b (10,138)	3- 6b (34,162)	4-13b (60,188)	4-14b (62,190)
2	2- 6b (22,150)	5-14b (94,222)	5-15b (96,224)	5-16b (98,226)
3	3- 1b (24,152)	4-15b (64,192)	4-16b (66,194)	4- 1b (36,164)
4	2- 1b (12,140)	5-17b (100,228)	5-18b (102,230)	5- 1b (68,196)
5	1- 1b (0,128)	4- 2b (38,166)		
6	2- 2b (14,142)	5- 2b (70,198)	5- 3b (72,200)	5- 4b (74,202)
7	1- 2b (2,130)	3- 2b (26,154)	4- 3b (40,168)	4- 4b (42,170)
8	1- 3b (4,132)	3- 3b (28,156)	4- 5b (44,172)	4- 6b (46,174)
9	2- 3b (16,144)	5- 5b (76,204)	5- 6b (78,206)	5- 7b (80,208)
10	3- 4b (30,158)	4- 7b (48,176)	4- 8b (50,178)	4- 9b (52,180)
11	2- 4b (18,146)	5- 8b (82,210)	5- 9b (84,212)	5-10b (86,214)
12	1- 4b (6,134)	4-10b (54,182)		
13	2- 5b (20,148)	5-11b (88,216)	5-12b (90,218)	5-13b (92,220)
14	1- 5b (8,136)	3- 5b (32,160)	4-11b (56,184)	4-12b (58,186)
15	1- 6f (11,139)	3- 6f (35,163)	4-13f (61,189)	4-14f (63,191)
16	2- 6f (23,151)	5-14f (95,223)	5-15f (97,225)	5-16f (99,227)
17	3- 1f (25,153)	4-15f (65,193)	4-16f (67,195)	4- 1f (37,165)
18	2- 1f (13,141)	5-17f (101,229)	5-18f (103,231)	5- 1f (69,197)
19	1- 1f (1,129)	4- 2f (39,167)		
20	2- 2f (15,143)	5- 2f (71,199)	5- 3f (73,201)	5- 4f (75,203)
21	1- 2f (3,131)	3- 2f (27,155)	4- 3f (41,169)	4- 4f (43,171)
22	1- 3f (5,133)	3- 3f (29,157)	4- 5f (45,173)	4- 6f (47,175)
23	2- 3f (17,145)	5- 5f (77,205)	5- 6f (79,207)	5- 7f (81,209)
24	3- 4f (31,159)	4- 7f (49,177)	4- 8f (51,179)	4- 9f (53,181)
25	2- 4f (19,147)	5- 8f (83,211)	5- 9f (85,213)	5-10f (87,215)
26	1- 4f (7,135)	4-10f (55,183)		
27	2- 5f (21,149)	5-11f (89,217)	5-12f (91,219)	5-13f (93,221)
28	1- 5f (9,137)	3- 5f (33,161)	4-11f (57,185)	4-12f (59,187)

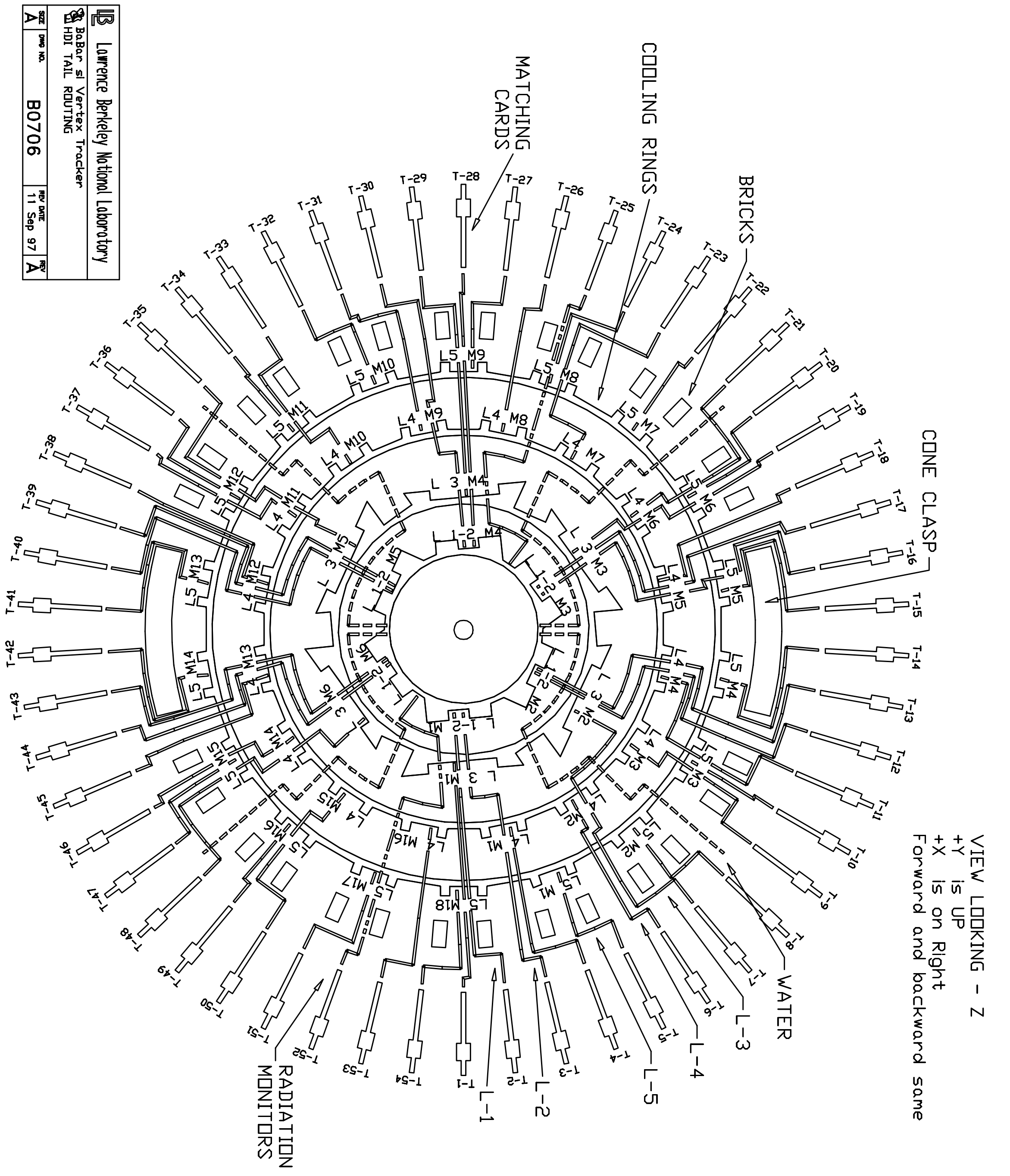

Figure 8: Layout drawing of the tail routing from LBL