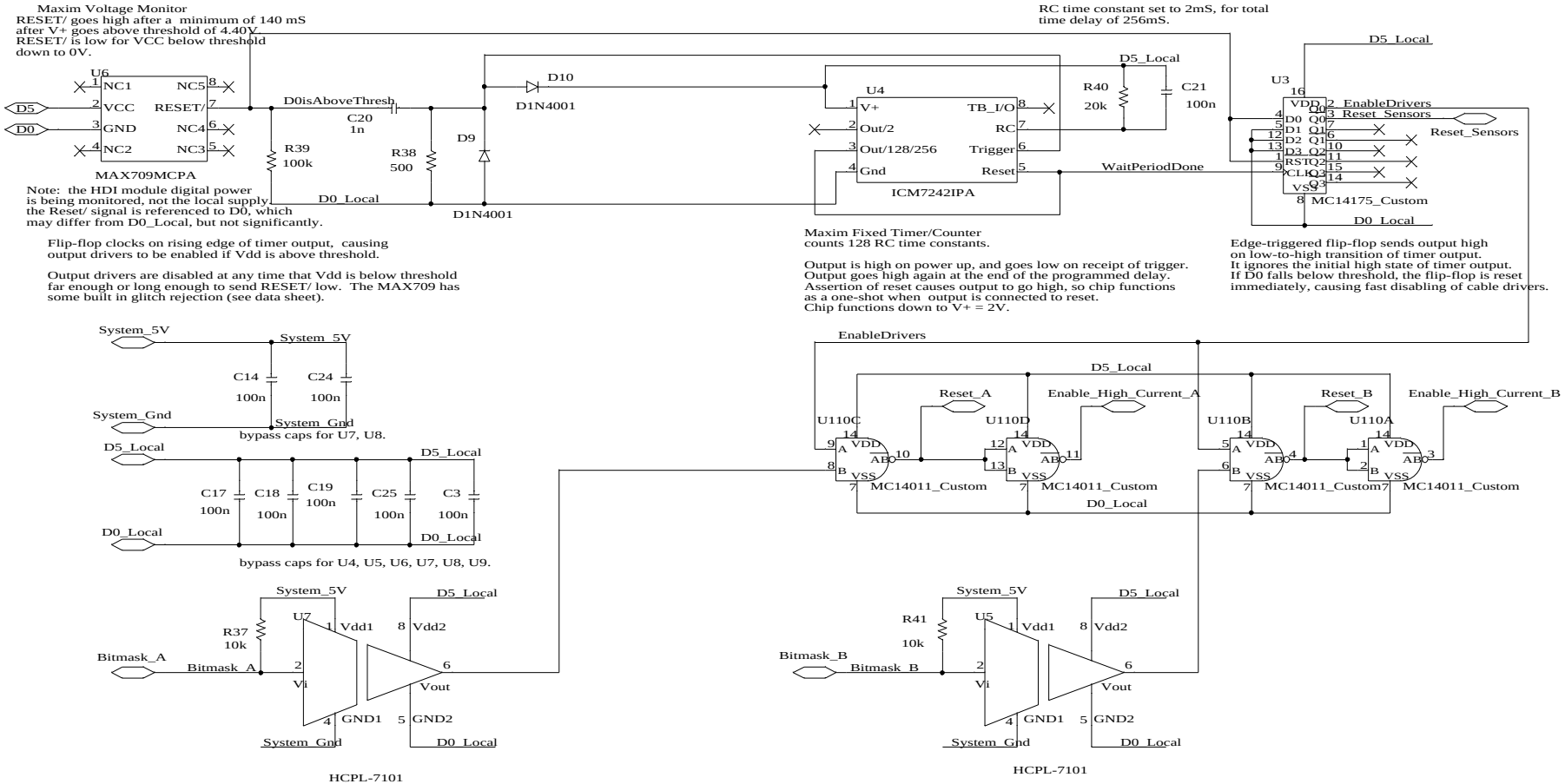
Maxim Voltage Monitor
RESET/ goes high after a minimum of 140 mS after V+ goes above threshold of 4.40V.
RESET/ is low for VCC below threshold down to 0V.
U6
NC1
VCC
GND
NC2
NC5
RESET/
NC4
NC3
D5
D0
MAX709MCPA
D0isAboveThresh
C20
1n
R39
100k
R38
500
D9
D10
D1N4001
D0_Local
D1N4001
Note: the HDI module digital power is being monitored, not the local supply the Reset/ signal is referenced to D0, which may differ from D0_Local, but not significantly.
Flip-flop clocks on rising edge of timer output, causing output drivers to be enabled if Vdd is above threshold.
Output drivers are disabled at any time that Vdd is below threshold far enough or long enough to send RESET/ low. The MAX709 has some built in glitch rejection (see data sheet).
RC time constant set to 2mS, for total time delay of 256mS.
U4
V+
Out/2
Out/128/256
Gnd
TB_I/O
RC
Trigger
Reset
ICM7242IPA
D5_Local
R40
20k
C21
100n
WaitPeriodDone
Maxim Fixed Timer/Counter counts 128 RC time constants.
Output is high on power up, and goes low on receipt of trigger. Output goes high again at the end of the programmed delay. Assertion of reset causes output to go high, so chip functions as a one-shot when output is connected to reset. Chip functions down to V+ = 2V.
U3
VDD
D0
D1
D2
D3
RSTI
CLK
VSS
Q0
Q1
Q2
Q3
EnableDrivers
Reset_Sensors
MC14175_Custom
D0_Local
Edge-triggered flip-flop sends output high on low-to-high transition of timer output. It ignores the initial high state of timer output. If D0 falls below threshold, the flip-flop is reset immediately, causing fast disabling of cable drivers.
System_5V
System_Gnd
C14
C24
100n
bypass caps for U7, U8.
D5_Local
D0_Local
C17
C18
C19
C25
C3
bypass caps for U4, U5, U6, U7, U8, U9.
EnableDrivers
Reset_A
Enable_High_Current_A
Reset_B
Enable_High_Current_B
U110C
U110D
U110B
U110A
MC14011_Custom
R37
10k
Bitmask_A
U7
Vdd1
Vdd2
Vi
Vout
GND1
GND2
HCPL-7101
R41
Bitmask_B
U5
HCPL-7101
Each bitmask bit turns on the clock and command drivers for one channel. The two channels A and B are switched independently. The default state is on, as defined by the 10k pullup resistors. This enables bench testing of the HDI_Link_Card with minimal external inputs.
TITLEBLK_B
SCIPP
Santa Cruz, CA 95064
408-459-2694
Page Size: B
PRELIMINARY
BABAR HDI Link Card
Clock/Command Cable Driver Enable Cricuitry.
Drv_En.sch
Revision1.20
2/25/97
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