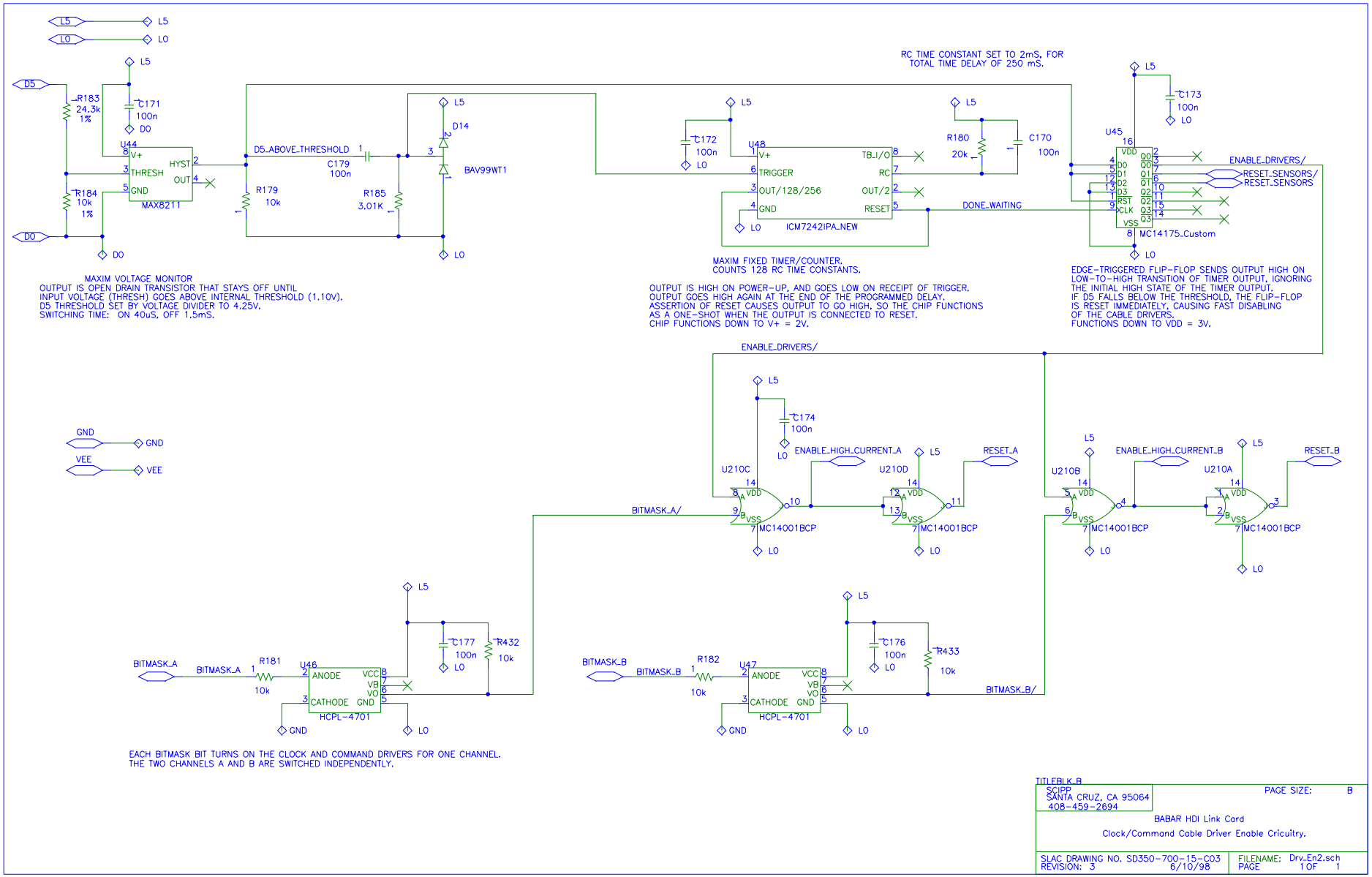
L5
L0
D5
R183
24.3k
1%
C171
100n
D0
U44
V+
THRESH
GND
HYST
OUT
R184
10k
1%
MAX8211
D5_ABOVE_THRESHOLD
C179
100n
R179
10k
R185
3.01K
D14
BAV99WT1
MAXIM VOLTAGE MONITOR
OUTPUT IS OPEN DRAIN TRANSISTOR THAT STAYS OFF UNTIL
INPUT VOLTAGE (THRESH) GOES ABOVE INTERNAL THRESHOLD (1.10V).
D5 THRESHOLD SET BY VOLTAGE DIVIDER TO 4.25V.
SWITCHING TIME: ON 40uS, OFF 1.5mS.
RC TIME CONSTANT SET TO 2mS, FOR
TOTAL TIME DELAY OF 250 mS.
C172
100n
U48
V+
TRIGGER
OUT/128/256
GND
ICM7242IPA_NEW
TB_I/O
RC
OUT/2
RESET
R180
20k
C170
100n
DONE_WAITING
MAXIM FIXED TIMER/COUNTER.
COUNTS 128 RC TIME CONSTANTS.
OUTPUT IS HIGH ON POWER-UP, AND GOES LOW ON RECEIPT OF TRIGGER.
OUTPUT GOES HIGH AGAIN AT THE END OF THE PROGRAMMED DELAY.
ASSERTION OF RESET CAUSES OUTPUT TO GO HIGH, SO THE CHIP FUNCTIONS
AS A ONE-SHOT WHEN THE OUTPUT IS CONNECTED TO RESET.
CHIP FUNCTIONS DOWN TO V+ = 2V.
C173
100n
U45
VDD
D0
D1
D2
D3
RST
CLK
VSS
Q0
Q1
Q2
Q3
MC14175_Custom
ENABLE_DRIVERS/
RESET_SENSORS/
RESET_SENSORS
EDGE-TRIGGERED FLIP-FLOP SENDS OUTPUT HIGH ON
LOW-TO-HIGH TRANSITION OF TIMER OUTPUT, IGNORING
THE INITIAL HIGH STATE OF THE TIMER OUTPUT.
IF D5 FALLS BELOW THE THRESHOLD, THE FLIP-FLOP
IS RESET IMMEDIATELY, CAUSING FAST DISABLING
OF THE CABLE DRIVERS.
FUNCTIONS DOWN TO VDD = 3V.
GND
VEE
C174
100n
ENABLE_HIGH_CURRENT_A
U210C
U210D
MC14001BCP
RESET_A
BITMASK_A/
ENABLE_HIGH_CURRENT_B
RESET_B
U210B
U210A
BITMASK_A
R181
10k
U46
ANODE
CATHODE
VCC
VB
VO
GND
HCPL-4701
C177
100n
R432
10k
BITMASK_B
R182
10k
U47
C176
100n
R433
10k
BITMASK_B/
EACH BITMASK BIT TURNS ON THE CLOCK AND COMMAND DRIVERS FOR ONE CHANNEL.
THE TWO CHANNELS A AND B ARE SWITCHED INDEPENDENTLY.
TITLEBLK_B
SCIPP
SANTA CRUZ, CA 95064
408-459-2694
PAGE SIZE: B
BABAR HDI Link Card
Clock/Command Cable Driver Enable Cricuitry.
SLAC DRAWING NO. SD350-700-15-C03
REVISION: 3 6/10/98
FILENAME: Drv_En2.sch
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