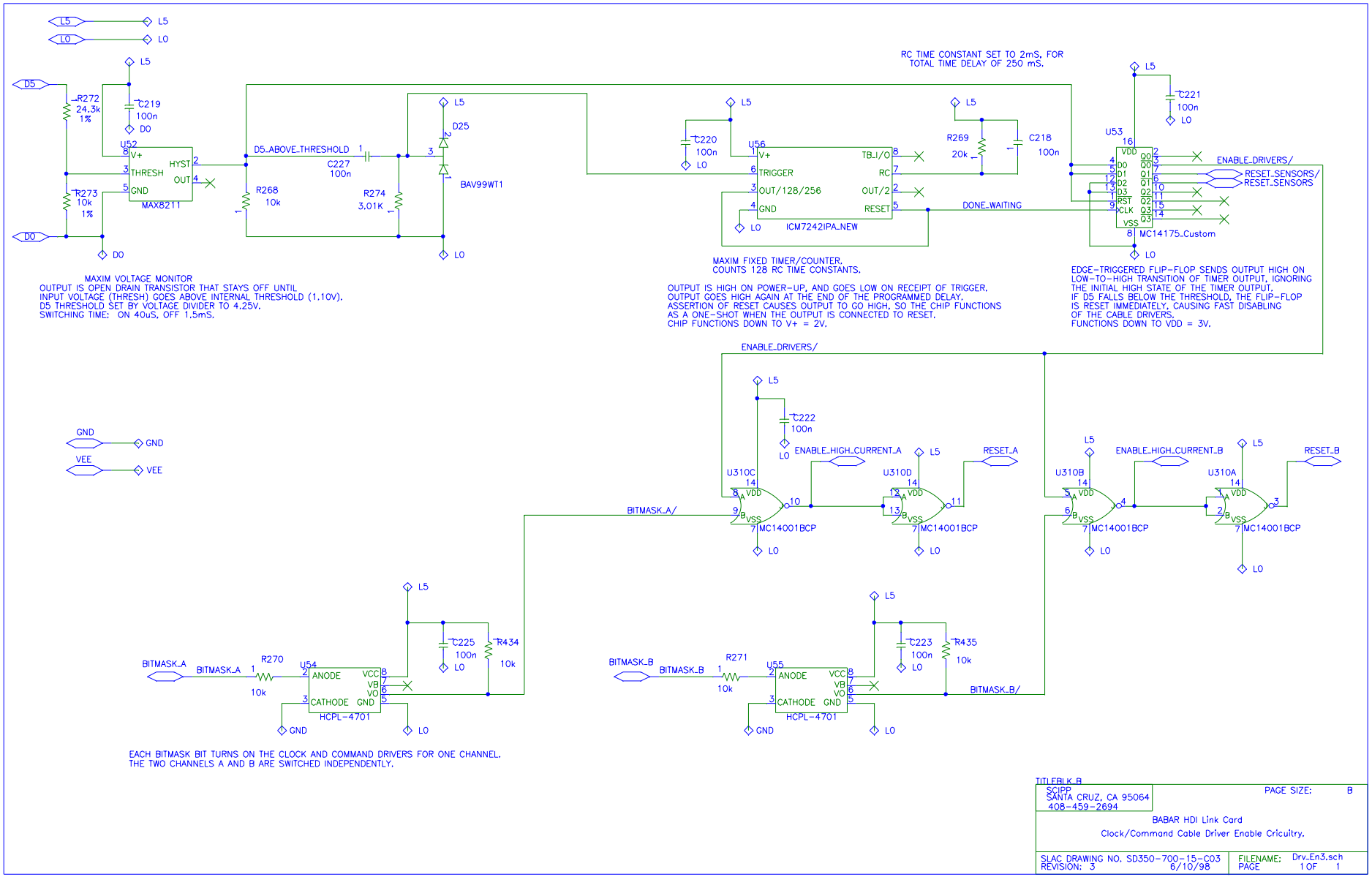
L5
L0
D5
R272
24.3k
1%
C219
100n
D0
U52
V+
THRESH
GND
HYST
OUT
MAX8211
R273
10k
1%
D5_ABOVE_THRESHOLD
C227
100n
R268
10k
R274
3.01K
D25
BAV99WT1
MAXIM VOLTAGE MONITOR
OUTPUT IS OPEN DRAIN TRANSISTOR THAT STAYS OFF UNTIL
INPUT VOLTAGE (THRESH) GOES ABOVE INTERNAL THRESHOLD (1.10V).
D5 THRESHOLD SET BY VOLTAGE DIVIDER TO 4.25V.
SWITCHING TIME: ON 40uS, OFF 1.5mS.
RC TIME CONSTANT SET TO 2mS, FOR
TOTAL TIME DELAY OF 250 mS.
C220
100n
U56
V+
TRIGGER
OUT/128/256
GND
TB_I/O
RC
OUT/2
RESET
ICM7242IPA_NEW
R269
20k
C218
100n
DONE_WAITING
MAXIM FIXED TIMER/COUNTER.
COUNTS 128 RC TIME CONSTANTS.
OUTPUT IS HIGH ON POWER-UP, AND GOES LOW ON RECEIPT OF TRIGGER.
OUTPUT GOES HIGH AGAIN AT THE END OF THE PROGRAMMED DELAY.
ASSERTION OF RESET CAUSES OUTPUT TO GO HIGH, SO THE CHIP FUNCTIONS
AS A ONE-SHOT WHEN THE OUTPUT IS CONNECTED TO RESET.
CHIP FUNCTIONS DOWN TO V+ = 2V.
U53
C221
100n
VDD
D0
D1
D2
D3
RST
CLK
VSS
Q0
Q1
Q2
Q3
ENABLE_DRIVERS/
RESET_SENSORS/
RESET_SENSORS
MC14175_Custom
EDGE-TRIGGERED FLIP-FLOP SENDS OUTPUT HIGH ON
LOW-TO-HIGH TRANSITION OF TIMER OUTPUT, IGNORING
THE INITIAL HIGH STATE OF THE TIMER OUTPUT.
IF D5 FALLS BELOW THE THRESHOLD, THE FLIP-FLOP
IS RESET IMMEDIATELY, CAUSING FAST DISABLING
OF THE CABLE DRIVERS.
FUNCTIONS DOWN TO VDD = 3V.
GND
VEE
ENABLE_DRIVERS/
C222
100n
ENABLE_HIGH_CURRENT_A
RESET_A
U310C
U310D
BITMASK_A/
MC14001BCP
ENABLE_HIGH_CURRENT_B
RESET_B
U310B
U310A
BITMASK_A
R270
10k
U54
ANODE
CATHODE
VCC
VB
VO
GND
HCPL-4701
C225
100n
R434
10k
BITMASK_B
R271
10k
U55
C223
100n
R435
10k
BITMASK_B/
EACH BITMASK BIT TURNS ON THE CLOCK AND COMMAND DRIVERS FOR ONE CHANNEL.
THE TWO CHANNELS A AND B ARE SWITCHED INDEPENDENTLY.
TITLEBLK_B
SCIPP
SANTA CRUZ, CA 95064
408-459-2694
PAGE SIZE: B
BABAR HDI Link Card
Clock/Command Cable Driver Enable Cricuitry.
SLAC DRAWING NO. SD350-700-15-C03
REVISION: 3 6/10/98
FILENAME: Drv_En3.sch
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