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Proposed Voltage Level Shifting Scheme for the SVT MUX Modules

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The following short write–up is intended to provide a description of the proposed level shifting scheme for the MUX Modules. A detailed description of the MUX Module and its functionality can be found in the PDR. In short, one module consists of the DAQ Link card and the HDI Link card where the voltage level shifting is located. One module services 4 HDI's (8 sides), thus 8 clock lines, 8 command lines, and 16 data lines, 32 channels in total. The system operates at a nominal clock frequency of 60 MHz.

The nominal voltage levels for the detector bias are ± 30 V for n– and p–side, respectively. The signals provided by the SVT DAQ system as well as the data sent back are at system level which is at the center tap of the detector bias voltage, whereas the front–end electronics is referenced to its respective bias voltage.

Several options have been considered to perform the necessary voltage translation of the clock, command, and data lines and are described in a previous note[1]. The options have been discussed in an internal 'mini–review' at SLAC on Dec 11th where it was agreed to further investigate only the possibilities of capacitive coupling (but not with the so–called chopper circuit as the timing restrictions are too tight) and optical coupling via LED's.

We propose a scheme based on capacitive coupling which is an improved version of the edge–sensing circuit presented in the previous note (called RS–Flip–Flop therein).

1 Description of the circuit

Figure 1 shows a rough sketch of the basic idea. The signals, differential PECL logic, are received by a line driver/receiver chip and sent through two capacitors in series (cf. safety discussion) to another receiver chip that has positive feed–back on both its inputs. Hence, the output stages of the second chip are bi–stable and consequently long strings of 1's and 0's that can occur on the command and data lines do not pose a problem to the circuit. The receiver switches polarity only if it receives a positive/negative going signal on its inputs.

[1]Available via anonymous ftp from `scipp.ucsc.edu` as `/pub/frey/level.ps`

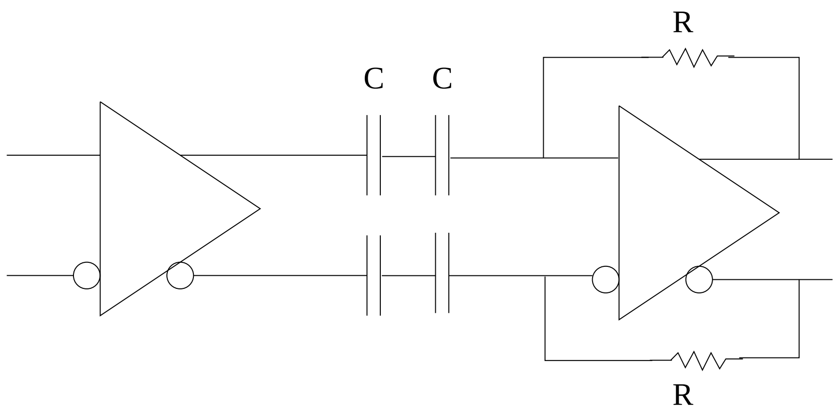

Figure 1: Basic sketch of the proposed ac–coupling scheme.

The actual schematic of the circuit is shown in fig. 2. For the clock and command channels, the 10114 ECL driver/receiver chips are used as buffers for the signals arriving at the HDI Link Card on the system level side, and as receivers with hysteresis on the HDI voltage level side. The capacitances are C = 80 pF (2×160 pF in series) and the feedback resistors have R = 100 Ω. For the signals, the chosen RC constant does not affect the shape, whereas common mode noise dies away with a time constant of RC = 8 ns which is just one half clock cycle. When the circuit is powered up and no signal provided on the input lines, the output state of the 10114 receiver is undefined. In order to overcome the problem that the receiver on the command line might come up in a logic high state and thus the first 0/1 transition be missed, the lines are reset to logic low on power up. This is done in the following way: A signal (Reset_Sensors) is derived from the power up sensing circuit that is logic high if the HDI power is below a given threshold (see fig. 3)[2]. This signal is applied to the base of a transistor that pulls the non–inverting input of the receiver low while Reset_Sensor is high. The transistor on the inverting line just serves the purpose of applying the same load on both lines.

The level shifting for the data lines is essentially the same except that instead of a 10114 ECL chip serving as the buffer for the signals coming from the AToM chips a AD9696 fast comparator chip with TTL logic is used. This is due to the fact that the 10114 chips require a minimum of 150 mV voltage swing between high and low whereas the AD9696 can handle signal swings as low as 50 mV. For a setting of the data output drivers of the AToM chip to 'low', we measured on our testboard

[2]The power sensing circuit was introduced to meet the requirement that the drivers have to be disabled on power up of the AToM front–end chips. For the sake of completeness fig. 3 shows the drivers for clock and command channels.

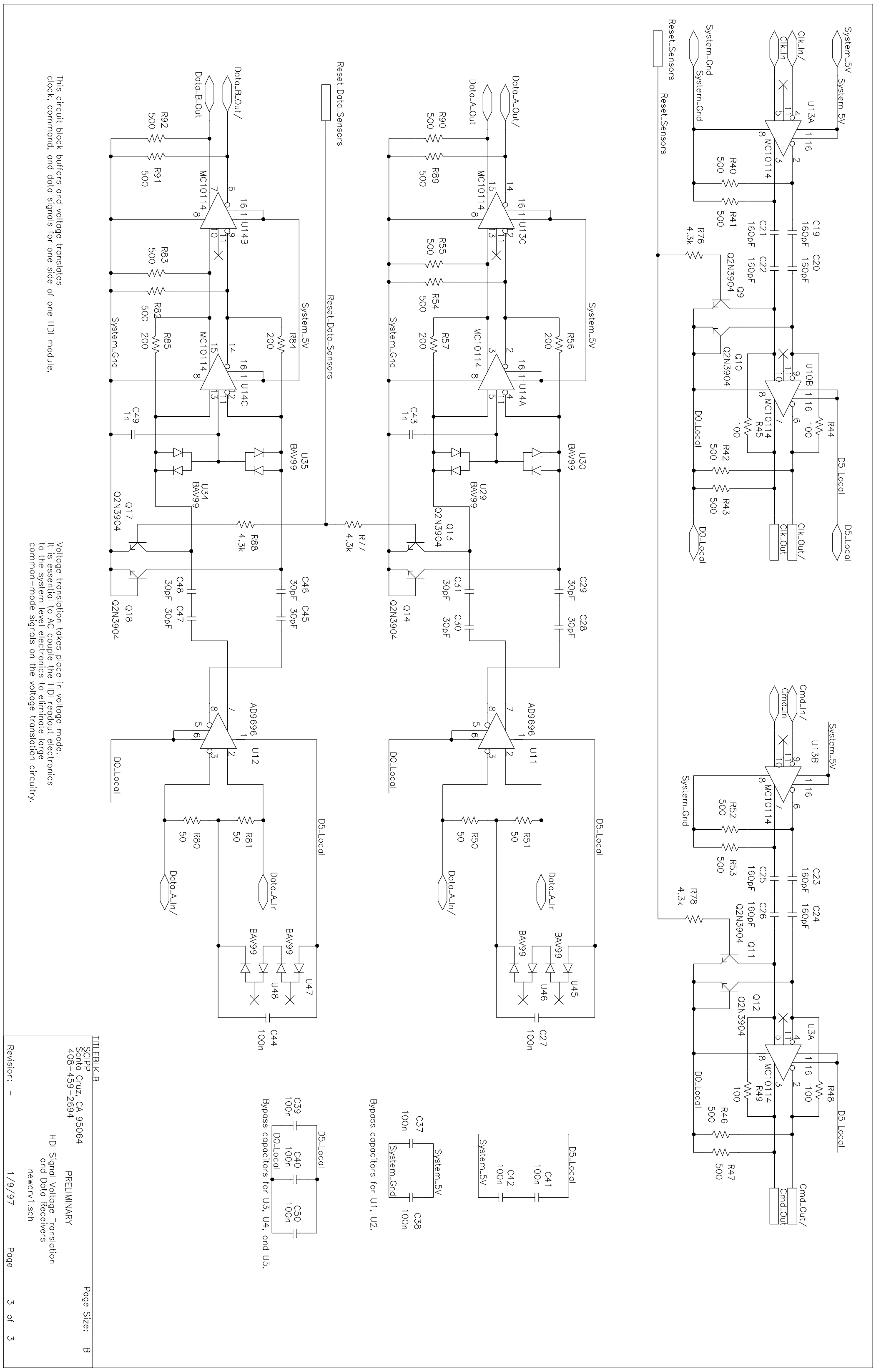

Figure 2: Schematic of the level shifting circuitry for clk/cmd (top) and data lines.

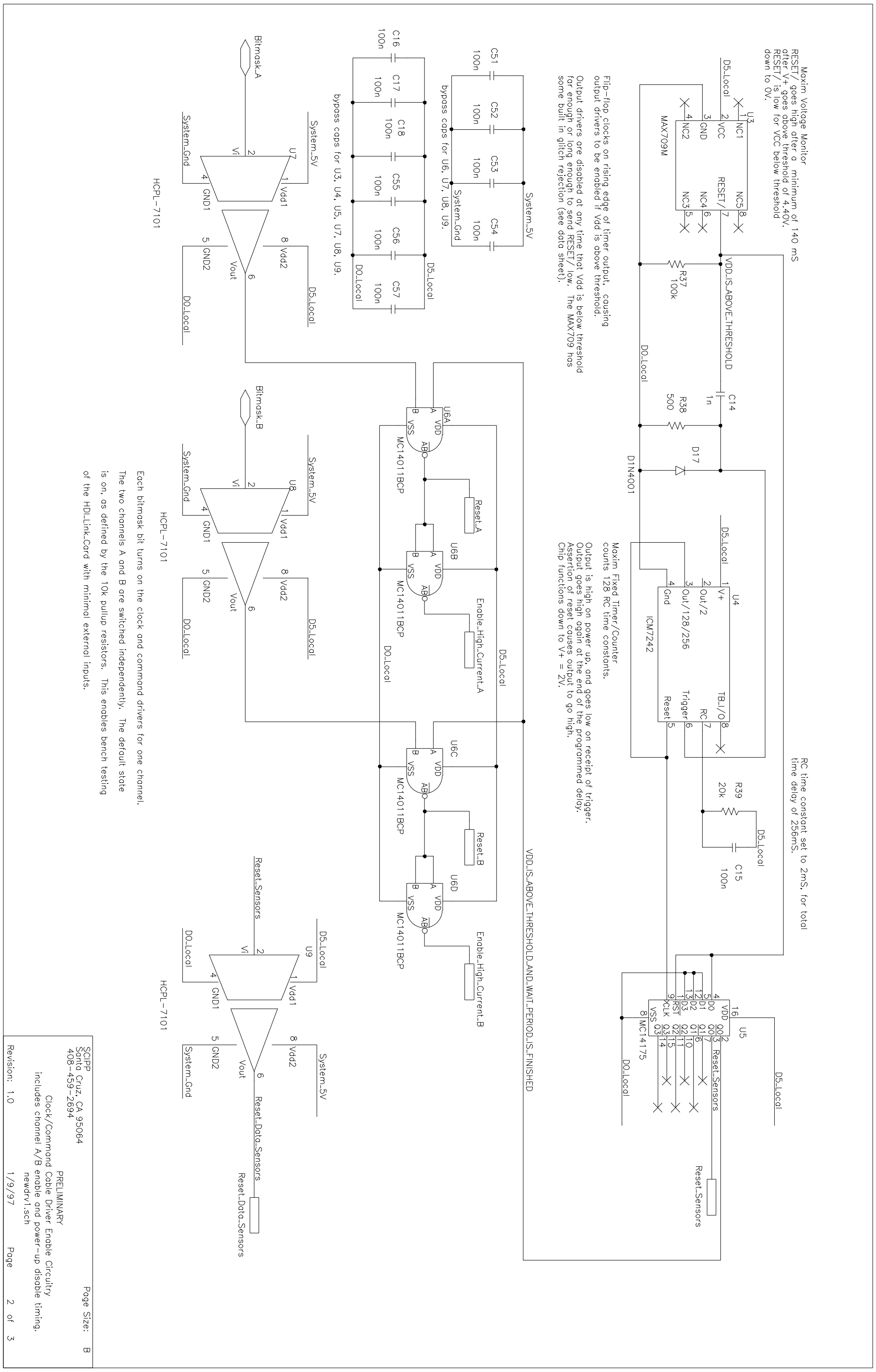

Figure 3: Schematic of the HDI power up sensing.

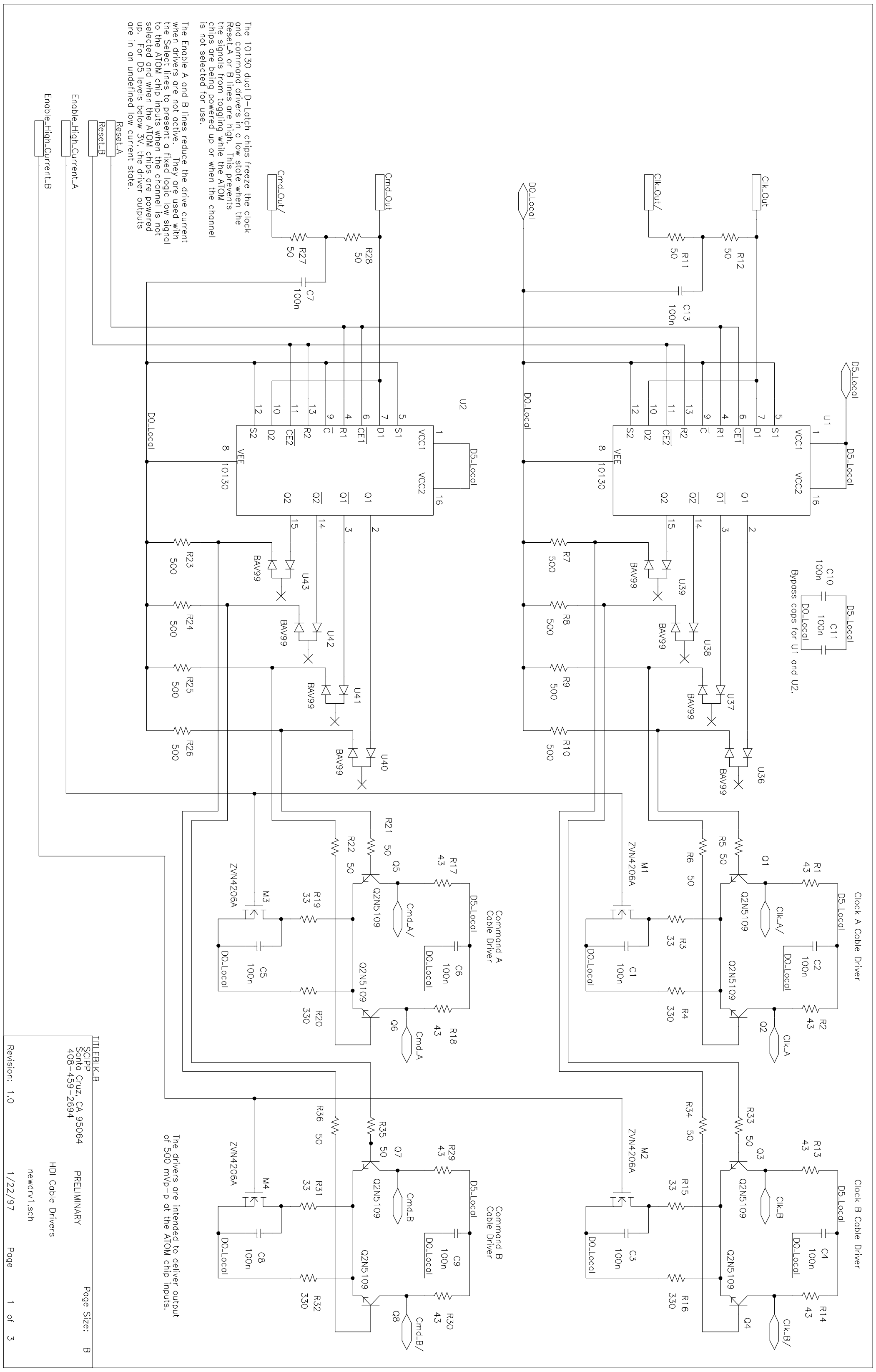

Figure 4: Schematic of the final clk/cmd drivers. The D–latch is used to freeze the outputs on power up.

a voltage swing of $\sim$ 230 mV single–ended. For an attenuation due to the 15 m cables of roughly a factor of three, the 10114 might not be able to hear the signal. The capacitance of the two series caps is less than for the clk/cmd lines in order to decrease the current draw of the AD9696 output stage. As mentioned before, this does not change the signal shape. Only for common mode noise suppression the RC time constant plays a rôle and is in this case even shorter (3 ns). However, because the AD9696 output runs at TTL levels, the voltage swing after the capacitors is $\sim$ 3.5 V. Therefore clamping diodes (C $<$ 1.5 pF) are used to restrict the voltage swing to one diode drop above and below the reference voltage of about 3.65 V of the 10114 receiving the data signal. For the data lines a second stage 10114 chip is used to drive the signals to the DAQ Link Card.

2 Performance

The level shifting scheme described above has been breadboarded and tested. The available bandwidth is larger than necessary, the system can run at a speed as high as 100 MHz. One data channel has been connected to the AToM testboard and worked without any problem.

Tests of the common mode rejection showed that the level shifting system is 'immune' against common mode noise of the order of $\pm$ 1 V. The feed–back resistors provide a path for common–mode noise, but suppressed by a factor of 10 and 20 for clk/cmd and data, respectively. Injecting a $\pm$ 1 V signal into the system resulted in a change of the outputs of just 80 mV (single ended, 20 mV differential), small compared to a ECL signal swing of 900 mV. For higher common mode noise, the high input might go above the +5 V rail causing the input protection diodes of the 10114 to turn on, and the reaction of the system output is not well defined.

Note that for good performance a local coupling of the +5 V rail at system and at HDI level is important. This is again for reasons of safety done with two capacitors in series.

If for some reason the output of the feed–back receiver misses a transition or switches state by mistake, the system recovers at the next transition, which can be either 1/0 or 0/1, but not immediately at the next bit. (It should be noted that also the LED level shifting scheme would have a similar error recovery behaviour, as the output of the LED receiver diode has to be ac–coupled to an amplifier with feed–back.)

3 Power consumption

Power consumption is a considerable issue as the specifications on the proposed power supply currents are rather tight. The proposed scheme is actually a very low power scheme as the 10114 chips as well as the AD9696 comparators were already part of the design and deployed as buffers and receivers. No additional chips are needed except for the second stage at the data channels, but those are not powered by the HDI power supplies. The table on the next page lists the currents per HDI side for the components working on the HDI voltage level for nominal and the worst case situations. Note that the current numbers for the final drivers are calculated for all four channels (`clk_a`, `clk_b` and `cmd_a`, `cmd_b`) being enabled. The nominal current draw with all four channels enabled is 480 mA, for worst case operation we estimate 530 mA which is 30 mA above the specifications in Mark Nyman's power spec document.

4 Safety and reliability

In this section only the coupling capacitors for the level shifting will be considered. A complete study of the reliability of the whole system will be available soon.

An extremely important task of the level shifting is to minimize the risk of the full bias voltage being applied to the front–end electronics. For this reason two capacitors in series, each one of them rated at 200 V, have been chosen rather than just one. If one of the capacitors fails short, the second one can withstand the voltage without any problem. This would introduce a capacitance asymmetry between the two differential lines. We verified that this does not affect the signal transmission, the only effect is a 1 ns shift in the timing of the signal. Thus, the failure of one capacitor does not cause a dead channel.

NovaCap provides reliability data on their capacitors, but unfortunately they never perform tests at voltages below the rated one and for temperatures below 125^oC, in fact they apply at least twice the rated voltage (they assume an acceleration factor of (applied voltage/rated voltage) to the third power for their quoted mean–time–before–failure).

In order to estimate the MTBF under the actual running conditions, the reliability prediction models of the MIL–HDBK–217F handbook have been used and it was checked that the predictions for high voltage and temperature are in the right order w.r.t the manufacturer's data.

Current draw of HDI Link Card circuitry per HDI side
(estimate includes only electronics at HDI potential)

device	number of devices/ HDI side	current per device nominal/ worst case (25^{o}C)	total current nominal	total current worst case
10114	1	58 mA/ 65 mA	58 mA	65 mA
10130	2	54 mA/ 64 mA	108	128
optocoupler output stage	2	5.5 mA/ 10 mA	11	20
optocoupler input stage	1	5.5 mA/ 10 mA	6	10
MC14175	1	$<$ 1 mA	1	1
MAX709M	1	$<$ 1 mA	1	1
ICM7242	1	$<$ 1 mA	1	1
2N3904	2	4 mA	8*	8*
AD9696	2	26mA/ 32 mA	52	64
cable driver subcircuit	4	60 mA	240**	240**
Total			478 mA	530 mA

* 2N3904s are turned on only when cable driver subcircuits are disabled.

** The cable driver subcircuits will draw a total of 24 mA when disabled.

Failure rates are calculated with the following model

$$\lambda = \lambda_b \cdot \pi_C \cdot \pi_Q \cdot \pi_E \ / \ 10^6 \text{ hours}$$

where λ_b is the basic failure rate, depending on the fraction S of applied to rated voltage and temperature as

$$\lambda_b = .0003 \left[\left(\frac{S}{.3} \right)^3 + 1 \right] \exp \left(\frac{T + 273}{398} \right)$$

for a device rated at $T_{max} = 125^o$C. The capacitance factor π_C is calculated as $\pi_C = .41 \cdot C^{0.11}$, for the quality factor we conservatively used $\pi_Q = 10$ ('lower') and $\pi_E = 2$ for a 'fixed environment'.

Total number of capacitors on all 26 MUX Modules :

— C = 160 pF on clk/cmd lines: 16×4 per module $\Longrightarrow$ $\Sigma = 1664$ caps

— C = 30 pF on data lines: 16×4 per module $\Longrightarrow$ $\Sigma = 1664$ caps

— C = 100 nF bypass caps: 16 per module $\Longrightarrow$ $\Sigma = 416$ caps

The voltage drop over both capacitors is conservatively taken to be 40 V which is equally distributed over the two caps. For the calculations a temperature of 40^oC was assumed (the MUX Modules will sit in water cooled crates). For continuous running the following failures rates per year (1 a = 8760 hours) are estimated:

Capacitors	failure rate/a	# of failures/a
160 pF	$8.62 \cdot 10^{-5}$	0.14
30 pF	$7.18 \cdot 10^{-5}$	0.12
100 nF	$1.74 \cdot 10^{-4}$	0.07
Sum		0.33

For the whole system of all MUX Modules we therefore estimate a reliability of only 1 failure in 3 years due to the coupling capacitors.

Concerning the safety issue for the AToM chips, one has to consider the probability that assuming one cap has failed short in a channel or in the bypassing, the other series capacitor in the same channel fails short, too. The voltage drop over the single cap is now the full 40 V and the probability of one given capacitor to fail is

- $1.08 \cdot 10^{-4}$/a for C = 160 pF
- $8.98 \cdot 10^{-5}$/a for C = 30 pF
- $2.17 \cdot 10^{-4}$/a for C = 100 nF

Putting aside the bypass caps given their very low total failure rate, the probability that after the failure of one coupling cap the front–end electronics will suffer the full bias voltage is 1:10000 per year continuous operation.

5 Conclusion

The proposed capacitive coupling scheme for the level shifting meets in our opinion the requirements concerning reliability, safety and performance. The obvious advantage over the transistor option, that was used on the first prototype card, is a much higher safety margin for the front–end. In addition, the inconvenient need to apply a minimum detector bias voltage in order to make the system work is eliminated.

Even though one might tend to think of the LED option as the genuinely 'cleanest' one, the proposed scheme has several advantages: The first is simplicity, the LED circuitry would essentially need the same components in addition to the LED transmitter and receiver diodes plus the LED driver circuit. The reliability of the LED diodes alone was estimated at 1 failure/year. The current budget of the capacitive coupling is the lowest of all options considered and much less than for the LEDs. Moreover, possible problems with the alignment of the LED diodes without the intended optical fiber between them are avoided. And last but not least the costs are very low for the capacitor scheme.