Interface Control Document

Between The

Version 2 TEM Board (Stanford) and the

Calorimeter Control Board (NRL)

Supporting the

GLAST Tower Beam Test

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NOTE: At this time, this is not strictly an interface control document but more a repository of useful information on the implementation of the calorimeter readout and the calorimeter TEM for the 1999 Beam Test. This includes both hardware and software issues relative to the operation of the calorimeter.

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1. Introduction:

This document describes the interface between the VME format TEM board Version 2 and the Calorimeter Control Board for the GLAST Beam Test. The calorimeter is a hodoscopic design consisting of 8 layers of 10 CsI scintillating crystals viewed by PIN photodiodes (see Figure 1). Each of the four sides of the calorimeter have front end electronics (FEE) circuit boards which support the capture and readout of energy losses in the 80 crystals. Each crystal is readout at both ends so that light ratios of the two ends can provide a position of the energy deposition along the length of the CsI crystal.

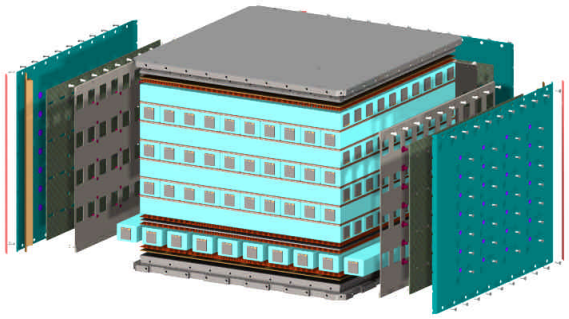

Figure 1. Beam Test Hodoscopic Calorimeter Design. Eight layers of 10 CsI crystals are held in a compression cell and read out by PIN photodiodes. This expanded view shows the printed circuit cards for the readout electronics and closeout shields on the side.

Each FEE board thus reads out one end of 40 CsI detectors. Each detector has a dedicated 12 bit ADC. Figure 2 shows schematically the flow of data from the calorimeter front-end electronics (FEE) into the DAQ. The figure shows the detail of one of the four sides of the calorimeter; the other three are similar. As seen in the figure, the 40 ADCs are organized into 5 columns of 8 ADCs. Each column or pipe transmits a serial stream to the DAQ.

The DAQ TEM board for the calorimeter accepts these 20 serial pipes (5 from each of 4 sides) and merges them into an event FIFO. Each ADC is represented by a 16-bit word. The TEM FIFO is loaded with pairs of ADCs, forming 32-bit words. Each trigger or digitization from the calorimeter creates 80 32-bit words in the FIFO containing ADC values. This list is preceded by a 32-bit trigger event number which identifies the trigger, a 32-bit trigger timer word, and a32-bit (13 useful) TREQ/Veto status word. After the 80 ADC values, a 32-bit deadtime measurement (18 useful bits) is appended. Thus 84 words are loaded into the event FIFO per digitization. In nominal operating mode for the calorimeter during the beam test, there will actually be 4 digitizations per trigger. These four digitizations are for the four energy domains supported by the front end electronics. In this case, 336 words will be loaded into the FIFO for each trigger.

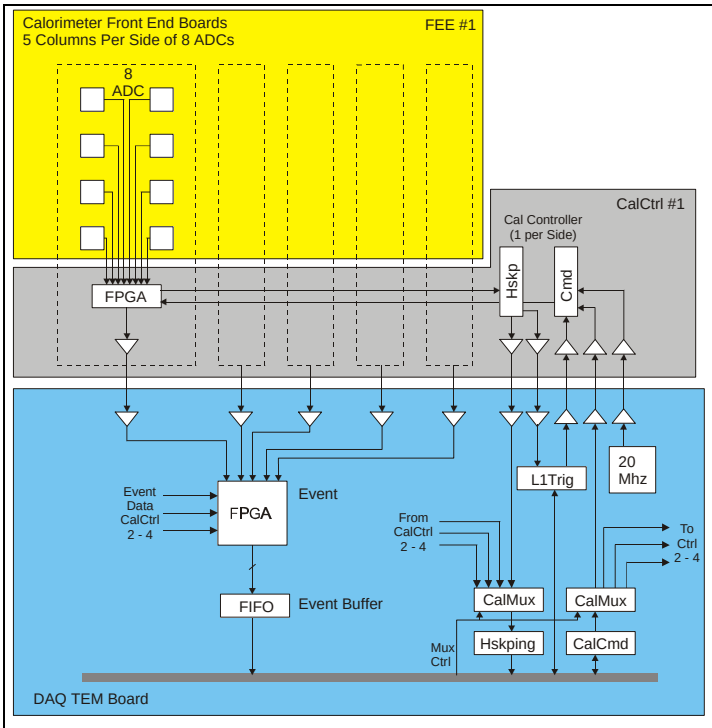

Figure 2. Organization of the Calorimeter Front End Electronics and DAQ TEM readout. The DAQ TEM communicates with 4 calorimeter controller boards – one per side of the calorimeter.

The Calorimeter TEM Board is a modified version of the Tracker TEM Board, and resides in a VME chassis. The Calorimeter Control Board resides under the calorimeter and controls one readout side of the

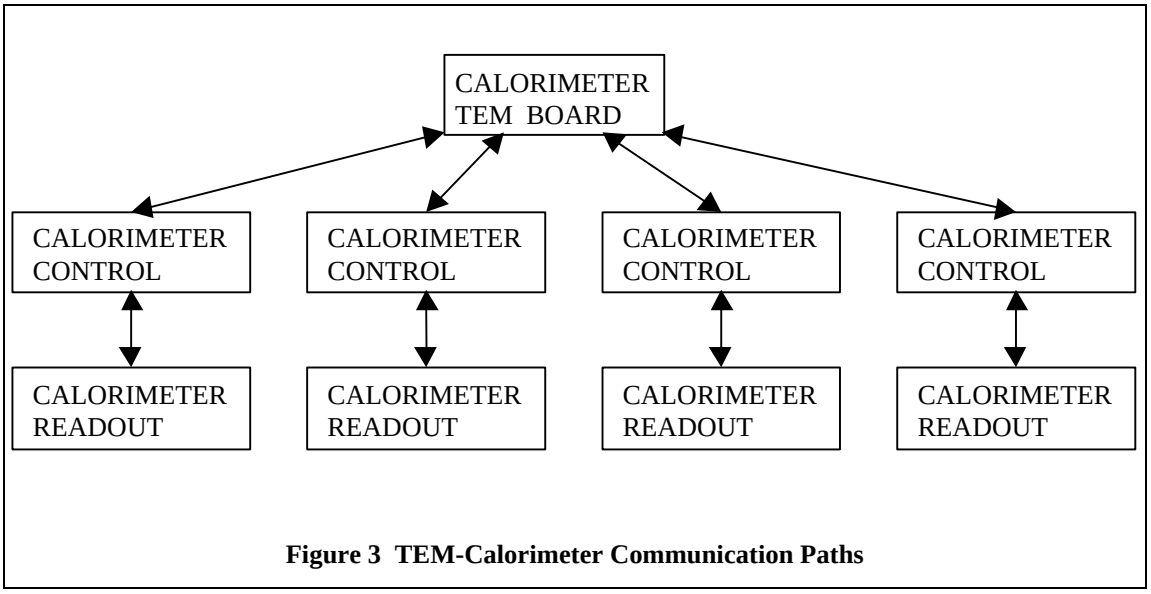

Figure 3 TEM-Calorimeter Communication Paths

calorimeter. Thus one TEM board communicates with four Calorimeter Control Boards. This is shown pictorially in Figure 3.

2. Wired Connections:

The main signal communications between the TEM and one calorimeter control is shown pictorially in Figure 4.

Communication of all signals is performed with Low Voltage Differential Signaling (LVDS). LVDS transmitters signal bits by changing the direction of a small output current. The LVDS receiver detects the change in voltage polarity across a resistor matched to the line. A common connector pinout is used between each of the Calorimeter Control Boards and the Calorimeter TEM Board. Note that the TEM board does not supply power to the Calorimeter.

The cable signal connections are shown in Table 1.

3. Communication Protocols

A 20 MHz clock distributed over the system is used for both transmitting and receiving messages. Data is

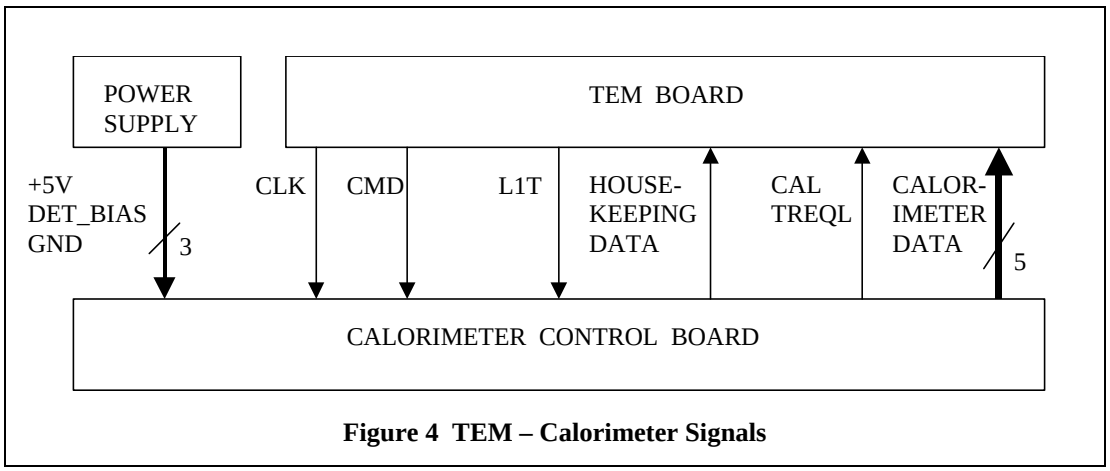

Figure 4 TEM – Calorimeter Signals

Table 1. Signal connections between TEM and Calorimeter

TEM Pin #	Cal Pin #	Description
	37	+5V
	36	+5V
	35	+5V
	34	+5V
	33	+PIN_Bias Voltage
	32	Bias Return
	31	Gnd
	30	Gnd
	29	Gnd
	28	Gnd
	27	Gnd
12	26	Data0_Hi
13	25	Data0_Lo
14	24	Data1_Hi
15	23	Data1_Lo
16	22	Data2_Hi
17	21	Data2_Lo
18	20	Data3_Hi
19	19	Data3_Lo

TEM Pin #	Cal Pin #	Description
20	18	Data4_Hi
21	17	Data4_Lo
22	16	SpareOut_Hi
23	15	SpareOut_Lo
24	14	CalReq_Hi
25	13	CalReq_Lo
26	12	Level1_Trig_Lo
27	11	Level1_Trig_Hi
28	10	Clk_Lo
29	9	Clk_Hi
30	8	Cmd_Lo
31	7	Cmd_Hi
32	6	HskpDat_Lo
33	5	HskpDat_Hi
34	4	Reset_Lo
35	3	Reset_Hi
	2	Gnd
	1	Gnd

transmitted on a rising clock edge and is received with the next rising clock edge. A delay may be inserted on the receiver clock circuit for correctly latching the data. Data is transmitted asserted LOW.

3.1. Event Data from the Calorimeter Control Board to the TEM Board:

Upon the receipt of a Level 1 Trigger signal from the TEM, the calorimeter initiates a digitization of all ADC channels. There are 40 ADCs per Calorimeter Control Board. The Calorimeter Control Board sends to the TEM the digitized pulse heights from all the calorimeter log ends. Each control board sends data simultaneously over 5 serial data lines (pipes). In normal operating mode, there is one digitized pulse height value per log end. Each pipe serially transmits a 128 bit (8 x 16) data packet as shown in Figure 5. All pipes transmit simultaneously.

For calibration mode, four pulse heights are readout per log end. This is implemented as essentially 4 separate transmissions of data in the format of Figure 5. The contents of the ADC will of course change as the energy range is sampled in the 4 digitizations and subsequent transmissions.

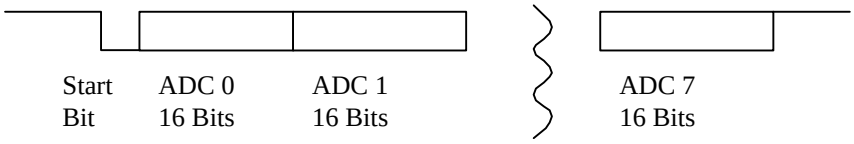

Figure 5. Normal data return mode.

Figure 6 indicates the organization of each 16-bit ADC values transmitted in the packet. The 12 bit ADC value is contained in the most significant bits. The remaining 4 bits encode the energy

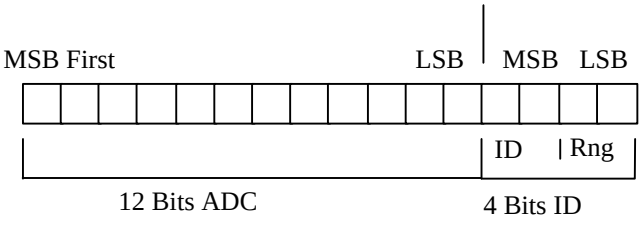

Figure 6. ADC data packet

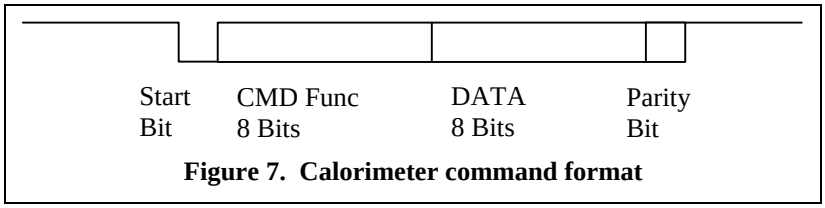

Figure 7. Calorimeter command format

range of the channel (least significant 2 bits) and a sequence number (ID, adjacent 2 bits) for the ADC.

3.2. Commands from the TEM board to the Calorimeter Control Board:

Commands are sent from the TEM to the Calorimeter for houskeeping functions and instrument mode settings. The format of the serial bit stream is shown in Figure 7. The TEM hardware adds the start bit and parity bit to a 16 bit value. Odd Parity bit is set by the hardware so that the base 2 summation of the command, data and parity bits is 1.

The TEM board has one command register for commanding the four calorimeter control boards. A multiplexor routes the serial data from the command register to the specified control board. The multiplexor is set by a control register (see Section 9) and must be set prior to writing the command in the TEM command register.

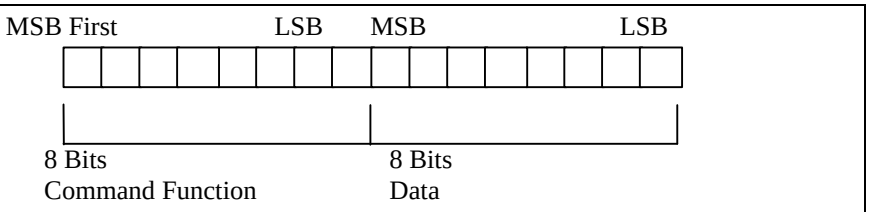

Figure 8. Command Word

The 16-bit command word is shown in Figure 8. The most significant 8 bits identify a command function code. The least significant 8 bits contain a data value to be set for the specified command function. Not all command functions require a data value in which case the data field is ignored. The parity bit is added by the TEM hardware. The command functions are defined in Section 0.

3.3. Command Response from the Calorimeter Control Board to the TEM Board:

Each command from the TEM board to the Cal Control Board results in a command response from the control board. The response consists of acknowledgements and optionally requested data. The length of the response message is variable, depending on command function. The acknowledgement is the repeated command function code and a status register as indicated in Figure 9. The command which requests the housekeeping readout of the rate counters results in a response of 41 16-bit words as shown in Figure 10,

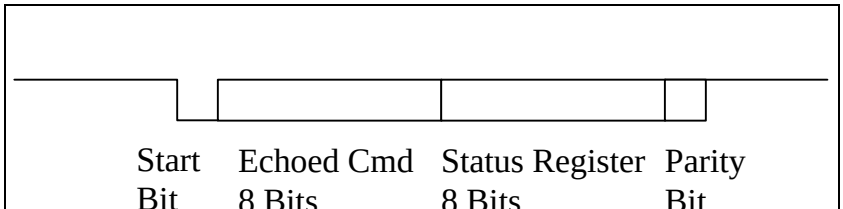

Figure 9. Command Return Format for Non Data Command

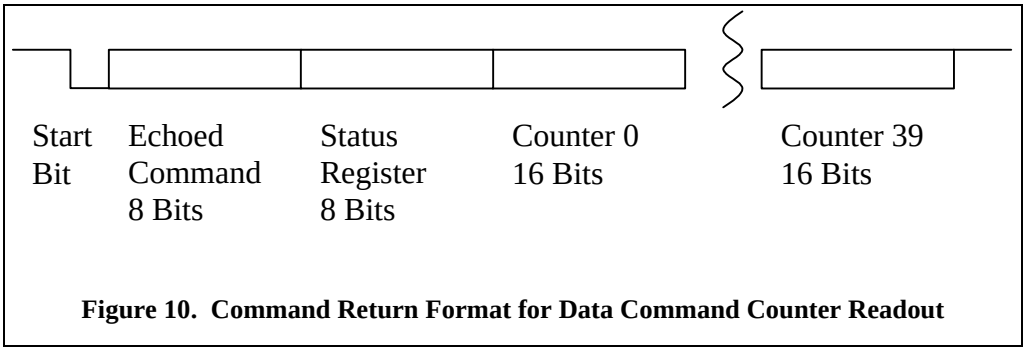

Figure 10. Command Return Format for Data Command Counter Readout

the acknowledgement and the 40 counter values..

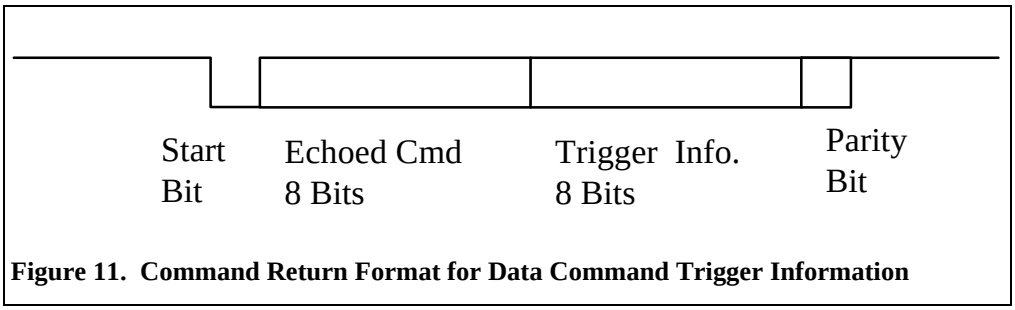

Figure 11. Command Return Format for Data Command Trigger Information

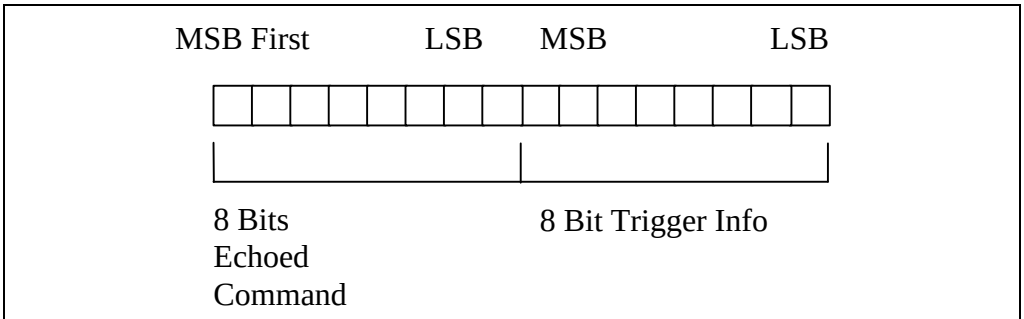

Figure 12 Command Return Word Format for Data Command Trigger Information

Table 2. Command Response Status Register Bits

Bit Position	Definition
0 LSB	Trigger Mode, See Table 4
1	
2	Data Readout Mode, See Table 5
3	
4	
5	Spare
6	Calorimeter Executed Command
7	Calorimeter Received Correct Parity

Table 3. Calorimeter Command Functions

Command Function, Hex	Command Description	Following Data Bits
00	Housekeeping Counters Readout	None
10	Load Input 0 Control Word	8 bit control word
11	Load Input 1 Control Word	8 bit control word
12	Load Input 2 Control Word	8 bit control word
13	Load Input 3 Control Word	8 bit control word
14	Load Input 4 Control Word	8 bit control word
20	Store DAC High Byte into Reg A	High Byte
21	Load DAC 0 Reg A + Low Byte	Low Byte
22	Load DAC 1 Reg A + Low Byte	Low Byte
23	Load DAC 2 Reg A + Low Byte	Low Byte
24	Load DAC 3 Reg A + Low Byte	Low Byte
30	Data Mode	3 bit data mode
40	Trigger Mode	2 bit trigger mode
50	Trigger Information 1, Rows	None
51	Trigger Information 2, Columns	None
60	Test Charge Injection	None
61	Pedestal Baseline Trigger	None
F0 - FF	Reserved pseudo commands to CAL TEM	

4. Commanding of the Calorimeter Control Board:

There are four control boards and associated front-end electronics boards (FEE). These four sides are labeled X-, X+, Y-, and Y+. See section 7 on the calorimeter coordinate system below. Table 3 summarizes the command functions recognized by the calorimeter control boards. The use of the command functions is discussed below. Commanding to the control boards utilizes the same TEM register for all four boards. A command can be sent to only one board per write to the command register. Consequently, a control register within the TEM must be set to select the appropriate control board for the command. Two bits in the control register set the command multiplexer to the desired cable. The physical wiring of the control boards to the TEM determine the relationship between multiplexer setting and addressed control board. The nominal definition of this relationship is CALMUX: 0 = X+, 1 = Y+, 2 = X-, 3 = Y-.

4.1. Housekeeping Counter Readout (0x00)

Each Cal control board contains 40 16-bit counters to monitor the threshold rate of each of the CsI log ends. The counters monitor the LowEn x4 lower level discriminator for each log; they are leading-edge triggered. The counters are active until receipt of the counter readout command. At that time, counting is disabled while the contents of all counters are transferred to output registers and the counters are cleared. Then counting resumes. The counter contents are transmitted to the TEM as described in section 3.3 (see Figure 10). The readout order of the 40 counters is summarized in section 9.15 (see Table 15).

4.2. Crystal Control Word Programming (0x10 – 0x14)

Each of end of the 80 CsI crystals can be individually enabled for trigger processing. These enables are organized in 5 control words, one per readout pipe, for each calorimeter control board. The 8-bit data portion of the control word command represents eight 1-bit enables for the 8 CsI crystals associated with that pipe.

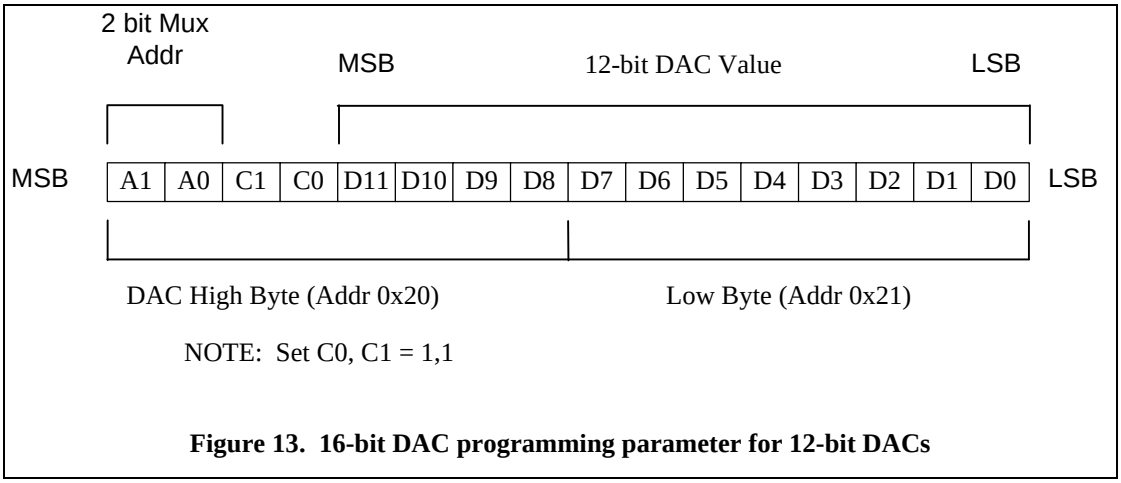

Figure 13. 16-bit DAC programming parameter for 12-bit DACs

4.3. DAC Programming Sequence (0x20 – 0x24)

Each Front End Electronics board contains 16 DACs to program ASIC discriminator levels, gain settings, and shaping time constants One quad DAC device provides four programmable DACs with 12-bit resolution over the voltage range 0 – 5.0 V. Three quad DAC devices provide 12 DACs with 10-bit
Table 4 defines the DAC functions and their addressing.

The 12-bit DACs are programmed thru two command functions: 0x20 – load dac high byte, and 0x21 – load dac0 low byte. In the programming sequence, the high byte command must preceed the low byte specification. Figure 13 identifies the organization of the required 16-bit DAC parameter specification into the data fields of the dac high byte and dac low byte commands. The high byte identifies which DAC in the quad unit and the most significant 4 bits of the 12-bit DAC value. The low byte defines the least significant 8 bits of the value. Bits C0 and C1 in the high byte should be set to 1,1.

The 10-bit DACs are programmed thru the same command function for the high byte, 0x20 – load dac high

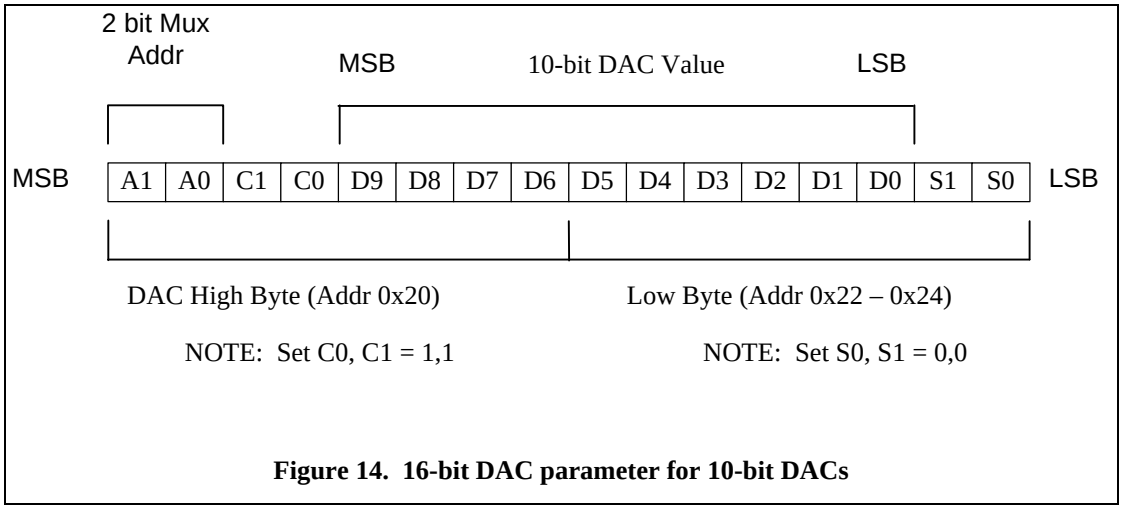

Figure 14. 16-bit DAC parameter for 10-bit DACs

byte, and one of three functions for the low byte, 0x22 – 0x24, load dac1 – dac3 low byte. In the programming sequence, the high byte command must preceed the low byte specification. Figure 14 identifies the organization of the required 16-bit DAC parameter specification into the data fields of the dac high byte and dac low byte commands. The high byte identifies which DAC in the quad unit and the most significant 4 bits of the 10-bit DAC value. The low byte defines the least significant 6 bits of the value. Note that the two LSBs of the low byte should be set to zero. Bits C0 and C1 in the high byte should be set to 1,1.

Table 4. Definition of DAC Mnemonics and Addresses

DAC Mnemonic	Description	Low Byte DAC Addr	DAC Mux Addr
DLEX4	LowEn x4 LLD ref (REFLLD), 12 bit	0x21	0
DFLE	Fast LowEn LLD ref (REFHF), 12 bit	0x21	1
DUL	ULD ref (REFULD), 12 bit	0x21	2
DFHE	FAST HiEn LLD ref (REFLF), 12 bit	0x21	3
TEST	Test Pulse Amplitude (VTDC)	0x22	0
ICNTRL	Current Threshold, CsICal (ICNTRL)	0x22	1
VICNTRL	Current Threshold, VICal (IV_CNTRL)	0x22	2
SPARE	Spare	0x22	3
GFLES	Fast LowEn Shaper Gain Cntrl (VGCFH)	0x23	0
GHES	HiEn Shaper Gain Cntrl (VGCL)	0x23	1
GHEX8S	HiEn x8 Shaper Gain Cntrl (VGC8L)	0x23	2
GFHES	Fast HiEn Shaper Gain Cntrl (VGCFL)	0x23	3
FBPA	Preamp feedback cntrl (VFBPA)	0x24	0
FBSA	Shaping amp feedback cntrl (VFC)	0x24	1
GLES	LowEn Shaper Gain Cntrl (VGCH)	0x24	2
GLEX4S	LowEn x4 Shaper Gain Cntrl (VGC4H)	0x24	3

4.4. Event Data Readout Mode Programming (0x30)

The calorimeter controllers support several selections for event data readout. The selection must be made prior to the level 1 triggers and is generally set once for an entire data run. There are two basic modes:

1. Readout all four gain ranges. In this mode there are four sequential readouts of the calorimeter, or, as described in section 7, 4×84 32-bit words. In this mode, there are four "sub-modes" which indicate whether the high energy channel should collect data with its test gain (hi gain mode) or its nominal gain. The other submodes control which of the energy ranges are readout first. See discussion below for the details. The test gain is useful for ground testing of the high energy channel using muons; it raises the gain of the high energy channel so that muons create a measureable signal.

2. Readout a single gain range. In this mode a single gain range is selected for readout. A single readout of 84 32-bit words is assembled in the TEM.

The 4-bit data values to specify the readout mode for the event readout mode command are listed in Table 5. Modes 6,7,14 and 15 specify various calibration readout modes that readout all four energy ranges. In this mode the readout appears as four events with identical event Ids. Energy range bits are encoded in the least significant 2 bits of each ADC value. As described in Table 5, these four modes include selection of test gains for the high energy range and readout sequence for the low and high gain channels. This ordering is important for test charge injection (see 4.7 below), since only the PIN associated with the 1st readout range receives the injected charge.

NOTE: *It is important that all four cal control boards are set to the same event readout mode. Otherwise the data handling software in the TEM will likely be confused and/or the TEM documentation of the event data will be incorrect or incomplete.*

Table 5. Data Readout Mode Bits

Data Readout Mode 4 Bit Value	Definition
0	Readout Low Energy Channel, x4 Gain
1	Readout Low Energy Channel, x1 Gain
2	Readout High Energy Channel, x8 Gain – Nominal
3	Readout High Energy Channel, x1 Gain - Nominal
4	Readout High Energy Chan, x8 Gain, - Test Gain (1pF preamp)
5	Readout High Energy Chan, x1 Gain, - Test Gain (1pF preamp)
6	Calibration Mode, Read all 4 Combinations (0,1,2,3)
7	Calibration Mode, Read all 4 Combinations (0,1,4,5)
8 - 13	Not normally used, same as 0 - 5
14	Calibration Mode, Read all 4 Combinations (2,3,0,1)
15	Calibration Mode, Read all 4 Combinations (4,5,0,1)

4.5. Calorimeter Trigger Mode Programming (0x40)

The calorimeter control boards support three modes for generating calorimeter triggers which are sent out to the TEM card for incorporation into the level 1 trigger. The trigger mode should be programmed prior to the starting of level 1 triggers. The trigger mode is programmed by a 2-bit data field in the trigger mode command. The specifications of this field and the associated trigger mode are identified in Table 6.

NOTE: *It is important that all four cal control boards are set to the same trigger mode. Otherwise the TEM documentation of the event data will be incorrect or incomplete.*

Table 6. Trigger Mode Specification

Trigger Mode 2 Bit Value	Defintion
0	Trigger on at least one hit in each of 3 adjacent rows (LowEn Fast)
1	Unassigned
2	Trigger on at least one hit in any row. (LowEn Fast)
3	LLD Muon Trigger (LowEnx4 LLD, 3.5 usec shaped)

4.6. Trigger Information Requests (0x50 and 0x51)

After the occurance of a trigger, trigger information request commands can be used to determine the detectors which generated the trigger. The information is returned in the command response data field in place of the 8-bit command status field. The definition of the responses are identified in Table 7. The 0x50 command interrogates trigger register 0 and the command, 0x51 interrogates register 1. The layers identified in the table are sequenced from top to bottom. For the X+ and X- sides, the sequence numbers represent layers 0,2,4,6; for the Y+ sides, the sequence numbers represent layers 1,3,5,7. (See section 7.)

Table 7. Trigger information bits

Bit Position	Reg 0 - Row – Description	Reg 1 – Col – Description
0 LSB	Row 0 (Top) “or”	Column 2 “or”
1	Row 1 “or”	Column 3 “or”
2	Row 2 “or”	Column 4 “or”
3	Row 4 (Bottom) “or”	Column 5 “or”
4	Adj side Row 0 “or”	Column 6 “or”
5	Adj side Row 1 “or”	Column 7 “or”
6	Column 0 “or”	Column 8 “or”
7	Column 1 “or”	Column 9 “or”

4.7. Test Charge Injection Request (0x60)

The calorimeter FEE boards provide test pulse generation for calibration and functionality testing. The test pulses are generated by first setting a pulse amplitude by setting a DAC value. The command, test charge injection request, then pulses that voltage into the test inputs to the FEE ASIC preamps. NOTE: Only one of the LowEn and HiEn preamps see the injected charge. The one that receives the charge is determined by the event readout mode pre-selected as described in section 4.4. For Event readout modes 0,1,6, and 7 the LowEn preamp receives the charge; for modes 2,3,4,5,14, and 15 the HiEn preamp receives the charge. The LowEn preamp is sees the injected charge on a 1 pF capacitor; the HiEn preamp is coupled with a 15 pF capacitor. There is one test charge injection per command.

NOTE: The test charge is injected into only one calorimeter controller at a time so that it is impossible to excite all four controllers in the same event.

4.8. Pedestal Baseline Trigger Request (0x61)

Causes a calorimeter trigger request without injecting a charge. One trigger occurs per command.

4.9. Resetting of the Calorimeter Controller Board.

The cal controller board reloads its Xilinx FPGA program upon Reset signal being asserted by the TEM. The cal controller is then in its initial power up state. Note that the calorimeter FEE boards DACs retain their current value through the reset process.

5. Calorimeter Command Scripting and Parsing

The commanding of the Calorimeter shall be supported by an ASCII command script parsing method which will permit “user-friendly” alphanumeric specification of commands without having to resort to the hexidecimal values for the commands. These ASCII command strings may be typed-in individually or be piped from a script file. The parsing language shall have the following features:

1. Enabling/disabling a log file of command requests and responses
2. Setting the default subsystem (eg. CAL, ACD, TKR, etc) for subsequent commands. On initialization, the subsystem is assumed to be CAL. At this time, the code will only support CAL commanding.
3. Setting the default calorimeter controller mux address for subsequent commands
4. Parsing commands of the form:
   <subsystem> <calmuxcode> <cmdmnem> <cmddatavalue> <; optional comments>, for example

   ```
   CAL X+ DAC LowEnx4 100.0  ; set threshold to 100 mv
   ```

   Both of the <subsystem> and <calmuxcode> may be omitted. In that case, the default values for those parameters will be inserted in the command. The default values are defined using a “SET” command.

NOTE: If a command specifies the <subsystem> or <calmuxcode> prefix, this value becomes the

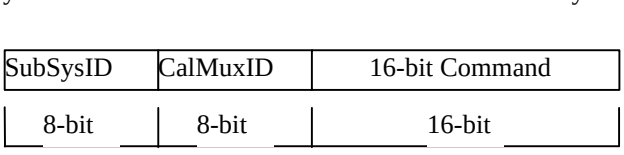

Figure 15. 32-bit format of Commands to the TEM command processor. SubsysID identifies CAL command and is zero. The least significant two bits of CalMuxID field set the cal control board mux.

default for all subsequent commanding until changed again by another prefix or by the SET commands.

Commands to the calorimeter shall be sent as 32-bit binary codes. The least significant 16 bits contain the 16-bit command function and associated data as described in section 4. The most significant 16-bits specify the calorimeter control card and subsystem (eg. CAL). This is shown in Figure 15

Table 8. Calorimeter Command Mnemonics – Command Parsing Environment

Command	Modifier	Data	Comment
SET	SUBSYSTEM	CAL	Subsequent commands go to calorimeter. This is initialized default
		{ACD, TKR, …}	Alternate subsystem specs
SET	CALMUX	{X+, X-, Y+, Y-, 0 - 3}	Set the command mux to the specified control board. Subsequent commands without calmuxcode will use this spec
SET	LOGFILE	<filename>	Close any open logfile and open new log as file <filename>
SET	LOGFILE	OFF	Close any open logfile (obviously, can't create logfile named OFF)

Table 9. Calorimeter Command Mnemonics - TEM Configuration

Command	Modifier	Data	Comment
RESET	None	None	Performs TEM card reset of calorimeter controllers and FIFOs. Use pseudo Cmdfunc = 0xF0
RESET	FIFO	None	Performs TEM card reset of FIFO and TEM FPGAs only. Use pseudo Cmdfunc = 0xF1
RESET	TRIGCNT	None	Performs TEM card reset of trigger counter register. Use pseudo Cmdfunc = 0xF2
L1T		{ON, OFF}	Enable/disable TEM recognition of Level 1 trigger inputs. Use pseudo Cmdfunc = 0xF3
CTREQ		{ON, OFF, 0x0 – 0xF)	Enable, disable or selectively enable the cal trigger req from the four controller cards. Hex values 0x0 – 0xF mask sides individually. ON = 0x0, OFF = 0xf. These are mask bits. Use pseudo Cmdfunc = 0xF4
STARTBIT		{X+,Y+, X-,Y-, 0 - 3}	Sets the TEM startbit mux to the specified controller card. Use pseudo Cmdfunc = 0xF5
CMUX		{X+, Y+,X-,Y-, 0 - 3}	Sets the TEM command mux to the specified controller card. Use pseudo Cmdfunc = 0xF6. Not normally used. Calmux setting (0xF6) will precede all parsed commands which address a specific controller

Table 10. Calorimeter Command Parsing - Commands to the Cal Controllers

Command	Modifier	Data	Comment
RATES			Readout rates from specified controller. Cmdfunc = 0x00. NOTE: this is useful for test only. TEM process normally acquires and transmits rates at fixed frequency.
CONTROL	<pipeid=0-4>	{0x00 – 0xFF)	8 1-bit trigger discriminator enables. (also enables singles rate counting) Cmdfunc = 0x10 – 0x14 MSB controls ASIC0, LSB for ASIC7 of pipe
DAC	{<dacmnem>, 0 – 15} See Table 4 for the mnem. Definitions	Dac value in millivolts or hex setting (0xnnn)	Set specified dac to value. Creates correct sequence of 0x20 – 0x24 cmds.
EVENT		{0 - 15}	Set event data readout mode. Cmdfunc = 0x30. NOTE: TEM software sends this same command to all four controllers.
TRIGGER		{0,2,3}	Set trigger generation mode. Cmdfunc = 0x40. NOTE: TEM software sends this same command to all four controllers.
INFO		<register id, 0, 1)	Get the trigger information bits on last trigger from specified controller: Cmdfunc = 0x50, 0x51 NOTE: this is useful for test only.
PULSE		<number of pulses, {0 – 255}	Inject a test charge pulse for the specified controller. Cmdfunc 0x60. Optional specification of number of pulses in data field. If not present, inject one pulse. TEM software will repetitively inject pulses at 1 ms intervals for the specified number.
PEDESTAL		<number of pulses, {0 – 255}	Create single trigger without injecting test charge for the specified controller. Cmdfunc 0x61.

The commands to the Cal TEM are allocated command function opcodes in the calorimeter controller command space. These commands have opcodes in the range 0xF0 – 0xF1. These command opcodes will be trapped in the TEM and not passed on to the calorimeter controllers. Similarly, the TEM command processor will guarantee that all four cal controllers operate in the same event data mode and trigger mode by sending any received command with those opcodes to all four controllers.

6. Level 1 Trigger Support

6.1. Calorimeter Trigger Generation

The TEM board has 4 differential inputs reserved for trigger requests from the calorimeter(Cal Req), and will generate a single calorimeter tower trigger (Level 1 Trigger) when any of the four input triggers are asserted. All trigger lines are asserted low. The calorimeter controller boards, individually, perform the logic required for determining a Cal Request trigger depending on the trigger mode selection (see section 0). The Cal Request trigger should be generated within 200 nsec of an event occuring and will be of minimum of 200 nsec in width. The maximum width of the Cal Request trigger is the time-over-threshold

```
> ; everything after the semicolon is comment
> ; parser is not case sensitive – upper and lower case are the same.
> set logfile mylog990728.log   ; turns on logging to specified file
> set subsys cal                ; sets default subsystem to calorimeter
> reset                         ; resets the calorimeter controller
> cal reset                     ; same as above but with subsystem identified
> X+ dac FLE  100.0             ; set X+ fast low energy threshold to 100 mV
> set calmux X+                 ; default controller is X+
> dac FLE 100.0                 ; set X+ fast low energy thresh to 100 mV
> dac FLE 0x100                 ; set X+ fast low en thresh to level 100 hex.
> dac pulse 500.0               ; set dac for test pulse amplitude to 500 mV
> pulse  1                      ; inject 1 test pulse into all controllers
> pulse   100                   ; inject 100 test pulses at 16 msec intervals.
```

Figure 16. Example Command Script.

of the analog signal. Additional information on the last calorimeter trigger request is obtained by using the Trigger Information command.

NOTE: *If the calorimeter trigger mode is set to the ground test configuration (3) for triggering on muons on the LowEn x4 LLD, the CalReq cannot be assured within the 200-nsec spec above. The slow shaping of the signal precludes that possibility. The CalReq in that configuration could be delayed by as much as 3.5 msec*

NOTE: *While the V2 TEM board supports both Cal High and Cal Low trigger requests, the prototype calorimeter controllers only support the Cal Low trigger. There are no connections to the Cal Hi trigger request lines.*

6.2. GLAST Level 1 Trigger:

The TEM board will have 4 differential outputs to communicate to each calorimeter side that a Level 1 Trigger event has occurred. The TEM board will generate a Level 1 Trigger within 500 nsec of receiving a calorimeter tower trigger. The Level 1 Trigger will then iniate calorimeter data readout.

NOTE: *The four calorimeter control boards must receive the Level 1 Trigger signal simultaneaously as determined by its detection on all four boards by the rising edge of the same 20 MHz clock pulse. If this simultaneity is not met, the 20 serial event readout will not be correctly phased and the TEM assembly of the event data will be corrrrupted corrupted.*

7. Calorimeter Readout Organization:

The readout of all 4 sides of the calorimeter will be arranged in a manner to simplify the processing of data by dowstream processors.

7.1. Calorimeter Coordinate System.

The Calorimeter has readout electronics on all four side faces. Opposing sides readout the two ends of the same CsI logs. The coordinate system for calorimeter readout discussions is the following:

Table 11. Coordinate System Definition

Z-Axis:	Points outward to the on-axis target position ("the viewing direction"), normal to the plane formed by the top layer of calorimeter logs
X-Axis:	At this point, arbitrary. By definition, the top layer of logs in the calorimeter have their long dimension parallel with this axis.
Y-Axis:	At this point, arbitrary, but forming "right-handed" coordinate system with X & Z. On the S/C it is likely to be aligned with the solar panel rotation axis

7.2. CsI Event Data Readout

The event data readout is organized by side face. Each side face supports the readout of 40 CsI log ends. The Front-End Electronics (FEE) control reads out the data in 5 "Pipes" per side. Each Pipe handles 8 ADC values which are readout in defined sequence, as shown in Figure 3. The sequence and sequence

Table 12. Organization of Event Data from FPGA. Sixteen bits per log end.

MSBit			LSBit
ADC Value 12 Bits	ADC ID 2 bits	PIN ID 1 Bit	Range Scale 1 Bit
	Sequence # mod 4	0 = Big Pin 1 = Sml Pin	0 = amplified rng 1 = full scale

number encoded in the 16-bit data value per ADC as shown in Table 6.

The faces of the calorimeter are identified by a two-character coordinate of the face: X+, X–, Y+, and Y–. The X+ electronics, for example, reads out the ends of the logs, aligned along the X- axis, at their +X end.

The data are readout in columnar sequence always starting at the top (+Z) and working to the bottom. The columns are readout from the "negative edge" to the "positive edge". That is, the X+,X– faces readout from the edge in the Y– direction to the Y+ edge, and the Y+, Y– faces readout from the edge in the X– direction to the X+ direction. This readout sequence is reflected in the numbering scheme for the CsI log ends which is defined in **Error! Reference source not found.** and shown graphically in Figure 17. The log end and ADC is identified by 8-bit Hex value. The most significant bit identifies the log end (0 = + face, 1 = – face).

The readout sequence for the four faces of the calorimeter is identified in Table 13. Refer to Figure 17 for geometric arrangement of the ADC Ids. In general, the faces readout from top to bottom but the column order is different for the faces. For the X+ face and the Y- face, the columns readout from left to right. For the X- face and the Y+ face, the columns readout from right to left. This ordering permits the assembly of the ADC values from the two ends of each CsI log into a single 32-bit word. This ordering is achieved first in the calorimeter controller by reading the 8 ADCs in the five pipes in the correct order, and then by the TEM FPGA accessing the data from the 20 pipes (5 pipes per side of the calorimeter in the correct order). The pipes are numbered from left to right on the FEE cards and reflect the connector number to the cal controller card.

Table 13. ADC Readout Order for Event Data

Pipe ID	Seq No.	Event Readout ADC ID			
		X+ Face	Y- Face	X- Face	Y+ Face
0	0	00	81	C0	41
	1	02	83	C2	43
	2	04	85	C4	45
	3	06	87	C6	47
	4	08	89	C8	49
	5	0A	8B	CA	4B
	6	0C	8D	CC	4D
	7	0E	8F	CE	4F
1	0	10	91	B0	31
	1	12	93	B2	33
	2	14	95	B4	35
	3	16	97	B6	37
	4	18	99	B8	39
	5	1A	9B	BA	3B
	6	1C	9D	BC	3D
	7	1E	9F	BE	3F
2	0	20	A1	A0	21
	1	22	A3	A2	23
	2	24	A5	A4	25
	3	26	A7	A6	27
	4	28	A9	A8	29
	5	2A	AB	AA	2B
	6	2C	AD	AC	2D
	7	2E	AF	AE	2F
3	0	30	B1	90	11
	1	32	B3	92	13
	2	34	B5	94	15
	3	36	B7	96	17
	4	38	B9	98	19
	5	3A	BB	9A	1B
	6	3C	BD	9C	1D
	7	3E	BF	9E	1F
4	0	40	C1	80	01
	1	42	C3	82	03
	2	44	C5	84	05
	3	46	C7	86	07
	4	48	C9	88	09
	5	4A	CB	8A	0B
	6	4C	CD	8C	0D
	7	4E	CF	8E	0F

The TEM shall assemble the 20 pipes into a data message of 81 32-bit words. The word ordering and content are described in Table 14 below. In the calorimeter readout mode in which all four energy ranges are readout, they appear as four sequential messages of the format in Table 14 with identical 32-bit Event ID in word 0. The messages appear in the order: LowEn x4, LowEn, HiEn x8, Hi En.

NOTE: *The V2 TEM card does not implement this order. Calorimeter software executing in the TEM PPC reorders the FIFO data to achieve this ordering.*

Table 14. ADC Readout Order in TEM 84 Word Event Message

Seq No.	32-bit Word Content		Data Source*	
	High 16-bit	Low 16-bit	High 16-bit	Low 16-bit
0	32-bit Event ID		TEM Event Counter	
1	32-bit Timer Word		TEM Event Trigger Time	
2	32-bit TREQ/VETO status		TEM Event Treq/Veto/Status	
3	ADC 00	ADC 80	X+, 0, 0	X-, 4, 0
4	ADC 10	ADC 90	X+, 1, 0	X-, 3, 0
5	ADC 20	ADC A0	X+, 2, 0	X-, 2, 0
6	ADC 30	ADC B0	X+, 3, 0	X-, 1, 0
7	ADC 40	ADC C0	X+, 4, 0	X-, 0, 0
8	ADC 01	ADC 81	Y+, 4, 0	Y-, 0, 0
9	ADC 11	ADC 91	Y+, 3, 0	Y-, 1, 0
10	ADC 21	ADC A1	Y+, 2, 0	Y-, 2, 0
11	ADC 31	ADC B1	Y+, 1, 0	Y-, 3, 0
12	ADC 41	ADC C1	Y+, 0, 0	Y-, 4, 0
13	ADC 02	ADC 82	X+, 0, 1	X-, 4, 1
14	ADC 12	ADC 92	X+, 1, 1	X-, 3, 1
15	ADC 22	ADC A2	X+, 2, 1	X-, 2, 1
16	ADC 32	ADC B2	X+, 3, 1	X-, 1, 1
17	ADC 42	ADC C2	X+, 4, 1	X-, 0, 1
18	ADC 03	ADC 83	Y+, 4, 1	Y-, 0, 1
19	ADC 13	ADC 93	Y+, 3, 1	Y-, 1, 1
20	ADC 23	ADC A3	Y+, 2, 1	Y-, 2, 1
21	ADC 33	ADC B3	Y+, 1, 1	Y-, 3, 1
22	ADC 43	ADC C3	Y+, 0, 1	Y-, 4, 1
23	ADC 04	ADC 84	X+, 0, 1	X-, 4, 1
24	ADC 14	ADC 94	X+, 1, 1	X-, 3, 1
25	ADC 24	ADC A4	X+, 2, 1	X-, 2, 1
26	ADC 34	ADC B4	X+, 3, 1	X-, 1, 1
27	ADC 44	ADC C4	X+, 4, 1	X-, 0, 1
28	ADC 05	ADC 85	Y+, 4, 1	Y-, 0, 1
…….	…….	…….	…….	…….
70	ADC 2D	ADC AD	Y+, 2, 6	Y-, 2, 6
71	ADC 3D	ADC BD	Y+, 1, 6	Y-, 3, 6
72	ADC 4D	ADC CD	Y+, 0, 6	Y-, 4, 6
73	ADC 0E	ADC 8E	X+, 0, 7	X-, 4, 7
74	ADC 1E	ADC 9E	X+, 1, 7	X-, 3, 7
75	ADC 2E	ADC AE	X+, 2, 7	X-, 2, 7
76	ADC 3E	ADC BE	X+, 3, 7	X-, 1, 7
77	ADC 4E	ADC CE	X+, 4, 7	X-, 0, 7
78	ADC 0F	ADC 8F	Y+, 4, 7	Y-, 0, 7
79	ADC 1F	ADC 9F	Y+, 3, 7	Y-, 1, 7
80	ADC 2F	ADC AF	Y+, 2, 7	Y-, 2, 7
81	ADC 3F	ADC BF	Y+, 1, 7	Y-, 3, 7
82	ADC 4F	ADC CF	Y+, 0, 7	Y-, 4, 7
83	32-bit Dead cause/time		TEM Event Dead cause/time	

* The data source is identified as side (eg. X+), pipe id, and ADC sequence in that pipe.

TEM STAT/TREQ/VETO Word:

Bit	Definition
12	Cal Readout mode 640/160, High = 640
11	Readout busy: Max (High, non-pipelined), Min (Low, pipelined)
10	ACDL Veto
9	CPU TREQ
8	EXT TREQ
7	CAL TREQH 3
6	CAL TREQH 2
5	CAL TREQH 1
4	CAL TREQH 0
3	CAL TREQL 3
2	CAL TREQL 2
1	CAL TREQL 1
0	CAL TREQL 0

TEM Dead Time Cause/Dead Time Word:

Bit	Definition
17	Readout L1T Wait
16	CPU Busy
15	Data FIFO Full
14	Cal Readout Busy
13 - 0	Dead Time Counter (50 nsec)

***NOTE**: In calorimeter readout mode of all four ranges (640), only the last range readout has correct deadtime information.*

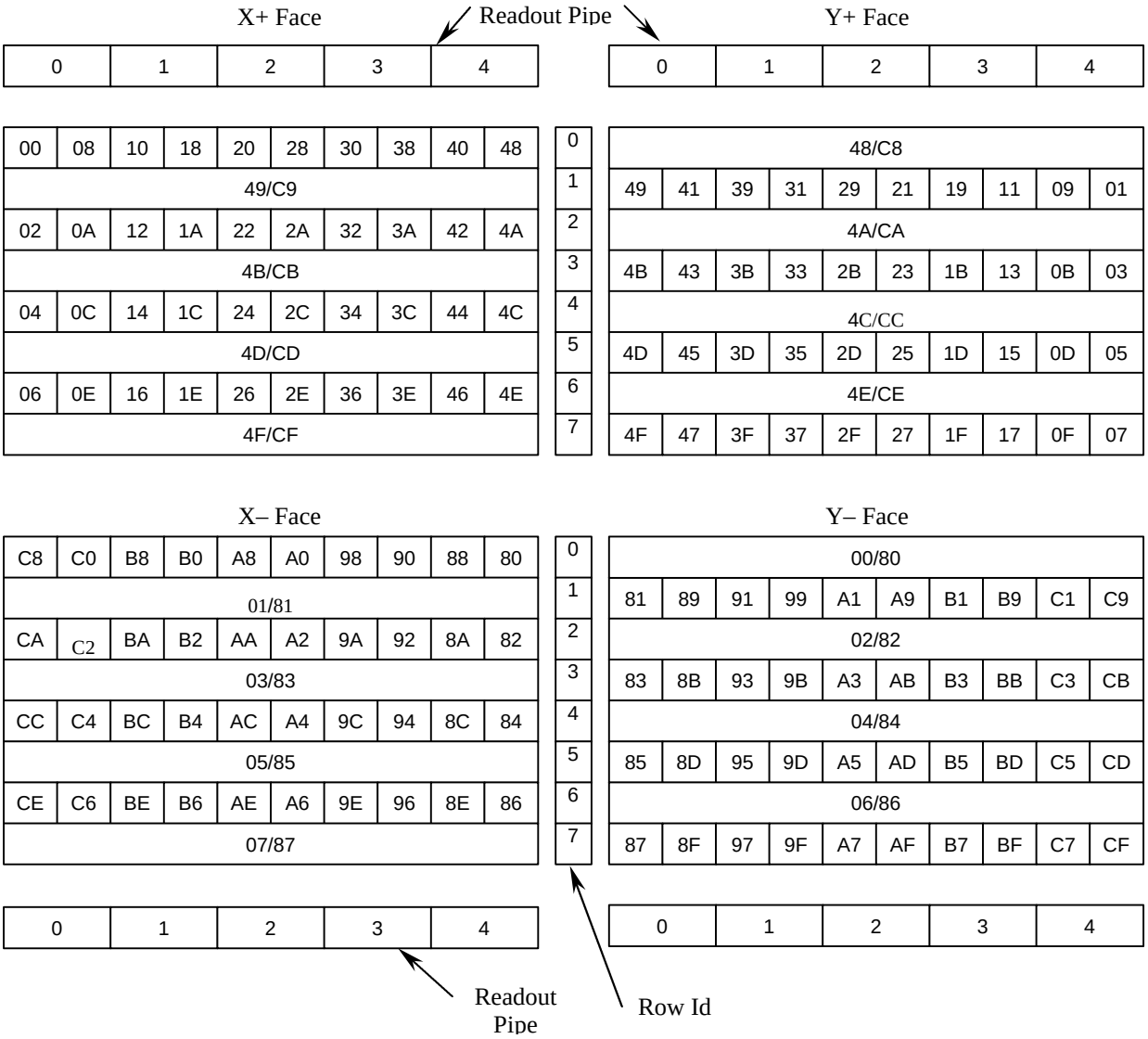

Figure 17. Graphical display of CsI log end enumeration. CsI crystal readouts are identified by 8-bit hex code. The most significant bit is the log-end identifier; thus code 00 and 80 identify the two ends of the same log.

8. Mechanical Arrangement

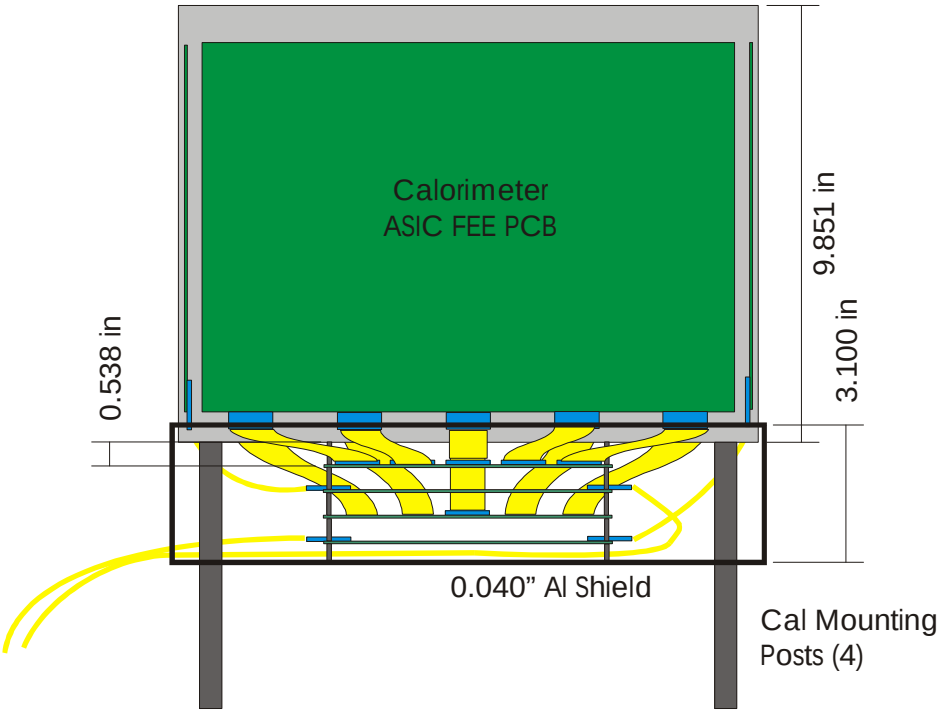

Figure 18. Side view of beam test calorimeter. The FEE boards on each side of the calorimeter connect to one of four controller boards attached below on the calorimeter baseplate via 5 cables. One cable from each controller board attaches to the TEM VME card.

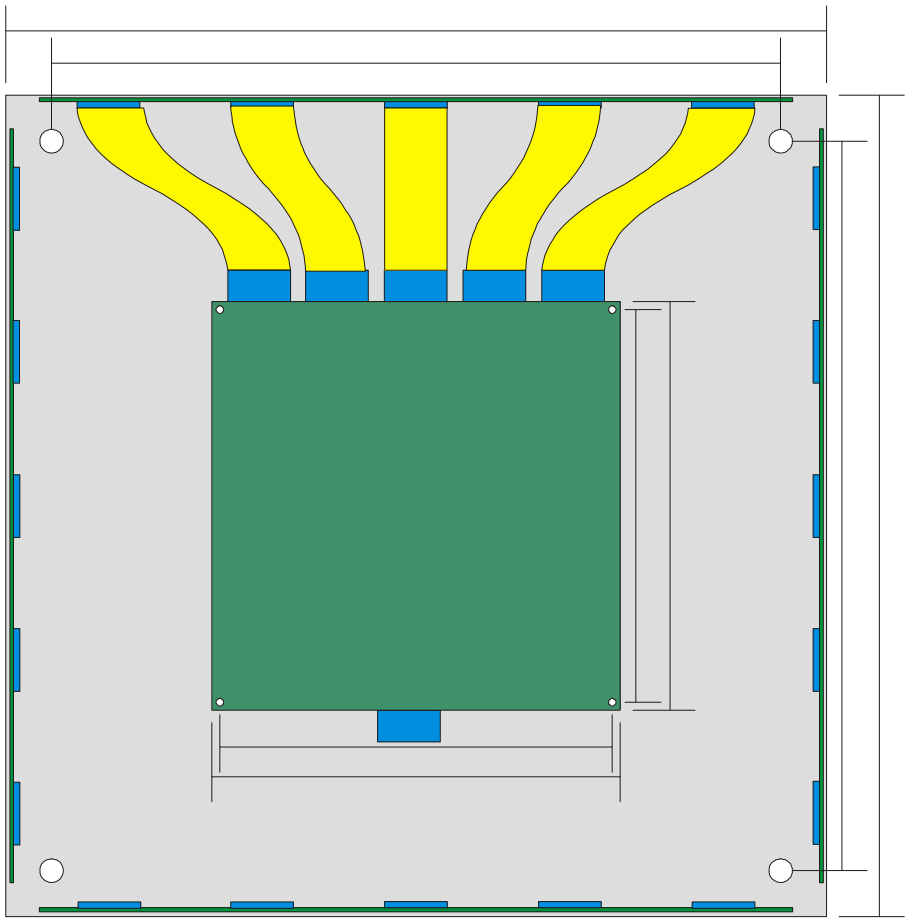

Figure 19. Bottom view of the calorimeter showing controller card stack.

9. Calorimeter TEM VME Card Registers

9.1. brdcntl

brdcntl	0x0020	Read/Write

D15	D14	D13	D12	D11	D10	D9	D8
					FPGA DCLK	FPGA NCFG	FPGA SDAT

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
					RST CAL	RST TRIG CNTR	RST FGPA/FIFO

brdcntl Definitions:

Function	Bit	Description
FPGA DCLK	10	??
FPGA NCFG	9	??
FPGA SDAT	8	??
RST CAL	2	Active low, reset to calorimeter FEE, set low then high
RST TRIG/CNTR	1	Active low, reset trigger counter, set low then high
RST FPGA/FIFO	0	Active low, clear FIFO, set low then high

9.2. brdstat

brdstat	0x0030	Read

D31(msb)	D30	D29	D28	D27	D26	D25	D24
FIFO3 REOF	FIFO3 FULL	FIFO3 HALF FULL	FIFO3 EMPTY	FIFO2 REOF	FIFO2 FULL	FIFO2 HALF FULL	FIFO2 EMPTY

D23	D22	D21	D20	D19	D18	D17	D16
FIFO1 REOF	FIFO1 FULL	FIFO1 HALF FULL	FIFO1 EMPTY	FIFO0 REOF	FIFO0 FULL	FIFO0 HALF FULL	FIFO0 EMPTY

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
				FPGA NSTAT ERR	FPGA CFG DONE		

brdstat Definitions:

Function	Bit	Description
FIFO3 REOF	31	Active hi, msbyte FIFO is full
FIFO3 FULL	30	Active low, msbyte FIFO is full
FIFO3 HALF FULL	29	Active low, msbyte FIFO is half full
FIFO3 EMPTY	28	Active low, msbyte FIFO is empty

FIFO2 REOF	27	Active hi, ms-1 byte FIFO is full
FIFO2 FULL	26	Active low, ms-1 byte FIFO is full
FIFO2 HALF FULL	25	Active low, msbyte FIFO is full
FIFO2 EMPTY	24	Active low, ms-1 byte FIFO is full
FIFO1 FULL	23	Active low, ms-2 byte FIFO is full
FIFO1 REOF	22	Active hi, ms-2 byte FIFO is full
FIFO1 HALF FULL	21	Active low, ms-2byte FIFO is half full
FIFO1 EMPTY	20	Active low, ms-2 byte FIFO is empty
FIFO0 REOF	19	Active hi, ms-2 byte FIFO is full
FIFO0 FULL	18	Active low, lsbyte FIFO is full
FIFO0 HALF FULL	17	Active low, lsbyte FIFO is half full
FIFO0 EMPTY	16	Active low, lsbyte FIFO is empty
FPGA NSTAT ERR	3	Active low, Error occurred while loading FPGA code
FPGA CFG DONE	2	Active high, FPGA code loading is done

9.3. fifo

Fifo	0x0010	Read

D31(msb)	D30	D29	D28	D27	D26	D25	D24
FDAT31	FDAT30	…					

D23	D22	D21	D20	D19	D18	D17	D16

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
						FDAT01	FDAT00

fifo Definitions:

Function	Bit	Description
FDAT31 – FDAT00	31 – 0	32-bit data value from the FIFO. See Table 14 for FIFO data order

9.4. intcntl1

intcntl1	0x0040	Read/Write

D7	D6	D5	D4	D3	D2	D1	D0(lsb)

intcntl1 Definitions:

Function	Bit	Description
Interrupt vector	7 - 0	The interrupt vector associated with the interrupt service routine

Here are the notes on the operation of the VME interrupt service supported by the TEM. This is determined more by trial and error than any detailed documentation.

The TEM supports two interrupts, gps tick and L1T Acq. Bumala says that the gps tick interrupt is a holdover from someother design and shouldn't happen. Both interrupts are programmed from the intcntl1, intcntl2 register pair. Intcntl1 stores the "base" interrupt vector associated with the desired interrupt service routine. Intcntl2 stores the interrupt priority. The actual interrupt vector for one of the two interrupts is derived from the base vector and the interrupt number. The L1T interrupt appears to be the second interrupt so with a base vector of 200, the L1T interrupt is 202. The gps interrupt would then be 201. There is also a possibility that both interrupts could be active at the same time, in which case the hardware would assert vector 203 (the "or" of the two interrupts). In this scheme, it is impossible to actually get an interrupt routed to the base vector address.

For the TEM, we have specified a base vector of 200 (decimal) and an interrupt priority of 6. Thus the L1T service is attached to vector 202.

9.5. intcntl2

intcntl2	0x0044	Read/Write

D7	D6	D5	D4	D3	D2	D1	D0(lsb)

intcntl2 Definitions:

Function	Bit	Description
Interrupt priority	7 - 0	The interrupt priority associated with the interrupt service routine, see notes to section 9.4

9.6. cntlreg

cntlreg	0x0200	Read/Write

D15	D14	D13	D12	D11	D10	D9	D8
					CPU BSY	CMODE 324/81	RDO BSY MAX/-MIN

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
SBIT MUX SEL1	SBIT MUX SEL0	CMD CBL SEL1	CMD CBL SEL0	CNTR CLR	TIMR CLR	REGS CLR	LOGIC CLR

cntlreg Definitions:

Function	Bit	Description
CPU BSY	10	Active high
CMODE 324/81	9	Active high, readout all 4 ranges in event (324 longs) else 1 range readout
RDO BSY MAX/-MIN	8	1 = non-pipelined readout, maximum readout busy time 0 = pipelined readout, minimum readout busy
SBIT MUX SEL1 SBIT MUX SEL0	7,6	Two bit identification of cal cable (FEE side) for readout start bit 0,0 = X+ side, 0,1 = Y+ side, 1,0 = X- side, 1,1 = Y- side
CMD CBL SEL1 CMD CBL SEL0	5,4	Two bit identification of cal cable (FEE side) for subsequent commanding 0,0 = X+ side, 0,1 = Y+ side, 1,0 = X- side, 1,1 = Y- side

CNTR CLR	3	Active high, toggle – reset trigger count
TIMR CLR	2	Active high, toggle – reset trigger timer counter
REGS CLR	1	Active high, toggle – reset FPGA regs to power-up state
LOGIC CLR	0	Active high, toggle – clears logic and counters, regs untouched

9.7. cmdreg

cmdreg	0x0204	Read/Write

D15	D14	D13	D12	D11	D10	D9	D8
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

cmdreg Definitions:

Function	Bit	Description
CF7 –CF0	15 – 8	Command function opcode (CF7, msb). See Table 3 for definition of command function opcodes.
CD7 –CD0	7 – 0	Command data field (CD7, msb)

9.8. statreg

statreg	0x0208	Read

D15	D14	D13	D12	D11	D10	D9	D8

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
		FIFO FULL	SDATA RDO TMOUT	SDATA RDO LNG BSY	SDATA RDO BSY	HSK PAR ERR	HSK RDO BSY

statreg Definitions:

Function	Bit	Description
FIFO FULL	5	Active high, data FIFO is full
SDATA RDO TMOUT	4	Active high, timeout has occurred (~500 usec) in waiting for data
SDATA RDO LNG BSY	3	Active high, start bit has occurred, busy shifting data
SDATA RDO BSY	2	Active high, waiting for start bit
HSK PAR ERR	1	Active high, parity error has occurred on incoming hskp data
HSK RDO BSY	0	Active high, busy reading hskp data

9.9. mskreg

Mskreg	0x020c	Read/Write

D15	D14	D13	D12	D11	D10	D9	D8
L1T OUT MSKC	L1T OUT MSKB	L1T OUT MSKA	L1T IN MSKC	L1T IN MSKB	L1T IN MSKA	ACDL VETO MSK	EXT TREQ MSK

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
CAL TREQH MSK3	CAL TREQH MSK2	CAL TREQH MSK1	CAL TREQH MSK0	CAL TREQL MSK3	CAL TREQL MSK2	CAL TREQL MSK1	CAL TREQL MSK0

msktreg Definitions:

Function	Bit	Description
L1T OUT MSKC	15	Active high, Enable L1T C
L1T OUT MSKB	14	Active high, Enable L1T B
L1T OUT MSKA	13	Active high, Enable L1T A
L1T IN MSKC	12	Active high, Enable L1T C
L1T IN MSKB	11	Active high, Enable L1T B
L1T IN MSKA	10	Active high, Enable L1T A
ACDL VETO MSK	9	Active high, Enable ACD L Veto
EXT TREQ MSK	8	Active high, Enable external trig requests
CAL TREQH MSK3	7	Active high, Enable Cal Hi Req board 3
CAL TREQH MSK2	6	Active high, Enable Cal Hi Req board 2
CAL TREQH MSK1	5	Active high, Enable Cal Hi Req board 1
CAL TREQH MSK0	4	Active high, Enable Cal Hi Req board 0
CAL TREQL MSK3	3	Active high, Enable Cal Low Req board 3
CAL TREQL MSK2	2	Active high, Enable Cal Low Req board 2
CAL TREQL MSK1	1	Active high, Enable Cal Low Req board 1
CAL TREQL MSK0	0	Active high, Enable Cal Low Req board 0

9.10. tstreg

Mskreg	0x0210	Read/Write

D15	D14	D13	D12	D11	D10	D9	D8
		L1T IN TSTC	L1T IN TSTB	L1T IN TSTA	ACDL VETO TST	CPU TREQ TST	EXT TREQ TST

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
CAL TREQH TST3	CAL TREQH TST2	CAL TREQH TST1	CAL TREQH TST0	CAL TREQL TST3	CAL TREQL TST2	CAL TREQL TST1	CAL TREQL TST0

tstreg Definitions:

Function	Bit	Description
L1T IN TSTC	13	Active high, Toggle L1T C
L1T IN TSTB	12	Active high, Toggle L1T B

L1T IN TSTA	11	Active high, Toggle L1T A
ACDL VETO TST	10	Active high, Toggle ACD L Veto
CPU TREQ TST	9	Active high, Toggle CPU TREQ
EXT TREQ TST	8	Active high, Toggle external trig requests
CAL TREQH TST3	7	Active high, Toggle Cal Hi Req board 3
CAL TREQH TST2	6	Active high, Toggle Cal Hi Req board 2
CAL TREQH TST1	5	Active high, Toggle Cal Hi Req board 1
CAL TREQH TST0	4	Active high, Toggle Cal Hi Req board 0
CAL TREQL TST3	3	Active high, Toggle Cal Low Req board 3
CAL TREQL TST2	2	Active high, Toggle Cal Low Req board 2
CAL TREQL TST1	1	Active high, Toggle Cal Low Req board 1
CAL TREQL TST0	0	Active high, Toggle Cal Low Req board 0

9.11. rngreg

Rngreg	0x0214	Read/Write

D15	D14	D13	D12	D11	D10	D9	D8
ADCLR7	ADCLR6	ADCLR5	ADCLR4	ADCLR3	ADCLR2	ADCLR1	ADCLR0

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
CALR7	CALR6	CALR5	CALR4	CALR3	CALR2	CALR1	CALR0

rngreg Definitions:

Function	Bit	Description
ADCLR 7- 0	15 - 8	ACD Veto 1shot range
CALR 7- 0	7 - 0	CAL Veto 1shot range

9.12. gps_timecap1

rngreg	0x0218	Read

D15	D14	D13	D12	D11	D10	D9	D8
GPS15	GPS14	GPS13	GPS12	GPS11	GPS10	GPS09	GPS08

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
GPS07	GPS06	GPS05	GPS04	GPS03	GPS02	GPS01	GPS00

rngreg Definitions:

Function	Bit	Description
GPS15 - 00	15 - 0	GPS least significant 16 bits

9.13. gps_timecap2

rngreg	0x021c	Read

D15	D14	D13	D12	D11	D10	D9	D8
GPS31	GPS30	GPS29	GPS28	GPS27	GPS26	GPS25	GPS24

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
GPS23	GPS22	GPS21	GPS20	GPS19	GPS18	GPS17	GPS16

rngreg Definitions:

Function	Bit	Description
GPS31 - 16	15 - 0	GPS most significant 16 bits

9.14. hskstat

hskstat	0x0100	Read

D15	D14	D13	D12	D11	D10	D9	D8
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
PARITY CORRECT	CMD EXECUTED	-	RDO MD2	RDO MD1	RDO MD0	TRIG TMD1	TRIG TMD0

hskstat Definitions:

Function	Bit	Description
CF7 –CF0	15 - 8	Echoed Command Function (bits D15 – D8 of command)
PARITY CORRECT	7	Active high, cal controller received correct parity
CMD EXECUTED	6	Active high, cal controller executed the command (wasn't busy)
		Programmed data readout mode. Indicates which range(s) to readout. See Table 5 for definition of 8 possible readout configurations.
TRIG TMD1 – TMD0	1 – 0	Programmed trigger mode. Indicates discriminator configuration which causes calorimeter trigger requests. See Table 6 or trigger mode definitions.

9.15. hskcntr0 – hskcntr39

hskcntr0 – hskcntr39 Definitions:

Function	Bit	Description
C15 –C0	15 - 0	16 bit count value from addressed rate counter. See **Error! Not a valid result for table.** for definition of the 40 counters.

hskcntr0 – hskcntr39	0x0104 – 0x01A0 (by 4)	Read

D15	D14	D13	D12	D11	D10	D9	D8
C15	C14	…..					

D7	D6	D5	D4	D3	D2	D1	D0(lsb)
					…..	C1	C0

Table 15. Definition of Rate Counters

Counter Number	Readout address	Rate Counter from Low En x4 Discriminator for CsI Log ID#			
		X+ Side	X- Side	Y+ Side	Y- Side
0	0x0104	00	C8	49	81
1	0x0108	08	C0	41	89
2	0x010C	02	CA	4B	83
3	0x0110	0A	C2	43	8B
4	0x0114	04	CC	4D	85
5	0x0118	0C	C4	45	8D
6	0x011C	06	CE	4F	87
7	0x0120	0E	C6	47	8F
8	0x0124	10	B8	39	91
9	0x0128	18	B0	31	99
10	0x012C	12	BA	3B	93
11	0x0130	1A	B2	33	9B
12	0x0134	14	BC	3D	95
13	0x0138	1C	B4	35	9D
14	0x013C	16	BE	3F	97
15	0x0140	1E	B6	37	9F
16	0x0144	20	A8	29	A1
17	0x0148	28	A0	21	A9
18	0x014C	22	AA	2B	A3
19	0x0150	2A	A2	23	AB
20	0x0154	24	AC	2D	A5
21	0x0158	2C	A4	25	AD
22	0x015C	26	AE	2F	A7
23	0x0160	2E	A6	27	AF
24	0x0164	30	98	19	B1
25	0x0168	38	90	11	B9
26	0x016C	32	9A	1B	B3
27	0x0170	3A	92	13	BB
28	0x0174	34	9C	1D	B5
29	0x0178	3C	94	15	BD
30	0x017C	36	9E	1F	B7
31	0x0180	3E	96	17	BF
32	0x0184	40	88	09	C1
33	0x0188	48	80	01	C9
34	0x018C	42	8A	0B	C3
35	0x0190	4A	82	03	CB
36	0x0194	44	8C	0D	C5
37	0x0198	4C	84	05	CD
38	0x019C	46	8E	0F	C7
39	0x01A0	4E	86	07	CF