The Silicon-Strip Tracker for the GLAST Prototype Tower

R.P. Johnson
Santa Cruz Institute for Particle Physics
University of California at Santa Cruz

Introduction

The purpose of this report is to document the technical goals, the requirements, and an overview of the design and construction of the silicon-strip tracker subsystem of the GLAST engineering prototype tower. The baseline design of the GLAST instrument is described in SLAC-R-522, the GLAST Collaboration proposal to the D.O.E. The GLAST instrument development program, including the prototype tower, is described in the GLAST Collaboration response to the NASA Research Announcement 98-217-02. *All figures contained in this report are for illustration purposes only; they are not to be used for engineering dimensions.*

Technical Objectives

1. Study the performance of the instrument in test beams.
   a) Measure the angular resolution and detection efficiency for photons over a wide energy range (20 MeV up to the maximum available energy) and over the full acceptance (all relevant angles of incidence and side entering as well as top entering). Compare in detail with Monte Carlo simulations.
   b) In conjunction with the calorimeter and ACD system, study the response to background charged particles. Compare in detail with Monte Carlo simulations to validate the design and simulations.
2. Study the performance of the tracker readout electronics.
   a) Measure the noise occupancy versus discriminator threshold in a realistic operating environment with data acquisition activities in progress.
   b) Measure the signal detection efficiency versus discriminator threshold for actual minimum ionizing particles at various incident angles.
   c) Measure the electronics channel failure rate during assembly and operation of a large system.
   d) Develop procedures for remote evaluation, control, and calibration of the electronics.
3. Develop tracker assembly (and disassembly) procedures that can eventually be elaborated into large-scale production procedures.
4. Develop and test the interface between the tracker and the data acquisition system.
5. Develop and test instrument triggers based upon the tracker detectors and electronics.
6. Develop quality control procedures and test stations for the detectors, electronics, and mechanical structures.
7. Develop the mechanical and thermal designs and validate them by vibration and thermal-vacuum testing.

Requirements

The prototype tower should adhere as closely as possible (within budget and other practical constraints) to the baseline flight-instrument conceptual design as presented in SLAC-R-522.

- The tracker will be full sized, with all 17 trays.
- Aluminum will be substituted for beryllium and carbon composites if required for schedule or cost reasons.
- The goal is to have 16 *x,y* planes of prototype detectors. However, if funding is insufficient to purchase the full complement of detectors, then a subset of the trays will be fitted with mechanical dummy detectors.
- The tracker readout electronics will meet the power, noise, and rate requirements of the flight instrument. The readout electronics and associated connectors and cables will also be of the miniature size needed in the flight instrument.
- The tracker will be designed and constructed to be able to withstand the anticipated Delta-II launch loading and vibration and temperature cycling during launch and orbit.

- The tracker will be designed to operate in vacuum. In particular, the passive cooling design must be implemented in this prototype.
- The tracker will be designed and constructed to the mechanical precision specified in SCIPP-97/32.
- Flight-qualified hardware and materials will be used when readily available. Otherwise, hardware and materials will be used that can reasonably be expected to be replaceable by functionally equivalent space-qualified components in the future.

Mechanical Design

a) Tower

The prototype tower consists of 17 composite trays. With the exception of the top and bottom trays, each tray supports on each side a 32 cm by 32 cm layer of silicon-strip detectors. The bottom tray has detectors on only the top, while the top tray has detectors on only the bottom. The trays are assembled into a tower by stacking, with the four bosses at the tray corners making the contact between trays and providing the precision vertical spacing. Locating tubes in the corner bosses provide the lateral alignment between trays. A cable passes through each set of corner bosses to tension the stack and carry part of the launch load, as illustrated in Figure 1.
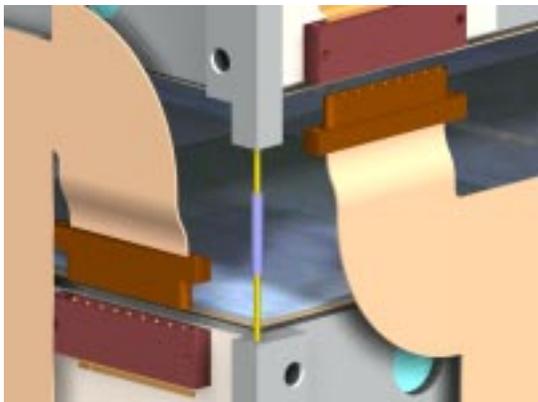

Figure 1. Detail of the tray corner region and the interface between trays.

b) Trays

Each tray is a composite structure with an aluminum closeout[1], a foam or hex-cell core, and carbon-fiber or aluminum face sheets, as illustrated in Figure 2. The lead converter foils mount on the outer surface the face sheet. Each is just the size of the active region of a single detector. A thin strip of material the thickness of the lead foil is needed to fill the gap along the tray edge where the detectors are wire bonded to the electronics.

Kapton flex circuits cover both the top and bottom surfaces to supply the bias potential to the backs of the detectors and electrically shield the detectors from possible noise in the tray. It also carries the signals from the detector strips around the tray corners to the electronics hybrid printed circuit (PC) boards mounted on two opposing sides of the tray.[2] The detector strips are wire bonded to narrow gold-plated traces on the flex circuit. The other end of each trace is wire bonded to an input pad on a front-end readout chip.

The readout chips and supporting electronics are mounted on the hybrid PC boards. Each board covers one edge of the tray. It is glued to the flex circuit and held against the closeout by 1-mm screws. A thin insulator is glued to the back of each board to separate it from the metallic closeout.
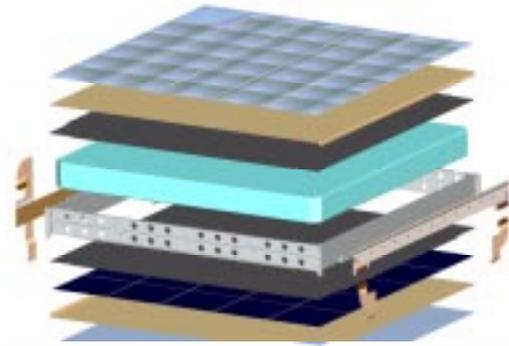

Figure 2. Exploded view of a tray.

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[1]The closeouts will be made from either beryllium or carbon fiber in the ultimate flight instrument. The core might eventually be beryllium foam or a composite hex-cell structure.

[2] The top and bottom trays are exceptional in that they have detectors on only a single side. The bottom three trays are exceptional in that they do not contain any converter foils.

c) Walls

The walls of the towers are completely covered by carbon-fiber panels, as illustrated in Figure 3. They serve to conduct heat and isolate the electronics and detectors from light and electromagnetic interference. In addition, they significantly stiffen and strengthen the tower. They are held onto the closeouts by mechanical fasteners, so that they are easily removed. Details of the fasteners still need to be worked out.
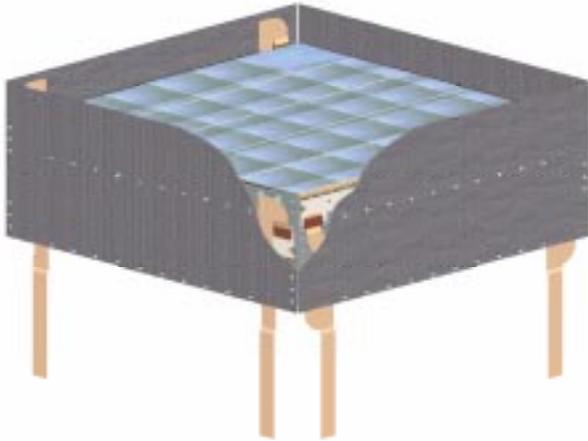

Figure 3. View of the bottom three trays of a single tower, with side walls attached. The Kapton cables extending downward carry the electronics power and signals.

Detectors

The silicon-strip detectors are to be manufactured in industry according to GLAST detailed specifications, which are contained in SLAC-R-522 and also summarized in http://scipp.ucsc.edu/~hartmut/GLAST/GLAST_Det_Specs.ps. They are *n*-bulk, *p*-strip, single-sided detectors with AC-coupled readout, including polysilicon bias resistors. The prototype tower will contain trays with two different detector sizes: 6.4×6.4 cm^2, from 4-inch wafers, and 6.4×10.68 cm^2, from 6-inch wafers.[3] The smaller size detectors will be in 5×5 arrays, while the larger size ones will be in 5×3 arrays.

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[3] In the final flight instrument we envisage using detectors from 6-inch wafers that are wider than 6.4 cm, but this size was chosen for the prototype tower to be compatible with the smaller detectors.

A fully equipped tower requires 800 of the smaller detectors or 480 of the larger ones.

a) Prototypes from 4-inch Wafers

300 detectors of the smaller size have been ordered from Hamamatsu Photonics, with most of them already delivered and found to be well within specifications in all respects. Part of the layout is shown schematically in Figure 4. The thickness is 385 μm.
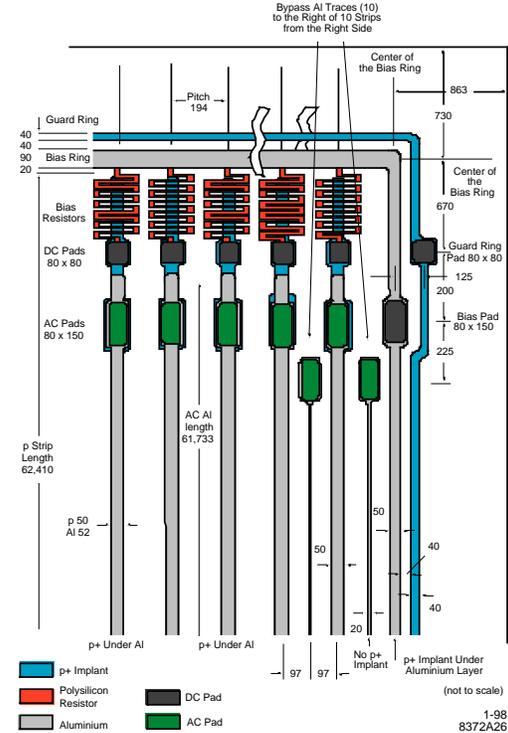

Figure 4. Schematic of the detector layout (not to scale).

b) Prototypes from 6-inch Wafers

Work is in progress at both Hamamatsu Photonics and Micron Semiconductor to develop detectors of the larger size for use in the prototype tower.

c) Assembly into Ladders

Detectors are assembled into 32-cm long ladders before installing them onto the trays. Each ladder consists of either five small detectors or three large detectors connected in series by wire bonds. The detectors are edge bonded with an epoxy adhesive before being

wire bonded. After all of the wire bonds between detectors have been made on a ladder and tested, the wire bonds are encapsulated by a hard epoxy potting compound that is sprayed on. The wire bonds plus encapsulation should not protrude above the detector surface by more than about 0.5 mm.

Electrical Design

Each readout section consists of a hybrid printed circuit board upon which are mounted 25 64-channel front-end readout chips and two readout controller chips. The front-end chips amplify, discriminate, and buffer the detector signals. The data are read out into the controller chips, one at each end of the board, and then passed on to the tower electronics module (TEM, located at the bottom of the tower, below the calorimeter) via two cables, one connected at each end of the board.

a) Front-End Readout Chip

Each readout chip has input pads for wire bonds from 64 detector strips, so five chips are needed for each detector ladder. In addition, there are 32 pads on each chip that are wire bonded to the hybrid, and 16 pads that are wire bonded to the neighboring chips. The

dimensions of the chip are 11.7 mm by 2.2 mm. Details of the front-end chip interfaces are found in SCIPP-98/25.

b) Readout Controller Chip

Each hybrid has 2 readout controller chips in addition to the 25 front-end chips. The controller chip's dimensions are 5 mm by 3.2 mm. 37 wire bonds are needed to connect each to the hybrid PC board. More details of the controller chip interfaces are found in SCIPP-98/26.

c) Hybrid Printed Circuit Board

The hybrid is an eight-layer printed circuit board made by standard technology with 4 mil minimum size traces and spaces. The substrate is FR-4, and the conducting layers are ½-ounce copper (about 17 μm thick), with the top and bottom layers coated with 10 microinches of soft gold (to facilitate wire bonding). The total thickness was specified to be 30±5 mils and turned out to be 32 to 35 mils in the manufactured prototypes. 13 holes are included for mounting of the board onto the closeout with 1 mm screws.
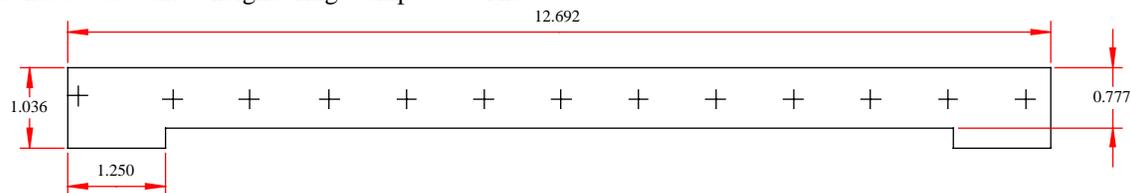

Figure 5. Dimensions of the hybrid printed circuit board, in inches. The crosses indicate the locations of the mounting holes.
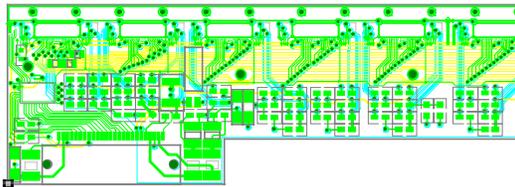

Figure 6. Detailed layout of three layers of the left end of the hybrid PC board.

Digital signals are carried by the central regions of the top two layers. Digital power and ground planes isolate the signals from the lower analog layers. The kapton flex circuit that brings the signals from the detector strips is glued all along the top edge of the board, with the 25 readout chips located next to it and wire bonded to it. Therefore, decoupling capacitors for the front-end chips must be located on the opposite side of the digital traces from the front-end chips. To ensure low-inductance connections from the chips and detectors to the capacitors, very wide traces or entire planes are used. The eight layers are, from top to bottom

1. Chips and other surface mounted parts, digital traces, and the surface area for gluing to the Kapton flex circuit,
2. Mostly digital traces,
3. Split power plane (digital and analog supplies),
4. Split ground plane (digital and analog),
5. Mostly analog ground (with digital ground under the controller-chip regions),
6. Mostly traces between the front-end chips and the decoupling capacitors,
7. Detector bias plane (for a low-inductance route to the decoupling capacitors),
8. Analog 2V plane (for a low-inductance route to the decoupling capacitors).

The layout of layers 1, 2, and 6 is partially displayed in Figure 6.

The back side of the board (layer 8) must be isolated from the conductive tray closeout. That is done by gluing a layer of plastic insulator about 10 mils (0.25 mm) thick to the back side of each board.

The mass of a board without components mounted is 15.35 gr. From the distribution of copper within the board, we estimate that the thickness in radiation lengths is nearly uniform and 1.1% on average.

The hybrid PC board includes on each end a location for a two-terminal IC temperature monitor (AD590F). The monitor acts as a current source that outputs 1 μA of current for each degree Kelvin.

Connectors, resistors, capacitors, inductors, fuses, and temperature monitors are surface mounted onto the hybrid by soldering. The IC chips are glued on with non-conductive epoxy and then wire bonded to the hybrid.

d) Detector Interconnect Flex Circuit

A Kapton flex circuit is used to supply the bias and ground potentials to the detector wafers, electrically shield the back side of each wafer (which is at the bias potential) from the tray structure, and carry the signals from the detector strips around the corner of the tray to the readout chips. The circuit width is the same as that of the hybrid PC board: 322.38 mm. The length is 326.52 mm, of which 3.72 mm forms the 90° 1-mm radius bend and bonds to the hybrid PC board.
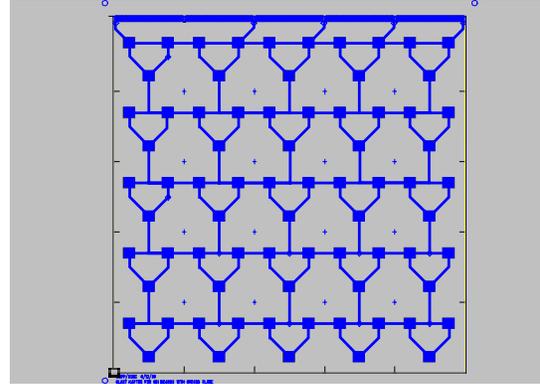

Figure 7. Layout of the Kapton detector-interconnect flex circuit. The 1600 traces for the detector strip signals are located along the top of the figure.

There are two ½-ounce (0.12% X_0) copper conductive layers in the circuit.[4] The lower one is the shielding plane. It is to be held at the analog ground potential. The upper layer, shown in Figure 7, is patterned to bring the bias potential to three square pads under each detector wafer. It also has a pattern of fine traces to carry the strip signals to the readout chips, plus several wider traces to carry the ground and bias potentials from the hybrid PC board and around the bend. Six vias connect the ground traces to the lower ground plane. The upper copper layer is coated with about 10 microinches of gold to facilitate wire bonding.

The section of the circuit that makes the bend has only one copper layer. The ground plane does not extend into that region, in order to minimize the stiffness and get down to a safe 1 mm bend radius. In the bend region there is Kapton on both sides of the copper, to prevent delamination of the copper.

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[4] We hope to decrease the copper thickness, at least for the ground plane, to ¼ ounce copper for the final product, but that will require a special order. The manufacturer does not normally stock or work with such material.
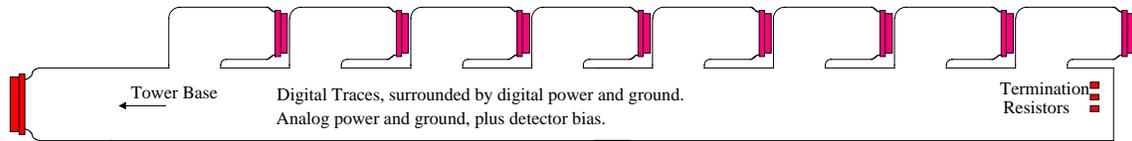
Figure 8. Concept for the flex cable for communication between the TEM and the tracker front-end electronics, showing how each readout section is connected via a dog leg. (Not to scale.)

e) *Flex-Circuit Cables*

The communication between the readout controller chips and the tower electronics module takes place via flat flex-circuit cables. Power transmission and temperature monitoring takes place over the same cable. There is one cable on each edge of each tower wall, for a total of eight cables per tower of four different geometries (left versus right and plug-up versus plug-down). Each cable has provisions for two temperature monitors, such that a total of four trays per tower side can be monitored.[5]

Each cable serves eight readout sections, *i.e.* every second tray. The distance from one readout section to the next is twice the vertical pitch of the stack of trays: 64.16 mm. The main part of the cable lies flat against the bosses protruding from the closeout and is thus held away from the electronics. The doglegs then dip inward to mate with the circuit boards.
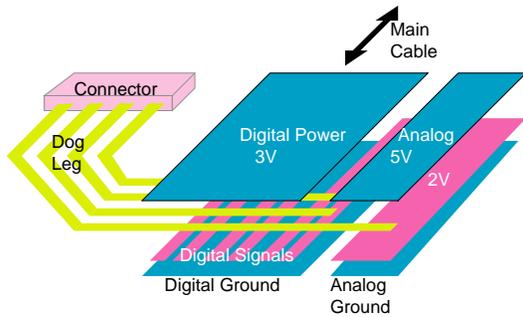

Figure 9. Concept for the flex-cable layout. The actual number of signal traces is much larger than shown here.

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[5] In this way, one could monitor the temperature of each of the 16 trays, but on only one side of each. Alternatively, one could monitor two sides of eight trays. However, one may choose to save power by not installing the maximum number of monitors.

Figure 10. Illustration of how the flex cable fits against the sides of three trays. The dashed lines are the corner bosses of the closeouts. The gray lines are bosses that protrude from the closeouts and support the cable but are cut away to provide clearance for the plugs.

The lowest section of cable must pass by the calorimeter. Its precise length is to be determined. A 37-pin connector at the bottom attaches to the TEM, and eight 25-pin connectors on doglegs attach to the readout sections. Three resistors at the top end of the cable terminate the clock, command, and trigger transmission lines.

The cable has four layers of conductors. The top and bottom layers are for power and ground, while the digital traces are sandwiched between the digital power and ground on one of the inner two layers. The other inner layer is used to cross over to connect the traces to the doglegs. This scheme is illustrated in Figure 9.

Each cable carries the following signal and power lines:

- Digital power (3V) and ground. (2 traces)

- Analog power (5V and 2V) and ground. (3 traces)
- Detector bias (≈100 V). (1 trace)
- Reset. (1 trace)
- Two temperature monitors. (4 traces)
- Data and token. (4 traces)
- Clock, Commands, and Trigger. (6 traces)
- Fast-OR from 8 readout sections. (16 traces)

All of the signals except for Reset are low-voltage differential (LVDS). The clock is intended to run at 20 MHz. More details of the interface to the data acquisition system are found in SCIPP-98/27.

f) Connectors

The connection between the hybrid circuit board and the flex cable (TRK-TEM) is made by 25-pin, 25-mil-pitch, single-row Nanonics Dualobe plastic body connectors. They are already space-qualified. A convenient tool needs to be made to aid in mating of the connectors, as the mating force is considerable considering the tiny size of the connectors. Captive jackscrews are used to pull the plugs up tight into the receptacle and to back them back out.

The receptacles mount flat on the hybrid circuits with surface mount solder pads. We also use surface mount solder pads for attaching the plugs to the flex cables. To make the connection sufficiently robust, the flex cable is backed up with a thin but stiff support plate under the solder pads, and the solder joints are potted with epoxy.

Two 1 mm screws pass through the circuit boards from the back side and thread into each connector. The tray closeout is relieved to accommodate the screw heads.

Mechanical-Electrical Integration

a) Flex Interconnect Installation

The Kapton flex circuit is bonded simultaneously to the tray surface and to the hybrid PC board by an epoxy adhesive. A jig bolted into the tray holds the hybrid precisely in position relative to the tray and in the same plane as the tray surface. The bonding surface on the hybrid is about 2 mm by 320 mm in area and contains 50 small holes to enhance the adhesion of the epoxy.

After the wire bonding is completed, the jig is removed and the Kapton circuit bent until the hybrid lies flat against the closeout wall, to which it is fastened by 13 1-mm screws. If necessary for testing or repairs, the hybrid can be repositioned in the plane of the tray by removing the screws and reinstalling the jig.

b) Detector Ladder Installation

The detector ladders are bonded to the Kapton flex circuit by a conductive adhesive that is applied to the three gold-plated pads under each detector. If possible, an adhesive will be found that will allow removal of a ladder without destruction of the Kapton flex circuit. Strips of tape two mils thick applied to the tray control the spacing between the tray and the detectors.

c) Electronics Quality Control

Many of the assembly procedures are not easily reversed, so it is essential that each part be thoroughly tested before installation. Test stations are being constructed for each of the electronics components:

- Front-end chips. The undiced wafers will be probed at UCSC on an automatic probe station using a probe card that has already been fabricated. A test station has been constructed that interfaces the card to a pattern generator and a logic analyzer controlled by a PC. Test vectors have been designed to test all of the chip functionality and all of the I/O pads. The chips will be diced from the wafers after testing.
- Controller chips. A probe card for this chip has also been fabricated. The chips will be tested in the same way as the front-end chip, except that they will be obtained from MOSIS already diced.
- Hybrid PC boards. The manufacturer will test the boards. After the passive components (connectors, resistors, capacitors, *etc*.) are loaded, we will test that the board can be powered. After the chips will have been loaded and wire bonded, we will connect the board to the data acquisition system and check its operation with a complete set of test vectors. Each board will then be burned in by leaving it under power for some length of time to be determined, followed by retesting.

- Detectors. The manufacturer will test each detector wafer at least for its global leakage current and for broken capacitors and disconnected strips. To what extent we will retest detectors before ladder assembly is to be determined. After wire bonding each ladder and before encapsulating it, we will test it for capacitors broken during wire bonding and for total leakage current.

d) Wire Bonding

The wire bonding is done at UCSC with a Kulicke and Soffa Model 1478 automated wedge bonder using 1-mil aluminum wire. With the exception of a few bonds discussed below, the chips on the hybrid circuit are wire bonded to the PC board and to each other before installation on the tray. All wire bonds between detectors on the detector ladders are to be made and encapsulated before installation on the trays. After installation of the ladders and completed hybrids, the wire bonds from the detectors and hybrids to the Kapton flex circuit are made, with the entire tray positioned in the bonder.

Each front-end chip is given a 5-bit address by the wire bonding procedure. The chip at the far left-hand end of the hybrid has address 0, and the chip at the far right-hand end has address 24. Those two addresses are special, because they turn off the corresponding unused Fast-OR inputs.

The controller chips are also addressed by the wire bonding. This has the unfortunate consequence of making the completed trays non-interchangeable if those wire bonds are encapsulated. In a future design it would be advantageous to have the connector plugs establish the address, but that would require a major change to the hybrid PC board layout.

It will be necessary to wait until the hybrid has been bonded to the flex circuit before making some of the chip-to-chip wire bonds on the hybrid. That is because the feet of the bonds that connect the bias and ground potentials from the hybrid to the flex circuit are below the chip-to-chip bonds. Only some of the bonds that carry the Fast-OR signals from one chip to another are affected. The consequence is that once the chips are installed on the hybrid, those signals cannot be tested until the bonding to the flex circuit is completed.[6]

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[6] All of the Fast-OR inputs and outputs will be tested on the chips before they are mounted, of course.

e) Potting of Wire Bonds.

The wire bonds between detectors are encapsulated during the ladder assembly, as discussed above. Any encapsulation of wire bonds on the hybrid PC boards should not be done until those boards have been installed on the trays and tested with the detectors connected. We will need to investigate to what extent and at what time potting should be done on the hybrids and on the wire bonds connecting the detectors and chips to the Kapton flex circuit.

References

1. *Proposal for the Gamma-ray Large Area Space Telescope*, edited by E. Bloom, G. Godfrey, S. Ritz, SLAC-R-522 (Feb. 1998).
2. *GLAST Instrument Technology Development: Integrated Instrument Development and Demonstration,* Response to NASA Research Anouncement 98-217-02. P.I. Peter Michelson, Stanford University (March 1998).
3. H.F.-W Sadrozinski, *Tray Assembly Precision for the GLAST Silicon Strip Tracker,* SCIPP-97/32 (Nov. 1997).
4. R.P. Johnson, *Interface Description for the GLAST Tracker Front-End Readout Chip, GTFE64,* SCIPP-98/25 (Aug. 1998).
5. R.P. Johnson, *Interface Description for the GLAST Tracker Readout Controller Chip, GTRC,* SCIPP-98/26 (Aug. 1998).
6. R.P. Johnson, *GLAST Tracker Electrical and Data Acquisition Interface,* SCIPP-98/27 (Aug. 1998).