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Complete List of the Functionality Tests Performed on the GLAST BTEM Tracker Front-end Electronics GTFE64, GTRC, and HDI

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Abstract

This document describes complete test procedures of electrical functionality tests on GTFE64c, GTRC/B, and HDI, that have performed for the GLAST BTEM construction. The test setup is described in "Setup for Functionality Test of GLAST Front-end Electronics GTFE64, GTRC, and HDI" by Masaharu Hirayama (January 2000, SCIPP 00/03). With the setup, GTFE64 chips were tested on a wafer, while GTRC's are diced before the test. HDI's were tested through the Nanonics connectors on both ends. Below in this document, all the steps of the functionality tests actually performed are listed step by step.

Contents

1 GTFE64c

1.1 Common settings/procedures

- Set the chip address and an address in a command to 17, unless otherwise specified.
- Perform the following tests once through the left control register, and another the right control register. Use a signal name in parentheses for the test through the right one.
- A pulse on TACKL (TACKR) must be at least one clock-cycle wide.
- When recording a bit stream on DLO (DRO), put some bit stream on DLI (DRI), and confirm that the same bit stream comes out on DLO (DRO) after an appropriate bit stream from the chip being tested.

1.2 Test of control register

1. Send a set-control-register command to set:
   - trigger mask to mask all but channels 0, 3, 6, ..., and 63,
   - channel mask to mask all but channels 1, 4, 7, ..., and 61,
   - calibration mask to mask all but channels 2, 5, 8, ..., and 62,
   - threshold DAC to 13, high range,
   - calibration DAC to 14, high range,
   - and control direction to "right".
2. Send a set-control-register command to set the same setting as above but with control direction set to "left". Then, record a bit stream on CTRLREG output and compare it with the first setting.
3. Send a set-control-register command to set the same setting as the second one and compare a bit stream from CTRLREG output with the second setting.

1.3 Test of calibration mask

1. Send a set-control-register command to set:
   - trigger mask and channel mask to unmask all channels,
   - calibration mask to mask all but channels 0, 3, 6, ..., and 63,
   - threshold DAC to 25, high range,
   - calibration DAC to 12 high range.
2. Send a reset-FIFO command.
3. Send a strobe command and a pulse on TACKL (TACKR). Then, record a state of TLO (TRO) and confirm it changes in response to charge injection.
4. Send a read-event command. Then, record a bit stream on DLO (DRO) and confirm a hit appears every third channel. Then, send an end-read command.
5. Repeat steps 1–4 with calibration mask set to mask all but channels 1, 4, 7, ..., and 61.
6. Repeat steps 1–4 with with calibration mask set to mask all but channels 2, 5, 8, ..., and 62.

1.4 Test of channel mask

1. Send a set-control-register command to set:
   - trigger mask to unmask all channels,
   - channel mask to unmask all but channels 0, 3, 6, ..., and 63,
   - calibration mask to mask all but channels 0, 3, 6, ..., and 63,
   - threshold DAC to 25, high range,
   - calibration DAC to 12 high range.
2. Send a reset-FIFO command.
3. Send a strobe command and a pulse on TACKL (TACKR). Then, record a state of TLO (TRO) and confirm it changes in response to charge injection.

4. Send a read-event command. Then, record a bit stream on DLO (DRO) and confirm no hit appears in data. Then, send an end-read command.
5. Repeat steps 1–4 with channel mask set to unmask all but channels 1, 4, 7, ..., and 61 and with calibration mask set to mask all but channels 1, 4, 7, ..., and 61.
6. Repeat steps 1–4 with channel mask set to unmask all but channels 2, 5, 8, ..., and 62, and with calibration mask set to mask all but channels 2, 5, 8, ..., and 62.

1.5 Test of trigger mask

1. Send a set-control-register command to set:
   - trigger mask to unmask all but channels 0, 3, 6, ..., and 63,
   - channel mask to unmask all channels,
   - calibration mask to mask all but channels 0, 3, 6, ..., and 63,
   - threshold DAC to 25, high range,
   - calibration DAC to 12 high range.
2. Send a reset-FIFO command.
3. Send a strobe command and a pulse on TACKL (TACKR). Then, record a state of TLO (TRO) and confirm it does not change in response to charge injection.
4. Send a read-event command. Then, record a bit stream on DLO (DRO) and confirm a hit appears every third channel. Then, send an end-read command.
5. Repeat steps 1–4 with channel mask set to unmask all but channels 1, 4, 7, ..., and 61 and with calibration mask set to mask all but channels 1, 4, 7, ..., and 61.
6. Repeat steps 1–4 with channel mask set to unmask all but channels 2, 5, 8, ..., and 62, and with calibration mask set to mask all but channels 2, 5, 8, ..., and 62.

1.6 Test of DAC's

1. Send a set-control-register command to set:
   - trigger mask, channel mask, and calibration mask to unmask all channels
   - threshold DAC to 25, high range,
   - calibration DAC to 12 high range.
2. Send a reset-FIFO command.
3. Send a strobe command and a pulse on TACKL (TACKR). Then, record a state of TLO (TRO) and confirm it changes in response to charge injection.
4. Send a read-event command. Then, record a bit stream on DLO (DRO) and confirm a hit appears every channel. Then, send an end-read command.
5. Repeat steps 1–4 with calibration DAC set to 5, low range, and confirm a state of TLO (TRO) does not change in response to charge injection, nor a hit on any channel.

1.7 Test of reset functionality

1. Send a set-control-register command to set:
   - trigger mask and calibration mask to unmask all channels
   - channel mask to mask all but channels 0, 3, 6, ..., and 63,
   - threshold DAC to 25, high range,
   - calibration DAC to 12 high range.
2. Send a reset-FIFO command.
3. Send a strobe command and a pulse on TACKL (TACKR).
4. Send a read-event command, then an end-read command after 30 clock cycles. Then, record a bit stream on DLO (DRO) and confirm a hit appears every third channel until an end-read command is in effect.
5. Repeat steps 1–4 with sending a pulse on RESET instead of an end-read command. Confirm a hit appears every third channel until an end-read command is in effect.

1.8 Test of FIFO

1. Send a set-control-register command to set:
   - trigger mask and calibration mask to unmask all channels
   - channel mask to mask all but channels 0, 8, 16, ..., and 56,
   - threshold DAC to 25, high range,
   - calibration DAC to 12 high range.
2. Send a reset-FIFO command.
3. Send a strobe command and a pulse on TACKL (TACKR).
4. Repeat steps 1–3 with channel mask set to mask all but channels 1, 9, 17, ..., and 57.
5. Repeat steps 1–3 with channel mask set to mask all but channels 2, 10, 18, ..., and 58.
6. Repeat steps 1–3 with channel mask set to mask all but channels 3, 11, 19, ..., and 59.
7. Repeat steps 1–3 with channel mask set to mask all but channels 4, 12, 20, ..., and 60.
8. Repeat steps 1–3 with channel mask set to mask all but channels 5, 13, 21, ..., and 61.
9. Repeat steps 1–3 with channel mask set to mask all but channels 6, 14, 22, ..., and 62.
10. Repeat steps 1–3 with channel mask set to mask all but channels 7, 15, 23, ..., and 63.
11. Send a read-event command and record a bit stream on DLO (DRO). Confirm a hit appears every 8th channel starting from channel 0. Then, send an end-read command.
12. Repeat step 11 7 more times. Confirm a hit appears every 8th channel starting from channel 1, 2, ..., and 7, respectively.
13. Send a reset-FIFO command.
14. Send two clear-FIFO commands.
15. Send a read-event command and record a bit stream on DLO (DRO). Confirm a hit appears every 8th channel starting from channel 2. Then, send an end-read command.
16. Send a reset-chip command.
17. Send a set-control-register command as in step 1.
18. Send a read-event command and record a bit stream on DLO (DRO). Confirm a hit appears every 8th channel starting from channel 0. Then, send an end-read command.

1.9 Test of continuity of fastOR line

1. Send a set-control-register command to set a trigger mask to mask all channels.
2. Put a bit stream on TLI (TRI) and record a bit stream on TLO (TRO). Confirm the bit stream identical to the one on the input appears on TLO (TRO).

1.10 Test of address decoding

1. Send a set-control-register command to set:
   - trigger mask and calibration mask to unmask all channels
   - channel mask to mask all channels
   - threshold DAC to 25, high range,
   - calibration DAC to 12 high range.
2. Send a reset-FIFO command.
3. Send 8 pulses on TACKL (TACKR).
4. Set the chip address to 0 (zero).
5. Send a read-event command with address 0 in the command. Record a bit stream on DLO (DRO) and confirm a hit pattern indicating no hit is followed by the bit stream put on DLI (DRI).
6. Set the chip address to 17.

7. Send a read-event command with address 0 in the command. Record a bit stream on DLO (DRO) and confirm no output appears on DLO (DRO).
8. Repeat steps 4–7 with the chip address and an address in a command set to 1, 2, 4, 8, 16. The chip address 17 should still be used for the second read-out.
9. Set the chip address to 17.
10. Send a read-event command with address 31 (broadcast address) in the command. Record a bit stream on DLO (DRO) and confirm a hit pattern indicating no hit is followed by the bit stream put on DLI (DRI).

2 GTRC/B

2.1 Common settings/procedures

- Set the chip address and an address in a command to 17, and set a GTFE address to 19 in a command, unless otherwise specified.
- Sample outputs of a chip twice in a period of the clock fed to the chip, in order to identify clock signals on CLKL.
- A pulse on TACKI must be at least two clock-cycle wide.

2.2 Test of control register

1. Send a set-GTRC-control-register command to set:
   - the number of chips to read to 19,
   - a flag to exclude an FCS attachment,
   - a flag to ignore x-y coincidence of triggers,
   - a flag to read a layer only with fastOR signals accompanied.
2. Send another set-GTRC-control-register command to set the same settings as above, and record a bit stream on DOUT. Confirm the correct contents of the control register appears in the bit stream.
3. Send a reset-chip command.
4. Send two set-GTRC-control-register command to set the same settings as above, and record a bit stream on DOUT. Confirm the default contents of the control register appears in the bit stream.
5. Put a pulse on RESET.
6. Send two set-GTRC-control-register command to set the same settings as above, and record a bit stream on DOUT. Confirm the default contents of the control register appears in the bit stream.

2.3 Test of command forwarding

1. Send a clock-on command and record a bit stream on CLKL. Confirm clock signals appear on CLKL. Put a pulse on RESET to stop the clock and confirm the stop on CLKL.
2. Send a send-reset-chip command and record a bit stream on CMDL and CLKL. Confirm a reset-chip command for GTFE appears on CMDL and clock signals of appropriate length on CLKL.
3. Send a send-reset-FIFO command and record a bit stream on CMDL and CLKL. Confirm a reset-FIFO command for GTFE appear on CMDL and clock signals of appropriate length on CLKL.
4. Put a pulse on TRI and on TACKI, such that TRI stays at logic high while TACKI is high. Then, send two clear-event commands and record a bit stream on CMDL and CLKL. Confirm a clear-event command for GTFE appear on CMDL for the first clear-event command to GTRC, and none for the second one. Also, confirm clock signals of appropriate length appears on CLKL.
5. Put a pulse on RESET.
6. Send a set-GTFE-control-register command to set:
   - calibration mask to mask all but channels 0, 3, 6, ..., and 63,
   - channel mask to mask all but channels 1, 4, 7, ..., and 61,
   - trigger mask to mask all but channels 2, 5, 8, ..., and 62,
   - threshold DAC to 13, high range,
   - calibration DAC to 14, high range,
   - and control direction to “right”.

   At the same time, put some bit stream on the CTRLREG input of GTRC and record a bit stream on CMDL and CLKL. Confirm a set-control-register command appears on CMDL followed by the correct contents of the control register to set. Confirm clock signals of appropriate length appears on CLKL, too.
7. Send a strobe command and record a bit stream on CMDL and CLKL. Confirm a strobe command for GTFE appears on CMDL and clock signals of appropriate length on CLKL.

2.4 Test of address decoding

1. Set the chip address to 0 (zero).
2. Send a send-reset-chip command with address 0 in the command and record a bit stream on CMDL. Confirm a reset-chip command for GTFE appears in the bit stream.
3. Set the chip address to 17.
4. Send a send-reset-chip command with address 0 in the command and record a bit stream on CMDL. Confirm no command for GTFE appears in the bit stream.
5. Repeat steps 1–4 with the chip address and an address in a command set to 1, 2, 4, 8, 16. The chip address 17 should still be used for the second command.
6. Set the chip address to 17.
7. Send a send-reset-chip command with address 31 (broadcast address) in the command and record a bit stream on CMDL. Confirm a reset-chip command for GTFE appears in the bit stream.

2.5 Test of read-out flags

1. Send a set-GTRC-control-register command to set:
   - the number of chips to read to 1,
   - a flag to include an FCS attachment,
   - a flag to require x-y coincidence of triggers,
   - a flag to read a layer only with fastOR signals accompanied.
2. Put a pulse on TRI and on TACKI, such that TRI stays at logic high while TACKI is high. Then, record a bit stream on TOUT and confirm a signal appears on TOUT.
3. Repeat the previous step 7 more times.
4. Send 8 clear-event commands and record CMDL and CLKL. Confirm a clear-event command for GTFE appears on CMDL for every clear-event command to GTRC. Also, confirm clock signals of appropriate length appear on CLKL.
5. Repeat steps 2–4 without issuing a signal on TRI.
6. Put a pulse on RESET.

2.6 Test of read-out protocol

1. Send a set-GTRC-control-register command to set:
   - the number of chips to read to 5,
   - a flag to include an FCS attachment,
   - a flag to require x-y coincidence of triggers,
   - a flag to read a layer even without fastOR signals accompanied.
2. Put a pulse on TRI and on TACKI, such that TRI stays at logic high while TACKI is high. Then, record a bit stream on TOUT and confirm a signal appears on TOUT.
3. Send a read-event command. At the same time, place a bit stream on RDIN which simulates signals from 5 GTFE's, such that the 1st GTFE and the 4th have some hits, and the others no hit (a single 0 per chip to check the zero-suppression protocol). Record a bit stream on CMDL and on CLKL. Confirm a read-event command and an end-read event for GTFE appear on CMDL, and clock signals of appropriate length on CLKL.
4. Send a set-GTRC-control-register command to set the same settings as above, but with 3 for the number of chips to read.
5. Put a signal on TACKI and record a bit stream on TOUT. Confirm no signal appears on TOUT.
6. Send a read-event command. At the same time, place a bit stream on RDIN which simulates signals from 5 GTFE's, such that the 1st GTFE and the 4th have some hits, and the others no hit (a single 0 per chip to check the zero-suppression protocol). Record a bit stream on CMDL and on CLKL. Confirm a read-event command and an end-read command for GTFE appear on CMDL, and clock signals of appropriate length on CLKL.

7. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.
8. Put a signal on TOKI and record DOUT. Confirm the simulated events are read-out correctly. The ToT should be 5.
9. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.
10. Repeat steps 7–9. Only events from the first three GTFE's should be reported and the ToT should be 0 (zero).
11. Repeat steps 1–10 with the following settings/procedures:
    - the number of chips to read is 5 for both events,
    - a flag to exclude an FCS attachment,
    - a flag to require x-y coincidence of triggers,
    - a flag to read a layer only with fastOR signals accompanied.

    Confirm only the first event is reported. The chip should report no hit for the second event.

2.7 Test of reset functionality

1. Send a set-GTRC-control-register command to set:
    - the number of chips to read to 1,
    - a flag to include an FCS attachment,
    - a flag to require x-y coincidence of triggers,
    - a flag to read a layer even without fastOR signals accompanied.
2. Set logic high to RDIN (throughout this section).
3. Put a signal on TACKI.
4. Send a read-event command. After 40 clock cycles, put a signal on RESET. Record a bit stream on CMDL and on CLKL. Confirm a read-event command and an end-read command for GTFE appear on CMDL and clock signals of appropriate length on CLKL. The clock signals should stop in response to the pulse on RESET.
5. Put a signal on TACKI.
6. Send a read-event command. After 30 clock cycles, send a reset-chip command. Record a bit stream on CMDL and on CLKL. Confirm a read-event command and an end-read command for GTFE appear on CMDL and clock signals of appropriate length on CLKL. The clock signals should stop in response to the reset-chip command.
7. Put a signal on TACKI.
8. Send a read-event command and wait until it finishes reading out.
9. Put a signal on TOKI.
10. Send a read-event command. After 65 clock cycles, put a signal on RESET. Record a bit stream on DOUT. Confirm 63 hits from the first GTFE are being reported and the bit stream stops in response to the pulse on RESET.
11. Put a signal on TACKI.
12. Send a read-event command and wait until it finishes reading out.
13. Put a signal on TOKI.
14. Send a read-event command. After 55 clock cycles, send a reset-chip command. Record a bit stream on DOUT. Confirm 63 hits from the first GTFE are being reported and the bit stream stops in response to the reset-chip command.

2.8 Test of trigger latency counter

1. Send a set-GTRC-control-register command to set:
    - the number of chips to read to 5,
    - a flag to include an FCS attachment,
    - a flag to require x-y coincidence of triggers,

- a flag to read a layer only with fastOR signals accompanied.

2. Place a pulse of 40 clock-cycle wide on TRI. After 32 clock cycles, put a signal on TACKI. Record a bit stream on TOUT and confirm a signal appears on TOUT.
3. Send a read-event command. At the same time, place a bit stream on RDIN which simulates signals from GTFE's. Record a bit stream on CMDL and on CLKL. Confirm a read-event command and an end-read command for GTFE appear on CMDL, and clock signals of appropriate length on CLKL.
4. Place a pulse of 40 clock-cycle wide on TRI. After 33 clock cycles, put a signal on TACKI. Record a bit stream on TOUT and confirm a signal appears on TOUT.
5. Send a read-event command. At the same time, place a bit stream on RDIN which simulates signals from GTFE's. Record a bit stream on CMDL and on CLKL. Confirm no command for GTFE appear on CMDL, and no clock signals of appropriate length on CLKL.
6. Put a signal on TOKI and record a bit stream on DOUT. Confirm the simulated events are reported correctly in the bit stream.
7. Put another signal on TOKI and record a bit stream on DOUT. Confirm no events are reported in the bit stream.

3 HDI

3.1 Common settings/procedures

- All the chip addresses of GTFE's and GTRC's are hard wired. Set addresses in a command to 31 (broadcast address) unless otherwise specified.
- Perform the following tests once through the Nanonics connector at the left side, and another at the right side. Set the right control direction to GTFE unless otherwise specified.
- A pulse on TACKI must be at least two clock-cycle wide.
- At the beginning of every test, put a pulse on RESET and send a reset-chip command to reset the entire HDI.

3.2 Test of GTRC control register

1. Send a set-GTRC-control-register command to set:
   - the number of chips to read to 19,
   - a flag to include an FCS attachment,
   - a flag to require x-y coincidence of triggers,
   - a flag to read a layer even without fastOR signals accompanied.
2. Send a set-GTRC-control-register command to set the same settings as above with the correct GTRC address in the command, and record a bit stream on DOUT. Confirm the correct contents of the control register appears in the bit stream.
3. Send a set-GTRC-control-register command to set the same settings as above with a wrong GTRC address in the command, and record a bit stream on DOUT. Confirm none appears in the bit stream.
4. Send a set-GTRC-control-register command to set the same settings as above with 31 (broadcast address) as a GTRC address in the command, and record a bit stream on DOUT. Confirm the correct contents of the control register appears in the bit stream.
5. Repeat steps 1–4 with the following contents of GTRC control register:
   - the number of chips to read to 12,
   - a flag to exclude an FCS attachment,
   - a flag to ignore x-y coincidence of triggers,
   - a flag to read a layer only with fastOR signals accompanied.

3.3 Test of GTFE control register

1. Send a set-GTFE-control-register command to set:
   - calibration mask to mask all but channels 0, 3, 6, ..., and 63,
   - channel mask to mask all but channels 1, 4, 7, ..., and 61,
   - trigger mask to mask all but channels 2, 5, 8, ..., and 62,
   - threshold DAC to 13, high range,
   - calibration DAC to 14, high range,
   - and control direction to "right".
2. Put a pulse on RESET.
3. Send a set-GTFE-control-register command identical to the one above, but with threshold DAC set to 19, high range, and calibration DAC set to 20, high range. A GTFE address in a command should be set to 0 (zero). Record a bit stream on DOUT and confirm the first setting appears on DOUT.
4. Repeat step 3 with a GTFE address in a command set to 1, 2, 3, ..., and 24.
5. Repeat step 3 with a GTFE address in a command set to 31 (broadcast address). Confirm non appears on DOUT.

3.4 Test of continuity of fastOR line

1. Send a set-GTFE-control-register command to set:
   - calibration mask and trigger mask to mask all but channels 0, 16, 32, and 48,
   - channel mask to mask all channels,
   - threshold DAC to 25, high range,
   - calibration DAC to 12, high range,
   - and control direction to the side being tested.
2. Send a strobe command with a GTFE address set to 0 (zero). Record a bit stream on TOUT and confirm a fastOR signal appears on TOUT.
3. Repeat step 2 with a GTFE address set to 1, 2, 3, ..., and 24.

3.5 Test of data flow in read-out

1. Send a set-GTRC-control-register command to set:
   - the number of chips to read to 25,
   - a flag to include an FCS attachment,
   - a flag to require x-y coincidence of triggers,
   - a flag to read a layer even without fastOR signals accompanied.
2. Send a set-GTFE-control-register command to set:
   - calibration mask, channel mask, and trigger mask to mask all but channel 11.
   - threshold DAC to 25, high range,
   - calibration DAC to 12, high range,
   - and control direction to the side being tested.
3. Send a reset-FIFO command.
4. Send a strobe command. Put a pulse on TAKI at the right time, such that GTFE's can latch their comparator outputs. Wait until the strobe command is over.
5. Send a read-event command. Wait until the GTRC finishes reading out all the GTFE's.
6. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.
7. Put a pulse on TOKI and record a bit stream on DOUT. Confirm the event is read out correctly. Check the FCS attachment and confirm the bit stream is not corrupted.
8. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.
9. Send a strobe command with an GTFE address in the command set to 19. Put a pulse on TAKI at the right time, such that GTFE's can latch their comparator outputs. Wait until the strobe command is over.
10. Repeat steps 5–8.

3.6 Test of reset functionality

1. Send a set-GTRC-control-register command to set:
   - the number of chips to read to 25,
   - a flag to include an FCS attachment,
   - a flag to require x-y coincidence of triggers,
   - a flag to read a layer even without fastOR signals accompanied.
2. Send a set-GTFE-control-register command to set:
   - calibration mask, channel mask, and trigger mask to mask all but channel 11.
   - threshold DAC to 25, high range,
   - calibration DAC to 12, high range,
   - and control direction to the side being tested.
3. Send a reset-FIFO command.

4. Send a strobe command. Put a pulse on TAKI at the right time, such that GTFE's can latch their comparator outputs. Wait until the strobe command is over.
5. Send a read-event command. After 25 clock cycles, put a pulse on RESET. Wait until the GTRC finishes reading out all the GTFE's.
6. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.
7. Put a pulse on TOKI and record a bit stream on DOUT. Confirm the bit stream includes a part of the event that is sent to the GTRC before the pulse on RESET. Check the FCS attachment and confirm the bit stream is not corrupted.
8. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.
9. Put a pulse on RESET and send a reset-chip command to reset the entire HDI.
10. Repeat 1–4.
11. Send a read-event command. Wait until the GTRC finishes reading out all the GTFE's.
12. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.
13. Put a pulse on TOKI. After 200 clock cycles, put a pulse on RESET. Record a bit stream on DOUT. Confirm the the event is being read out correctly, but terminated in response to the pulse on RESET.
14. Place some bit pattern on DIN and record DOUT. Confirm the pattern appears on DOUT.