Signal Timing for the GLAST Prototype Tracker

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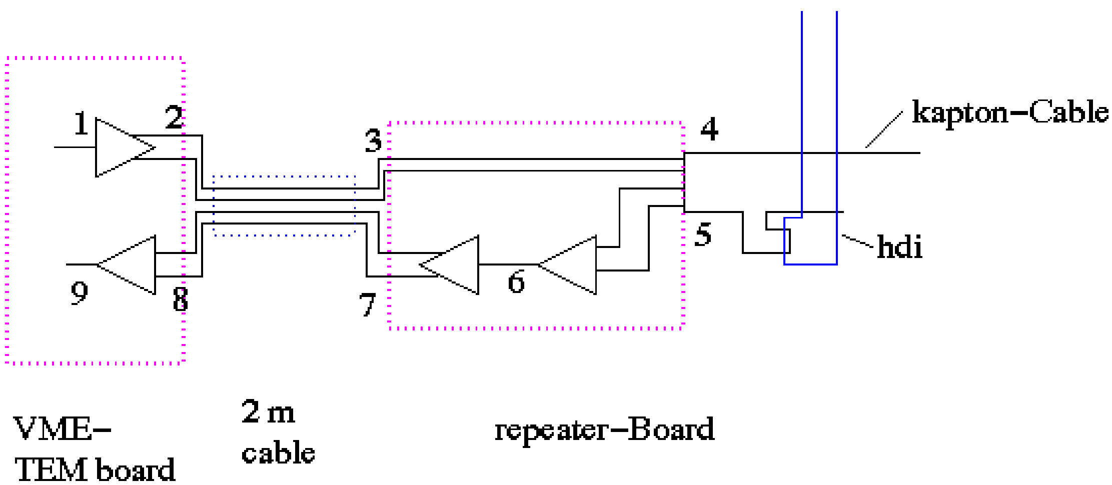
Introduction

Timing issues of the tracker signals i.e.: clock, command, token, data and fast-Or are discussed with respect to the interface of the front-end electronics and the TEM-board. The discussion is based on the setup that will be used at the SLAC beam test.

- Phase between the clock and the tracker command
- Phase between the TEM-clock and the tracker data at the TEM-board
- Propagation delay of the fast-Or signal.

Figure 1 shows the setup that will be used at the beam test.

Figure 1: Schematic of the setup.



The TEM board is connected to the repeater board by a two meter long twisted pair cable. The signals from the TEM-board to the hybrids are not buffered, whereas the data and the fast-Or signals from the hybrids to the TEM-board are buffered by a stage of lvds to cmos and cmos to lvds chips.

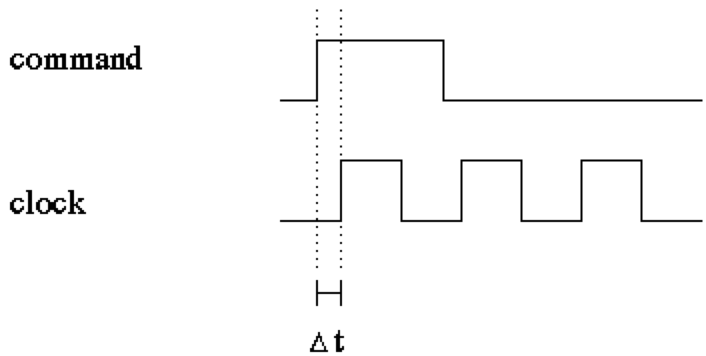
The values shown in the following section were obtained with a setup close to the one for the beam test but neither the cable nor the repeater board is the one that will be used for the beam test. Therefore, the measurements have to be repeated with the final setup.

The actual measurements are discussed in the measurement section at the end of this note.

Phase Clock-Command

The rising edge of the clock at the input of the controller chip has to be delayed with respect to the rising edge of the command signal.

Figure 2: Phase between Command and Clock



A safe range of the delay over which the controller chip works is:

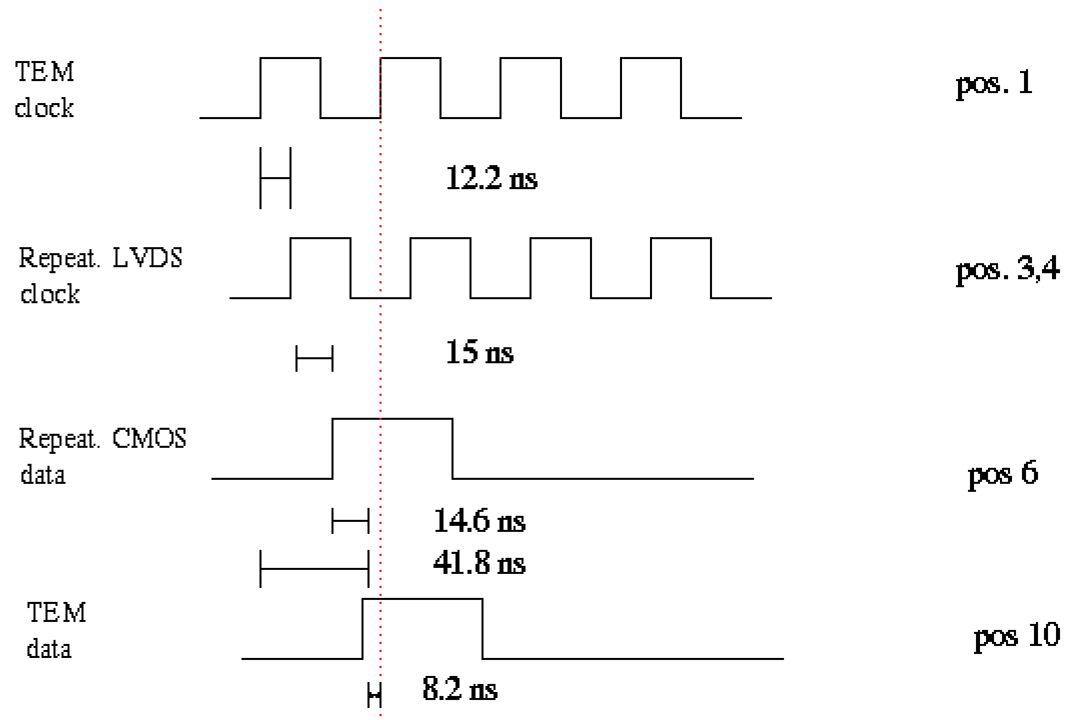
$$\Delta t_{\text{(cmd-clk)}} = 10 - 30 \text{ ns}$$

The phase between the clock and command is not altered by the cable or the repeater board.

Phase Clock and Data

Figure 3 shows a timing diagram of the clock and the data at different positions of the setup (the positions are defined in fig. 1). The important issue is the phase of the clock and data at the TEM-board.
The delay between the clock and data (pos. 6) doesn't include the number of clock cycles that are needed by the controller before it puts out the data. Figure 3 and table 1 only show the shift in phase.

Figure 3 : Timing diagram for the clock and data



The following table breaks down the different delays at the different locations of the setup (see fig 1).

Table 1: Delays introduced in the setup .

Delay between position	*Delay [ns]*	*Min [ns]*	*Max [ns]*	*Comment*
1-2	2.0	1.0	3.0	Driver
2-3	10.2	9.7	10.7	Cable
3-4	0	0	0.5	Board
4-5	13.0 (+ n·50ns)	? (13)	? (13)	Controller, kapton cable
5-6	2.0	1.0	2.7	Receiver
6-7	1.0	0.5	1.7	Driver
7-8	10.2	9.2	11.2	Cable
8-9	3.4	1.5	5.0	Receiver
Total (1-9)	41.8	35.9	47.8	
Δt	8.2	14.1	2.2	

The minimum and maximum values for the driver and receiver chips were obtained from their data sheets. Most of the timing uncertainty is due to these chips. The minimum and maximum values for the propagation delay of the cable are assumed to be 1.48 and 1.63 ft/ns respectively.
The last row shows the time difference between the rising edge of the data and the rising edge of the clock at the TEM-board.

Response to Token

After a trigger acknowledge is issued the read-event-all command followed by a token is sent. The token tells the controller to send its data to the TEM-board. However, a controller first has to read the data from the front-end chips into its own buffer before it starts to put out data. In the standard readout sequence the token is issued immediately after the read-event-all command, which initiates the reading of the front-end chip data into the controller. Assuming the controller reads *nChips* front-end chips and out of those chips there are *nChipsWithHits* with hits it takes,

$$22 + (nChipsWithHits * 65) + (nChips - nChipsWithHits),$$

clock cycles before the start bit of the data appears at the output. So, if there are 25 front-end chips to read and no hits were recorded it takes 47 clock cycles.

The data from all layers are putout to a serial line. The first layer receives a token from the TEM-board and sends the data as soon as it is ready. After all data are sent the token is passed to the next layer. If the next controller is already ready to sent data there is at least one clock cycle between the last bit of the last controller and the start bit of the next controller. However, if the next controller has not finished to read the data from the front-end chips it holds the token until it is ready to send data.

FastOr Delay

Internal charge injection was used to measure **Δt:** the delay between a signal at the input of the preamplifier and the fast-Or signal received at the TEM-board after the lvds receiver chip. The delay depends on the size of the injected signal and the threshold settings.

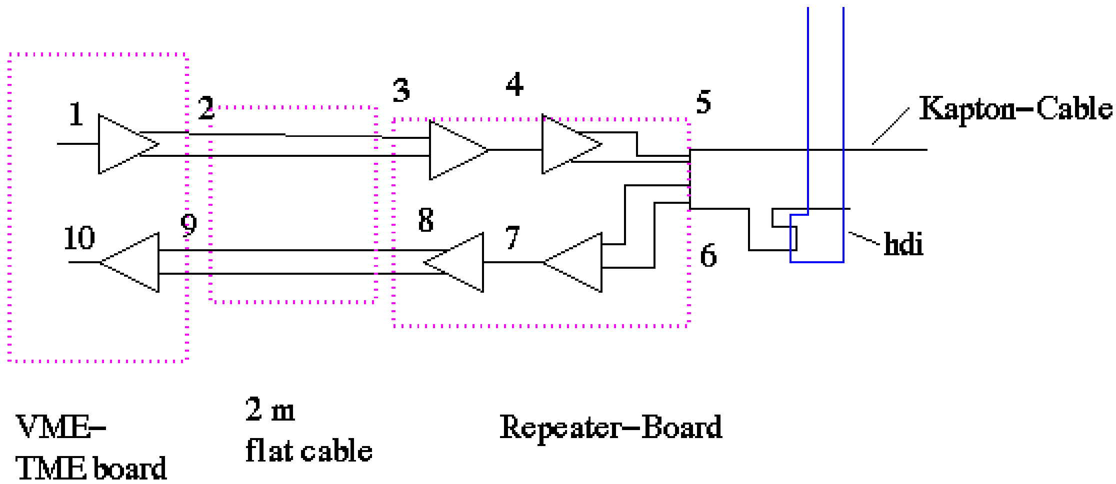
Injected Signal [fC]	*Number of mips*	*Threshold [mV]*	*Δt [ns]*
18	3.5	375	463
18	3.5	225	407
18	3.5	171	373
18	3.5	110	343
18	3.5	60	311
75	15	60	293

For very large signals and low threshold the delay is about 290 ns.

Measurements

This section describes the measurements that were used to obtain the above data.
The setup that was used is different from the one that will be used in the beam test. The main difference is the cable and the repeater board. As shown in the following figure the signals (clock, command, trigger acknowledge and token) are buffered using a

LVDS->CMOS->LVDS stage. The repeater board for the beam test doesn't include this stage. Because of the poor signal quality the timing was measured at the CMOS levels of the repeater board (pos. 4, and 7) and the CMOS level of the TEM-board (pos 10).



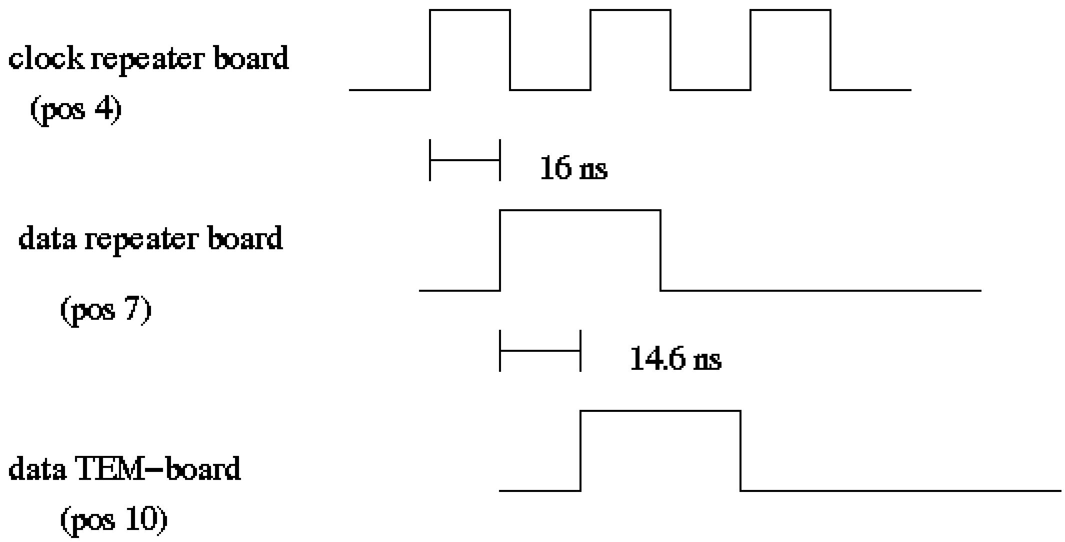
The repeater board uses the DSLV048ATM as a receiver chip and DSLV047ATM as a driver chip. The delays given by the data sheet are:

	Typical [ns]	Min [ns]	Max [ns]
DSLV048ATM	2.0	1.0	2.7
DSLV047ATM	1.0	0.5	1.7

Two measurements were performed:

1. The phase between the clock (pos 4) and the controller data (pos 7).
2. The delay of the data from the repeater board to the TEM-board (pos. 7 to 10 in the figure above).

From these measurement the delay of the cable and the phase of the clock and data at the kapton cable input are estimated.



Delay of the cable

The time between the data CMOS signal on the repeater board and the delayed signal at the TEM board is 14.6 ns. This delay is due to the cable and the DS90LV047 driver and the DS90C032 receiver. The typical delay of these chips are 1.0 and 3.4 ns respectively. Therefore, the delay due to the cable is 10.2 ns.

Phase at the kapton cable

The rising edge of the clock appears 16 ns before the rising edge of the data measured on the repeater board (pos 7,10). If the typical delays due to the LVDS driver and receiver are used, the phase between clock and data at the kapton cable input (pos. 5 to 6) is 13 ns.