

Proposal for Change of Specifications of GLAST Detectors (to be used in Price and Schedule Inquiries)

1) Specification:

Keep the specification the same, but change the specification #7 to the following:

Maximum tolerable number of bad strips <0.5%
 Sum of shorted capacitors,
 bad isolation,
 shorted Al electrodes,
 disconnected strip implant,
 open Al electrode)

2) Layout of generic detectors

For price and schedule inquiries, we have to define a GLAST production detector. In the absence of a final tray/tower design (16 towers vs. 25, 30cm trays vs. 40cm etc.), we should make a guess at what the final detector might look like.

A few guiding principles;

design for ~40cm trays

optimize the layout for 6" wafers

annulus of dead area around rim of wafer : 5mm for 4", 7.5mm for 6"

make detectors square

pitch < 200 microns

Table 1 shows the detector sizes for different wafer sizes for a 38cm tray and a minimum number of detectors covering a tray. As with present detectors, an inactive width between detector edge and inside of bias ring of 888micron normal to strips and 775 micron along strips assumed on the detector edges.. A space of 200 microns between detectors is assumed. The last column shows the maximum detector diameter in comparison to the wafer diameter, and the active area of one GLAST layer with 16 towers.

Table 1: Detector Sizes for 38cm trays for different Wafer Sizes.

Wafer Size [inch]	Tray Coverage dety x detx	Detector Size [cmxcm]	Det Diam/Wafer Diam [cm/cm]	Active area m ²
6"	4x4	9.56 x 9.56	13.52/15.0	2.253
5"	5x5	7.685 x 7.685	10.87/12.5	2.254
4"	6x6	6.437 x 6.437	9.1/10	2.257

(Prototype tower: 25 towers, 5x5 array of 6.4cm x 6.4cm detectors; active area = 2.420 m²)

Assuming the detector sizes from Table 1, the number of chips varies as a function of pitch. This is shown in Table 2, where as a function of pitch, the number of chips per

tray side, and the number of chips covering one detector is shown for 6", 5" and 4" wafers. It turns out that for 6" wafers and 183 and 209micron pitch, there is an integer number of chips per detector, which might have slight advantages for integrating chips, Kapton and detectors.

If the tray size is changed, it is easy to keep the same number of chips and simply scale the pitch by the same amount, unless the change is so large that feature size on the Kapton interconnect or the chip size are affected.

Table 2: Number of Chips per Tray Side and per Detector

Pitch [micron]	# of Chips per tray side	# of 64 channel chips per detector		
		6"	5"	4"
183	32	8	6.4	5.3
195	30	7.5	6	5
209	28	7	5.6	4.7