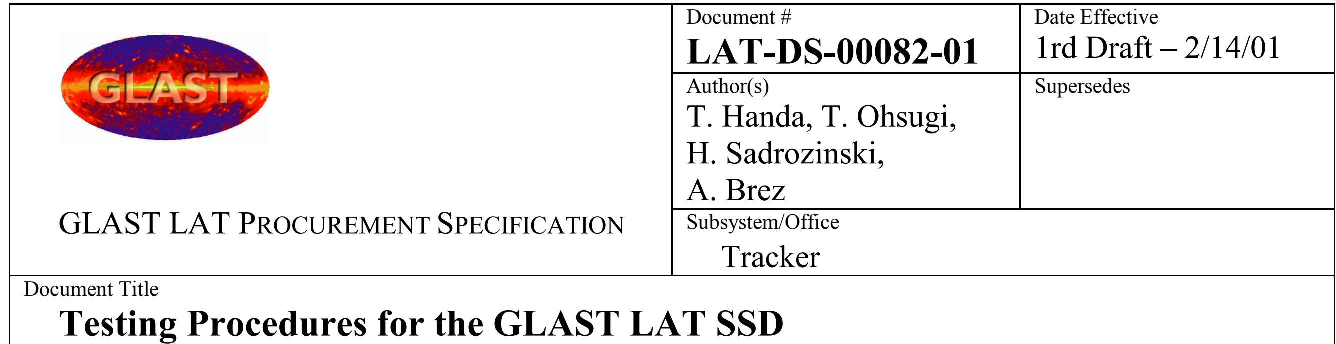

GLAST LAT PROCUREMENT SPECIFICATION	Document # **LAT-DS-00082-01**	Date Effective 1rd Draft – 2/14/01
	Author(s) T. Handa, T. Ohsugi, H. Sadrozinski, A. Brez	Supersedes
	Subsystem/Office Tracker	
Document Title **Testing Procedures for the GLAST LAT SSD**		

Gamma-ray Large Area Space Telescope

(GLAST)

Large Area Telescope (LAT)

Testing Procedures for the GLAST LAT Silicon Strip Detectors (SSD)

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes

1. PURPOSE

These Procedures will serve as the basis for the testing of the GLAST LAT silicon strip detectors.

2. SCOPE

The procedures describe the methods used to test the GLAST LAT SSD and test structures at GLAST LAT institutions.

3. DEFINITIONS

3.1 Acronyms

GLAST	Gamma-ray Large Area Space Telescope
LAT	Large Area Telescope
SSD	Silicon Strip Detector
TBR	To Be Resolved
TBB	To Be Determined

3.2 Definitions

AC Coupling	The Al metal electrode is covering almost the whole length of the p+ implant, separated from it by a dielectric material
AC Pad	Pad to access the Al metal electrode on the strips
Active Area	Area of the Volume from which charge is collected on the strips in <<1us
Buyer	Institution procuring GLAST LAT SSD
C	Capacitance
Contract	Purchase agreement to procure GLAST LAT SSD's
Coupling Capacitor	Capacitor formed by Al metal electrode, dielectric and implant
Customer	Institution involved in the procurement and testing of GLAST LAT SSD's
C-V	Measurement of body capacitance (C) as a function of voltage (V)
DC coupling	Al metal electrode and implant in ohmic contact.
DC Pad	Pad to access the strip implant
Bias Resistor	Resistor connecting every implant to the bias ring
Bias Ring	Implant surrounding the active area, connects to bias resistors
Fiducial	Physical mark in the Al metal layers for alignment and metrology
Guard Ring	Implant ring outside the bias ring without bias connection ("floating")
HPK	Hamamatsu Photonics
I-V	Measurement of leakage current (I) as a function of voltage (V)
N-sub	Substrate contact on the detector front
Pad	Area of the Al metal layer accessible through the passivation. The pad area is defined as the bondable area.
Pitch	Distance between strip centers
Passivation	Topmost layer covering of inert translucent material
Seller	SSD Manufacturer, Vendor,
Sensor	Silicon Strip Detector (SSD)
um	Micro meter (10^{-6}meter)
us	Micro second (10^{-6}second)
V	Voltage, Volt

4. REFERENCES

GLAST LAT AO Response P. Michelson *et al,* Nov 1999.

Strip Technology		T. Ohsugi *et al.,* NIM A, 383 (1996) 167.
BTEM prototype detectors		P. Allport *et al,* SLAC-Pub-8471, June 2000.
Flow-down of GLAST LAT SSD Spec's		H. Sadrozinski, SCIPP 00/33.
GLAST LAT SSD Specifications		LAT-DS-00011-08
GLAST LAT SSD QA Provisions		LAT-DS-00082-01
Drawings	SSD	LAT-DS-00026
	Test structures	LAT-DS-00027

5. SSD TESTING PROCEDURES

i. General Instructions

QA Provisions for the handling of SSD and clean room requirements are spelled out in LAT-DS-00082-01.

ii. Reporting

Test data shall we entered into the SSD data base within one day of taking the data.

iii. Nomenclature

Figure 5.1 is a simplified sketch of the drawing LAT-DS-00027 of the cut-off , identifying the location of the test structures.

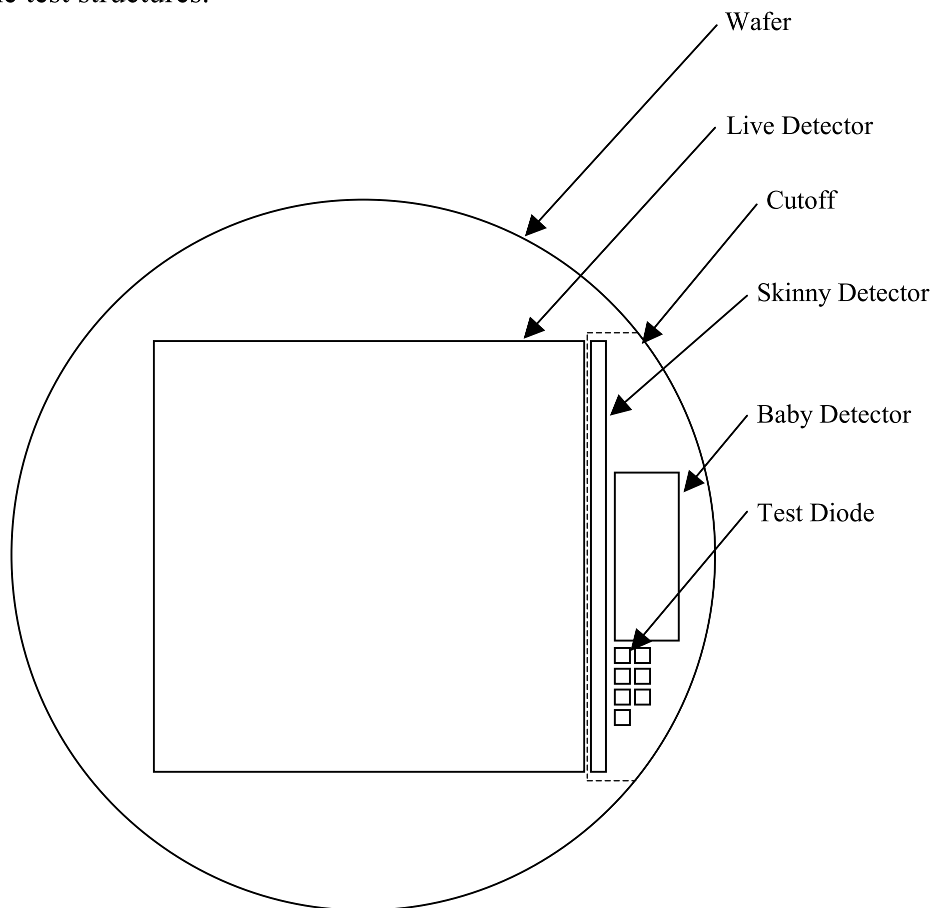

Fig. 5.1 Simplified version of LAT-DS-00027 identifying the location of test structures.

iv. **Detailed Test Procedures**

LEAKAGE CURRENT

Current between bias ring and backside plane.

Connections: see Fig. 5.2

Bias voltage : 0V-200V
Voltage step : 5V
Waiting time before starting measurement : 0 seconds
Waiting time between each voltage step : 5 seconds

On Test structures only: Check the time dependence with 150V bias for a day.

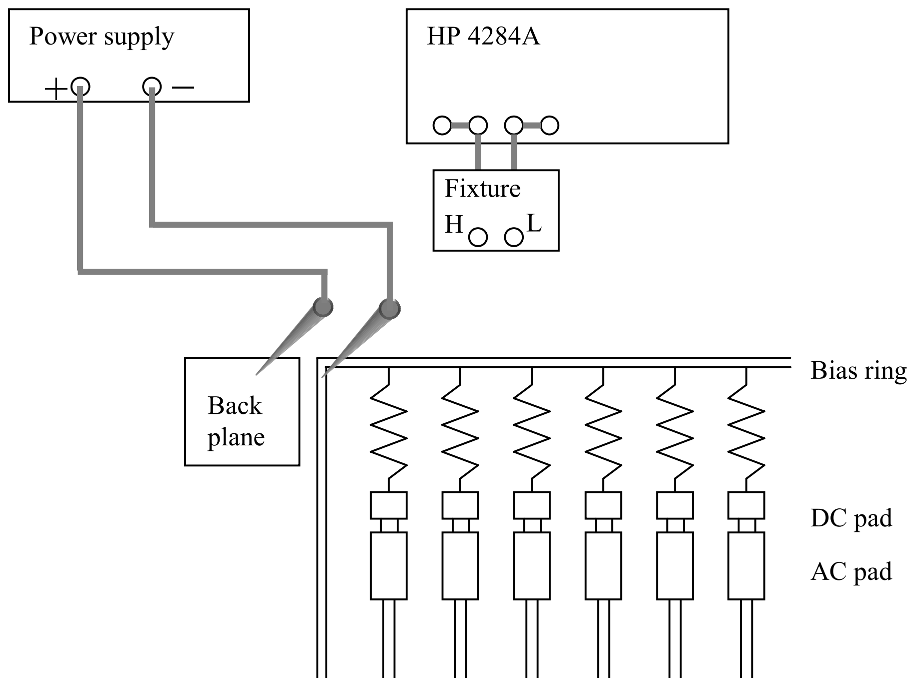

Fig. 5.2 Connections for measuring between the backplane and bias ring for I-V curves.

BODY CAPACITANCE
(TO MEASURE THE FULL DEPLETION VOLTAGE)

Capacitance between bias ring and backside plane.

Connections: see Fig. 5.3

Bias voltage	:	0V~200V
Voltage step	:	5V
Warm up time	:	0 second
Step waiting time	:	5 seconds

Instrument setting for live detectors

Probe	:	Bias Ring
HP4284A mode	:	Cs (poly-silicon register is connected serially)
Frequency	:	100Hz
Level	:	100mV (1V at SLAC)

Instrument setting for diode pads with guard ring

Probe	:	Bias ring(inner ring with probing pads). Use the pad closest to the center of the wafer
HP4284A mode	:	Cp
Frequency	:	1MHz
Level	:	100mV (1V at SLAC)

Instrument setting for baby detectors

Probe	:	Bias ring
HP4284A mode	:	Cp
Frequency	:	100Hz
Level	:	100mV (1V at SLAC)

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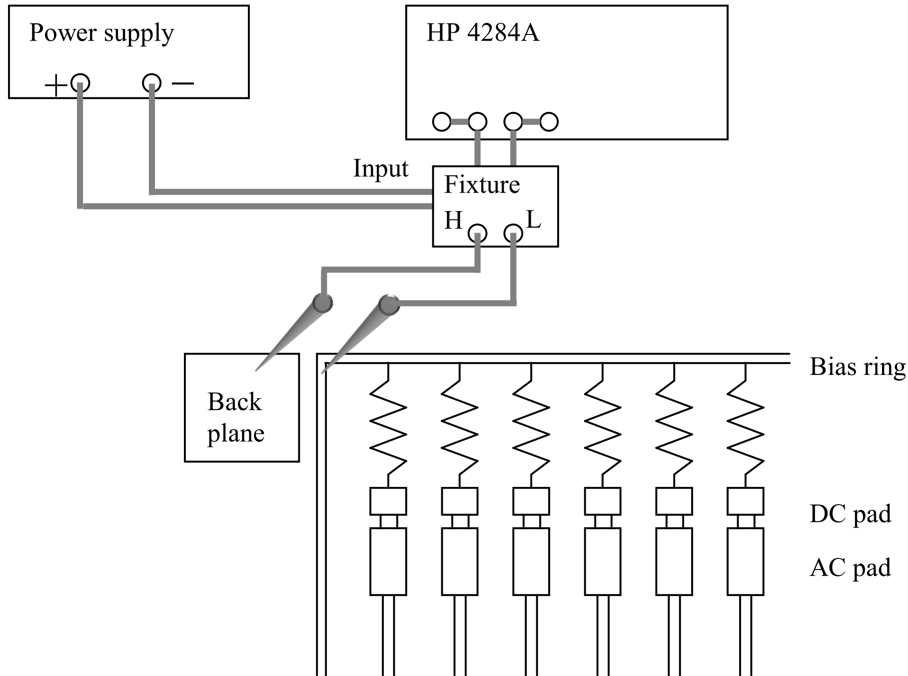

Fig. 5.3 Connections for measuring between the backplane and bias ring for C-V curves

INTERSTRIP CAPACITANCE

Capacitance between an AC strip and the neighboring strips.
.
Connections: see Fig. 5.4

Bias voltage : 150V
Warm up time : 5 minutes
Strips : Three strips in a detector.
Pick up one detector and measure twenty strips.
Number of neighbors : One neighboring pair.
Estimate the ratio between interstrip capacitance at one neighboring pair and the interstrip capacitance at all neighboring pairs.
Use the ratio to evaluate the real interstrip capacitance.
Time dependence : Time dependence of the interstrip capacitance with 150V biasing. (Time constant -> several hours?)
Correlation between the leakage current?

Instrument setting for live detectors and skinny detectors

Probe : Bias+ : Back plane, Bias - : bias ring
LCR fixture high : the strip
LCR fixture low : neighboring strips
HP4284A mode : Cp
Frequency : 1MHz
Level : 100mV (1V at SLAC)

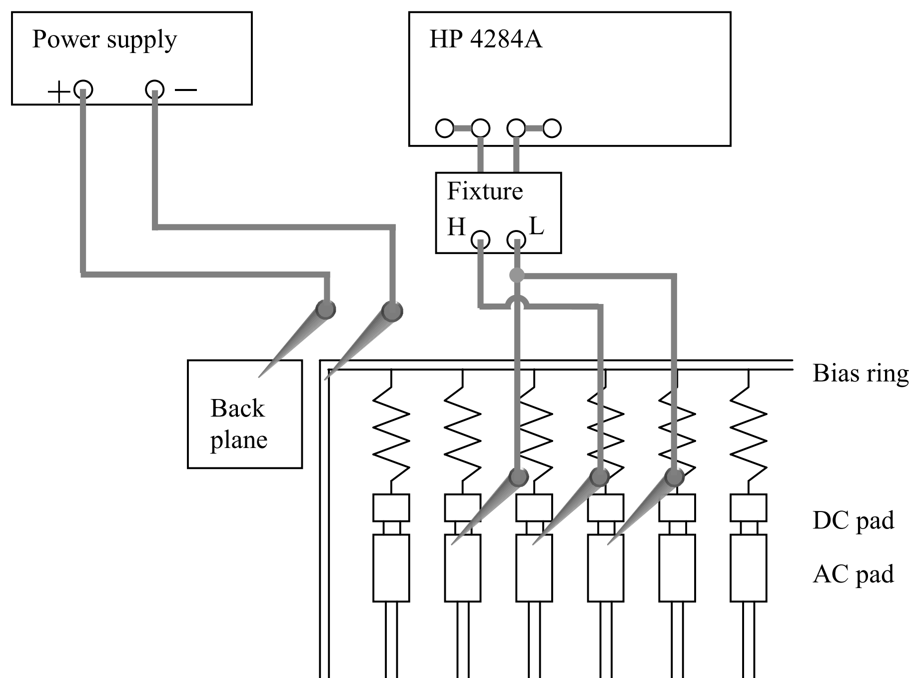

Fig. 5.4 Connections for measuring Interstrip Capacitance.

COUPLING CAPACITANCE

Capacitance between an AC strip and the same number of DC strip.

Connections: see Fig. 5.5

Bias voltage	:	150V
Warm up time	:	5 minutes
Strips	:	Three strips in a detector. Pick up one detector and measure twenty strips.

Instrument setting for live detectors and skinny detectors

Probe	:	Bias+ : Back plane, Bias - : bias ring LCR fixture high : AC strip LCR fixture low : DC strip
HP4284A mode	:	Cs
Frequency	:	1kHz
Level	:	100mV (1V at SLAC)

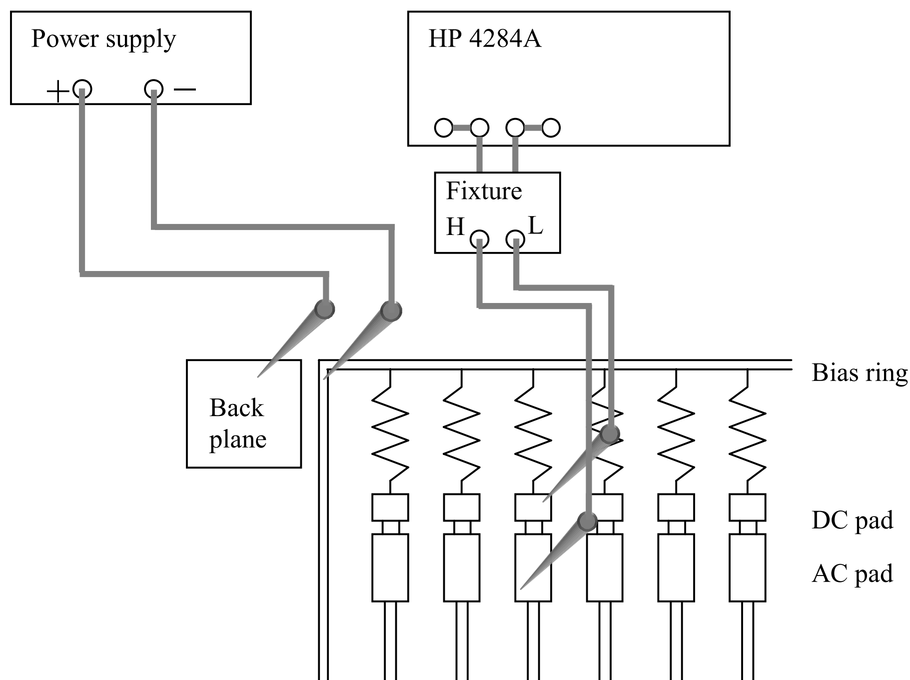

Fig. 5.5 Connections for measuring the Coupling Capacitance.

POLY-SILICON RESISTANCE

Resistance of a poly-silicon bias resistor.

Connections: see Fig. 5.6

Bias voltage	:	150V
Warm up time	:	5 minutes
Strips	:	Three strips in a detector.

Instrument setting for live detectors and skinny detectors

Probe	:	Bias+ : Back plane, Bias - : bias ring
Additional power supply plus:		The DC strip Connection
Additional power supply minus:		Power supply minus
Ampere meter:		before the DC strip probe

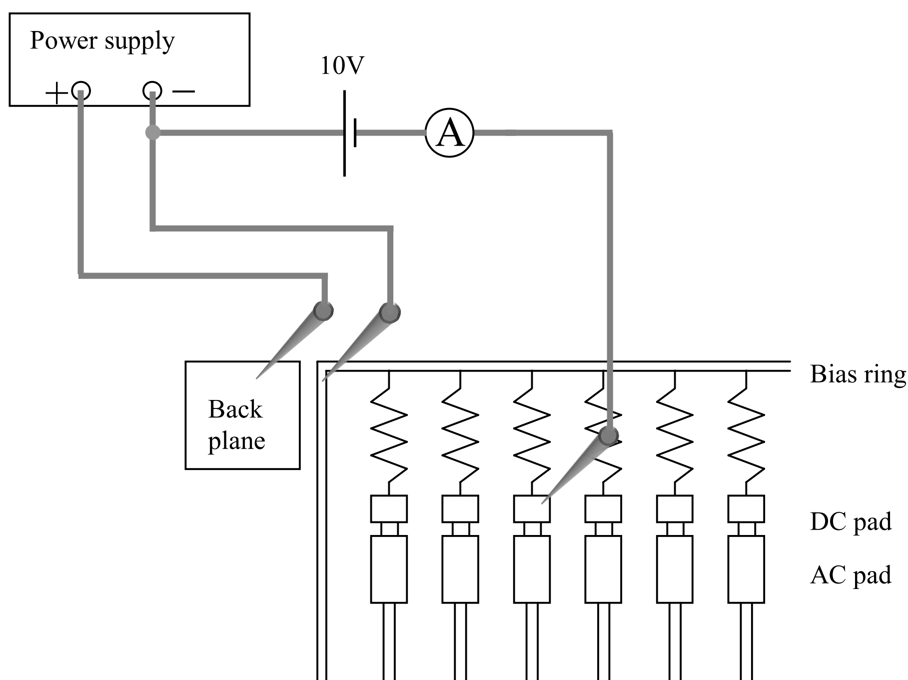

Fig. 5.6 Connections for measuring the Bias Resistors.

INTER-STRIP RESISTANCE

Resistance between two adjacent DC strips.

Connections: see Fig. 5.7

Bias voltage : 150V
Warm up time : 5 minutes
Strips : Three strips in a detector.

<u>Instrument setting for live detectors and skinny detectors</u>

Probe : Bias+ : Back plane,
Bias - : bias ring and a DC strip
Additional power supply plus: Neighboring DC strips Connection
Additional power supply minus: Power supply minus
Ampere meter: before mid strip probe

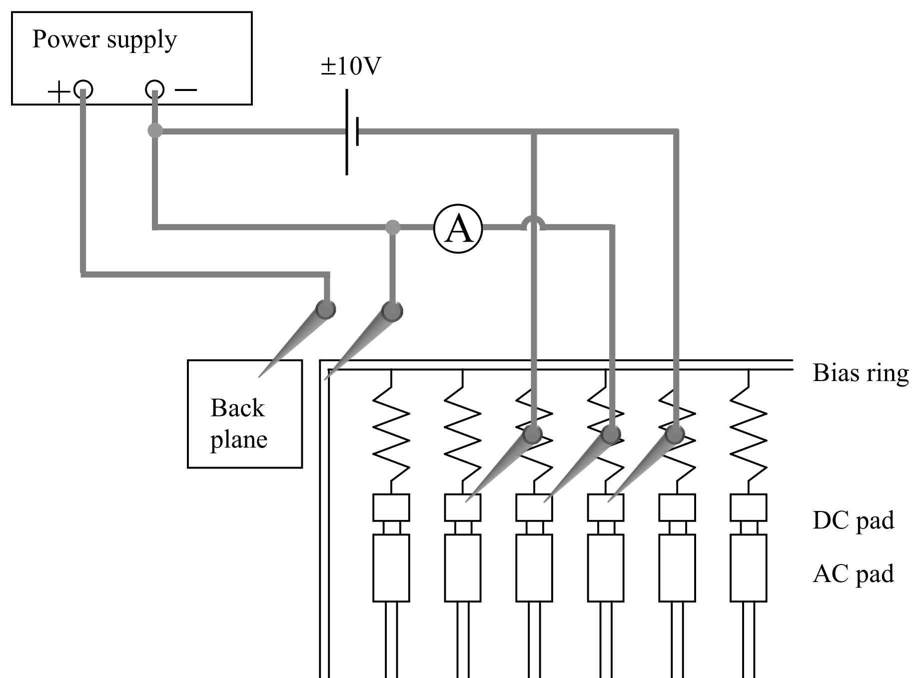

Fig. 5.7 Connections for measuring the Interstrip Resistance.

SAMPLE TEST SHEET

Minimum Information to be entered into the Data Base

GLAST 2000 Test Sheet

Detector ID #	Tester	Date

		HPK Test	GLAST Test (Pre-Rad) Tester Temp: Date			GLAST Test (-100Gy Tester Temp: Date		
			Detector	Skinny	Baby	Skinny	Baby	Other
I (150V)	[nA]							
I (200V)	[nA]							
V (dep)	[V]							
C (dep,)	[pF]							
# of Bad Chan.								
R Bias (Ave)	[MOhm]							
R Bias (High)	[MOhm]							
R Bias (Low)	[MOhm]							
R(Al Strip)	[Ohm]							
R(Int-2neighb.)	[Gohm]							
C(Int-4neighbor	[pF]							
C(Coupling)	[pF]							
Thickness	[um]							
Width	[cm]					Edge-to-Marker B		
Length	[cm]					Edge-to-Marker B		
Alignment First	[um]					Centering Implant-Metal		
Alignment Last	[um]					Centering Implant-Metal		

Comments