ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Trieste

INFN/TC-xx/xx
xx Settembre 2000

SIMULATIONS OF THE SILICON MICROSTRIP DETECTOR FOR THE GLAST EXPERIMENT.

Claudio Piemonte

INFN, Sezione di Trieste, Via A. Valerio 2, I-34127 Trieste, Italy

Abstract

Device simulations of the silicon microstrip detectors that will equip the Tracking System of the GLAST experiment have been performed. The influence on the electric characteristics of both strip pitch and width have been evaluated. First, a DC calculation is done to predict the risk of breakdown within the working bias conditions. Then, the backplane and interstrip capacitances are estimated by means of an AC analysis.

Published by **SIS-Pubblicazioni**
Laboratori Nazionali di Frascati

1 Introduction.

The GLAST tracking system uses silicon microstrip detectors to track the electron-positron pairs resulting from gamma-ray conversion in thin lead foils [1,2]. It consists of a square 4×4 array of nearly identical tower modules. Each tower has a scintillator veto counter on the top, followed by a 16-layer silicon-strip tracker and, finally, a cesium iodide calorimeter. Each tracking layer uses two planes of single-sided silicon strip detectors with strip oriented at 90 degrees with respect to each other. The detectors, cut from 6-inch wafers, have a size of about $9 \times 9\,cm^2$ and are wire bonded into "ladders" $36cm$ long. Four of these "ladders" compose a detector plane. When operating a system, with such a high channel count, in space, two limitations appear : the availability of power for the electronics and the difficulty of dissipating the resulting heat. In order to satisfy these constraints, both the number of channels and the readout electronics power consumption should be minimised.

The baseline detector is realised on n-type wafer having a resistivity of $6\,k\Omega \cdot cm$, and a thickness of $400\,\mu m$. The readout electronics is AC coupled to the p^+ implants, which are biased by means of integrated polysilicon resistors. This design foresees a strip pitch of $208\,\mu m$, and an implant width of $50\,\mu m$. The metal overhangs the oxide $4\,\mu m$ beyond the implant in order to reduce the risk of breakdown. The resulting number of strips per detector is 448, thus, using a 64-channel readout electronics, 7 chips are necessary to collect all the information. Recently, the constraints on the power consumption has been revised, forcing a reduction of the number of chips. It results in a reduction of the number of strips per detector.

In this paper, the electrical performances of the detector are evaluated, varying both the strip pitch and width. First, a DC analysis is done to estimate the electric field in the critical region. Then, an AC analysis is applied in order to predict the interstrip and backplane capacitances.

2 Simulation technique.

The simulation is carried out with ATLAS Device Simulation Software produced by Silvaco [3]. A 2D approach is adopted since, for the simulated values, the partial derivative along the strip length is negligible. The lateral boundary conditions are a crucial point when selecting the length of the structure to be simulated. Mainly, there can be two approaches. One is to build a very long cell in order to keep the lateral boundaries distant from the region of interest. The drawback is a high number of mesh points and, consequently, a long computational time. The other approach is to choose a lateral boundary

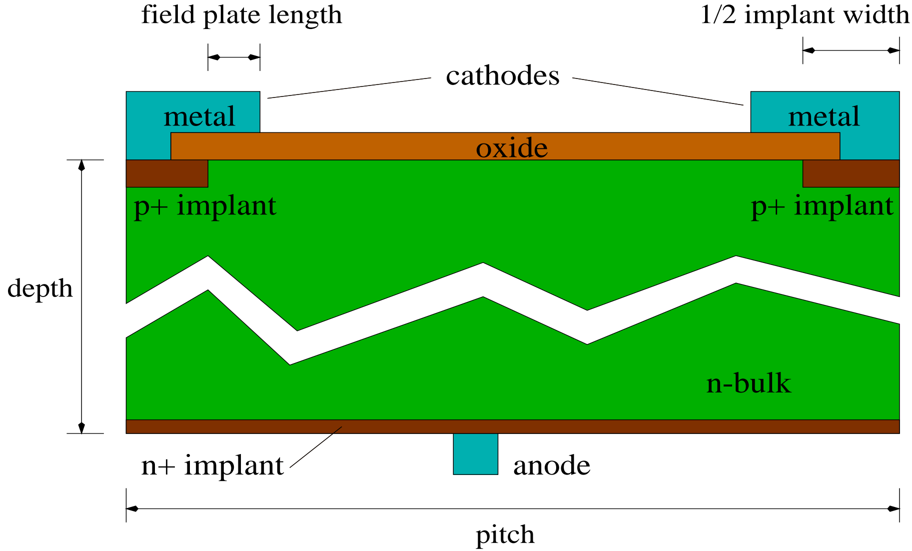

Figure 1: Basic cell used for the simulations.

where only the vertical component of the electric field is present. As a result, we obtain a very narrow cell having a length equal to the strip pitch (fig. 1). This is optimal for the electric field analysis because a high number of points can be used to refine the mesh at the edges of the implants without exceeding the computational time. Nevertheless, this structure is not suitable for the interstrip capacitance evaluation, because the coupling between non-adjacent strips is neglected. As a matter of fact, this calculation requires a lower number of mesh points with respect to the DC analysis, thus we can join more cells without increasing the computational cost.

The DC solution is obtained solving both Poisson and carrier continuity equations. This analysis allows for the evaluation of the breakdown risk. It is known that breakdown occurs when free carriers are accelerated up to a point where they have sufficient energy to generate more free carriers when colliding with the atoms of the crystal. In order to acquire sufficient energy two conditions must be met: the electric field is enough high (more than about $3 \times 10^5\,V/cm$), and the mean free path of the carriers is long enough to allow acceleration to a sufficient high velocity. Only when the generation rate of these free carriers is sufficiently high this process leads to avalanche breakdown. In order to take into account these parameters, an impact ionization model is included in the simulation.

Before starting the simulations, two parameters must be defined: the oxide charge density and the p^+ implant profile. The former, for the sake of simplicity, is considered all localised at the $Si - SiO_2$ interface, while a gaussian shape is chosen for the latter.

It is worth noting that, in the simulations, the p^+ implant has been directly connected to

the metal. This does not introduce an appreciable error since the flat band voltage, related to the thin AC coupling oxide layer, is very small.

The AC analysis is performed joining two elementary cells. It allows for the re-

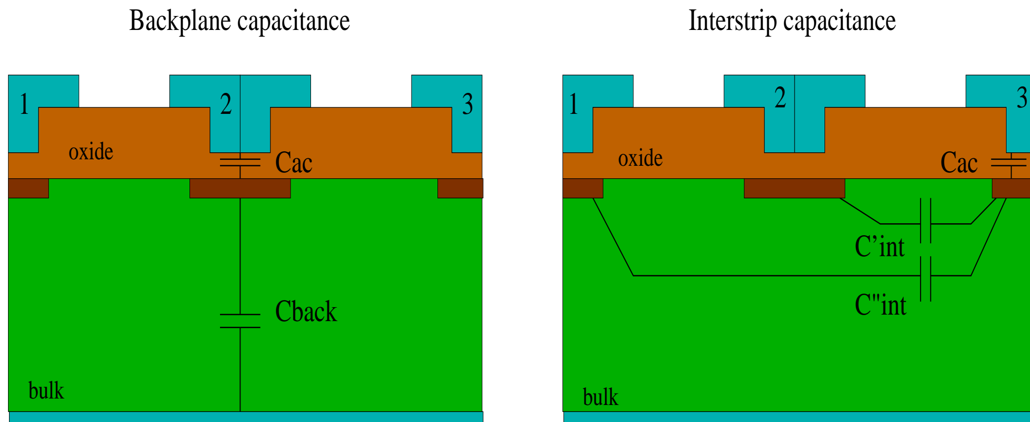

Figure 2: Structure adopted for the AC analysis .

construction of the strip capacitance, one of the parameters determining the noise level of the readout electronics. It is given by the sum of two capacitances: one (C_{back}) derives form the coupling between the implant and the backplane layer, while the other (C_{int}) is due to the coupling between the considered strip and all the others. We do not take into account a third tiny contribution given by the AC coupling capacitor, since the simulation is performed on a structure in which the metal is connected directly to the implant.

The procedure adopted for the simulation is the following: first, the device is brought at a bias voltage rising the potential of the anode. Then, in order to evaluate C_{back}, a small signal (with a frequency of $1MHz$) is applied to the anode, and the capacitance between the central strip (strip n. 2) and the anode itself is checked. As far as C_{int} is concerned, a small AC signal is applied to the cathode n. 3 and the capacitances C'_{int} and C''_{int} are measured. In this way the coupling to more distant neighbours is neglected, and the total capacitance is given by:

$$C_{tot} = C_{back} + C_{int} = C_{back} + 2 \times (C'_{int} + C''_{int}) \qquad (1)$$

The calculation of the backplane capacitance as a function of the bias voltage permits the reconstruction of the full depletion voltage by means of the $1/C^2_{back}$ curve.

The table below shows the pitch/width values used in the simulations.

width μm	pitch μm	width/pitch
50	175	0.286
50	208	0.240
50	235	0.213
50	265	0.189
60	175	0.343
60	208	0.289
60	235	0.255
60	265	0.226

Table 1: Pitch and width values used in the simulations.

3 DC analysis.

First, a simulation is done in order to estimate the impact of the metal overhang on the electric field intensity in the vicinity of the junction. Fig. 3 shows the map of the electric

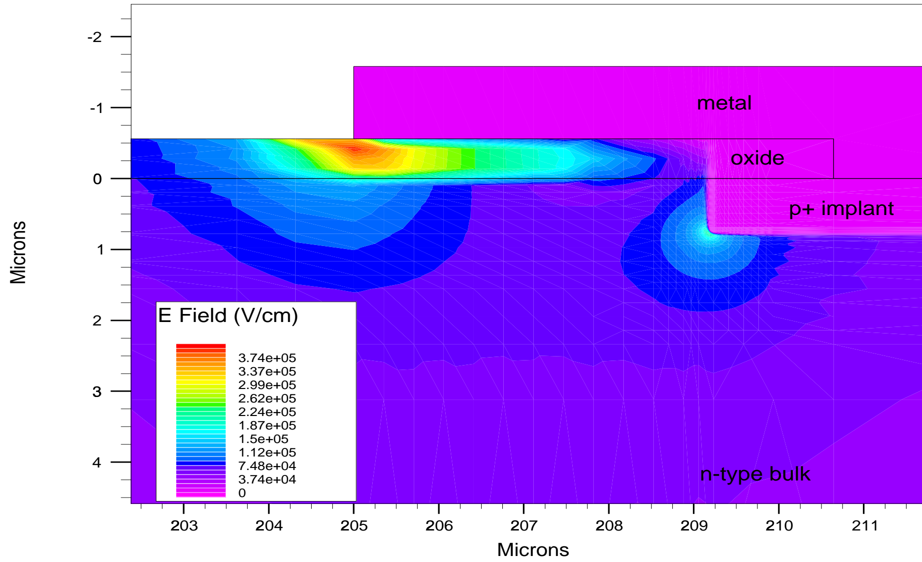

Figure 3: Map of the electric field strength for the $235/50$ structure (the bias voltage is $200V$).

field intensity for the $235/50$ (pitch/width) structure with a metal overhang of $4\,\mu m$, and an oxide charge Q_{ox} of $1 \times 10^{11}\,q/cm^2$. In the silicon, the highest electric field is located at the implant edge and in the proximity of the metal border. Without field-plates, the

lines of the electric field would be all accumulated at the edge of the implant. Fig. 4 shows the profile of the electric field strength, taken along a line crossing the edge of the p^+ implant, for the same structure: (a) with, and (b) without field-plate. The usefulness

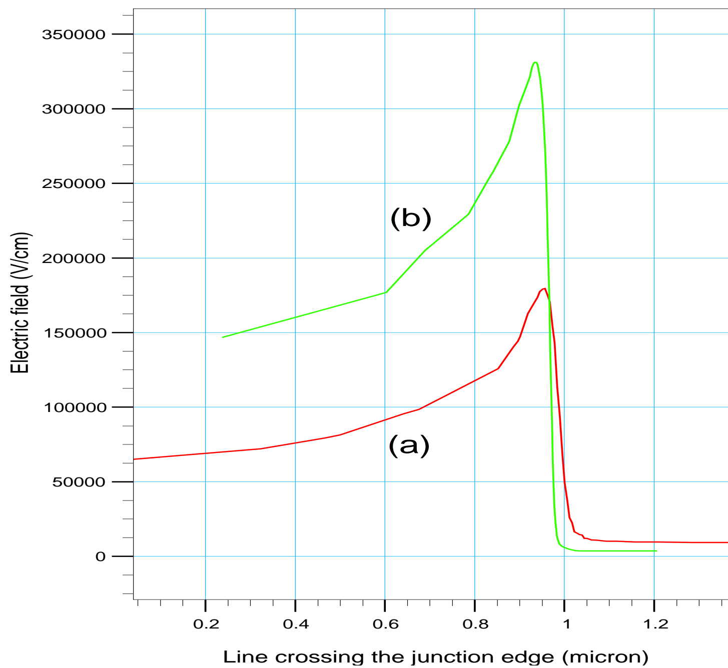

Figure 4: Electric field profile along a cut-line crossing the implant edge for the $235/50$ structure: (a) with, and (b) without field-plate.

of the field-plate is clearly visible: the peak height is reduced by two times. Furthermore, the device without field-plate presents a peak higher than the critical value, hence potentially dangerous. Fig. 5, showing the electron current density, demonstrates that there is generation of free carriers in that region, but not high enough to determine an avalanche breakdown. According to the simulations, it occurs at a bias voltage of about $600V$. Plainly, the calculation does not take into account the presence of local defects which could generate enough free carriers to reach the breakdown at a lower voltage with respect to the ideal case. Thus, the use of the metal overhang is advisable in a detector with such characteristics.

Now, let us analyse the influence of the pitch/width size on the electric field strength. Fig. 6 and 7 display the maximum value of the electric field as a function of the bias voltage for the structures listed in Table 1. As expected, it depends both on the implant pitch and width. Anyway, the peak intensity is below the critical value for all the structures up to a bias voltage of $300\,V$.

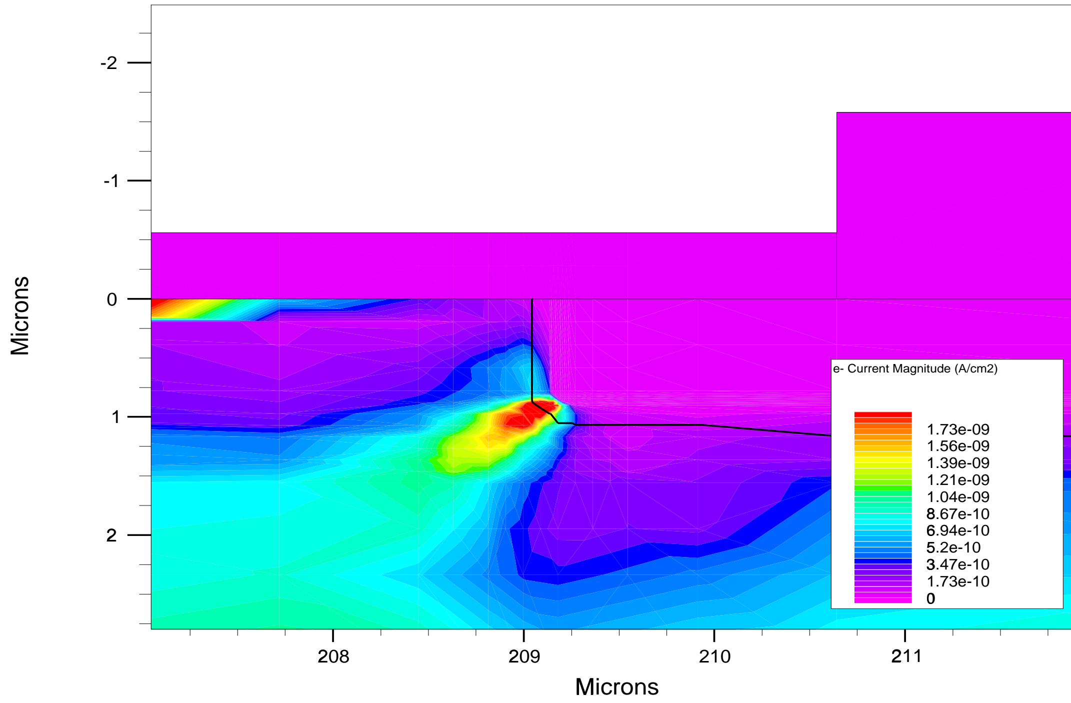

Figure 5: The electron current density plot evidences a carrier generation at the edge of the implant.

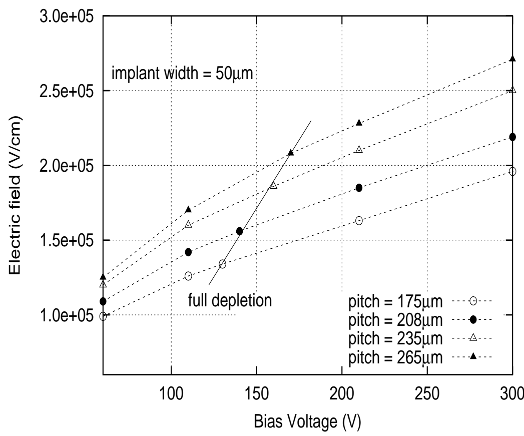

Figure 6: Magnitude of the electric field peak as a function of the applied voltage, for structures having an implant $50\,\mu m$ wide.

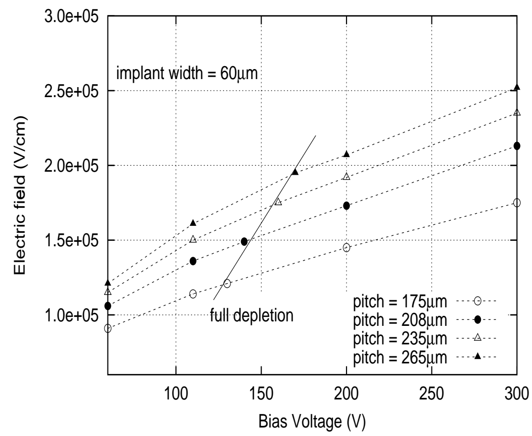

Figure 7: Magnitude of the electric field peak as a function of the applied voltage, for structures having an implant $60\,\mu m$ wide.

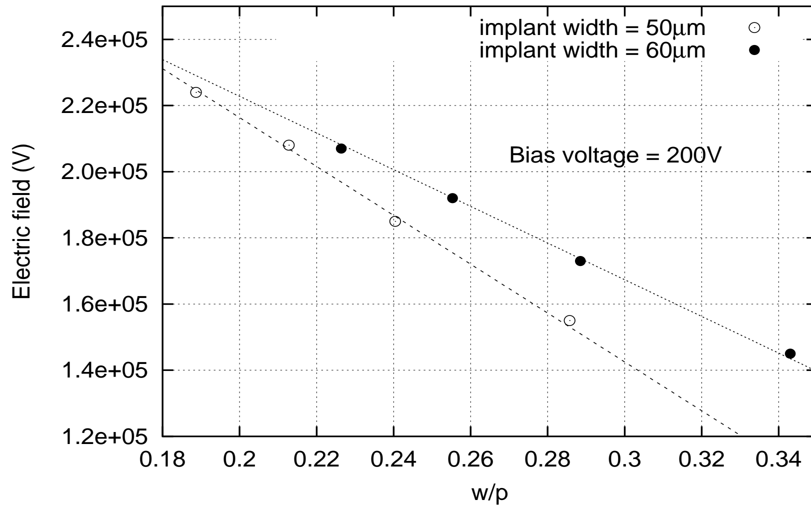

Figure 8: Electric field peak as a function of the width/pitch ratio.

Also the oxide charge density plays an important role: the higher the concentration the stronger the electric field. As an example, fig. 9 shows the effect of varying the oxide

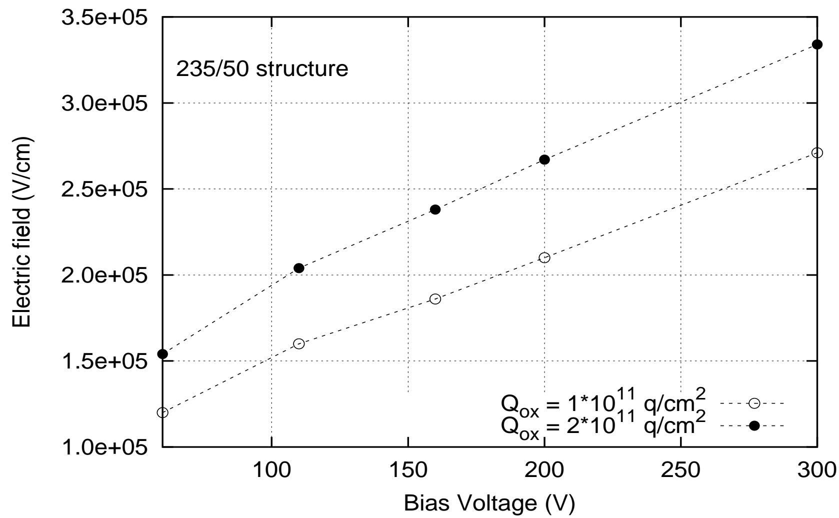

Figure 9: Electric field peak as a function of the bias voltage for different oxide charges.

charge density from 1×10^{11} to $2 \times 10^{11} q/cm^2$ for the $235/50$ structure. The higher concentration brings the electric field over the critical value when we apply more than $250V$.

4 AC analysis.

In order to verify the quality of the simulations, a comparison between the calculations and experimental data is performed. The data are taken from [4], where a careful experimental study regarding the capacitances is done. One of the tested structures is very similar to our detector, having a thickness of $410\,\mu m$ and a bulk resistivity of $6\,k\Omega$. The silicon is $< 111 >$-type, leading to a higher oxide charge concentration with respect to the $< 100 >$ crystal type foreseen for GLAST. Three structures with a constant width/pitch ratio, equal to 0.15, are measured. Figures 10, and 11 show a comparison between ex-

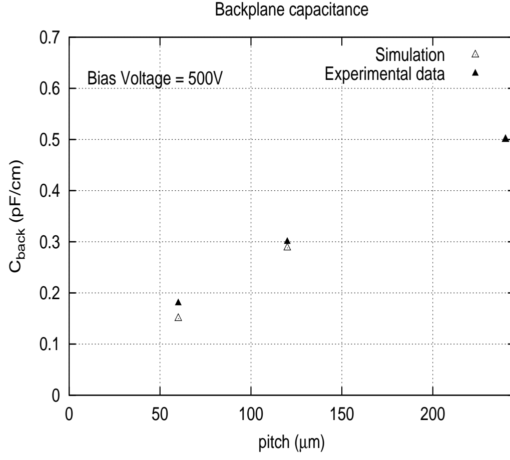

Figure 10: Backplane capacitance of the test detector.

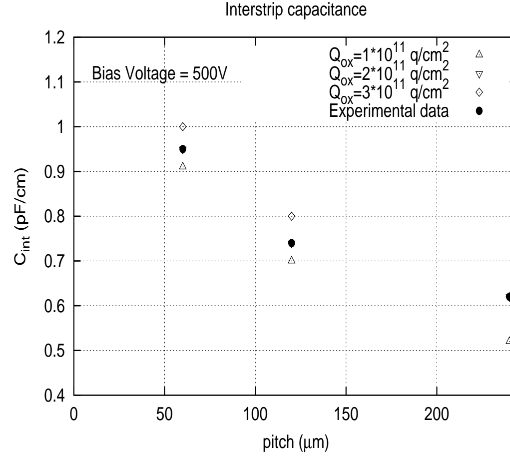

Figure 11: Interstrip capacitance of the test detector.

perimental data and simulation results for both interstrip and backplane capacitance. The agreement is found to be quite good, thus validating the simulation procedure. It is worth noting that the value of the interstrip capacitance depends on the electron accumulation layer under the $Si - SiO_2$ surface, that in its turn depends on many parameter. In particular, such parameters are: the fixed oxide charge density, the bias voltage, and the environmental humidity. It is quite difficult to estimate numerically the influence of the last parameter. In a qualitative way, negative charges (polarised water molecules) are collected on the uncovered oxide surface, partially compensating the positive oxide charge [5]. In our case the effective value of $Q_{ox} = 2 \times 10^{11}\, q/cm^2$ is found to fit in a proper way the experimental data.

Let's now simulate the capacitances of the structures listed in Table 1.

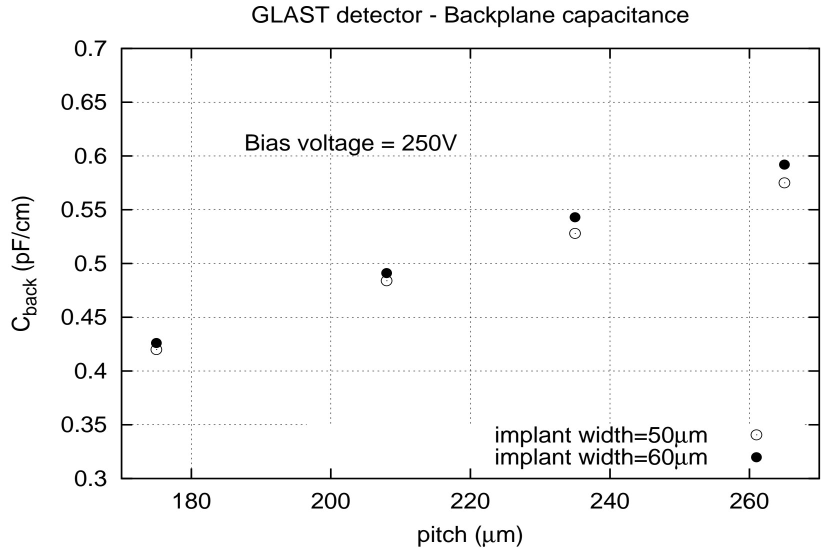

Figure 12: Backplane capacitance as a function of the pitch.

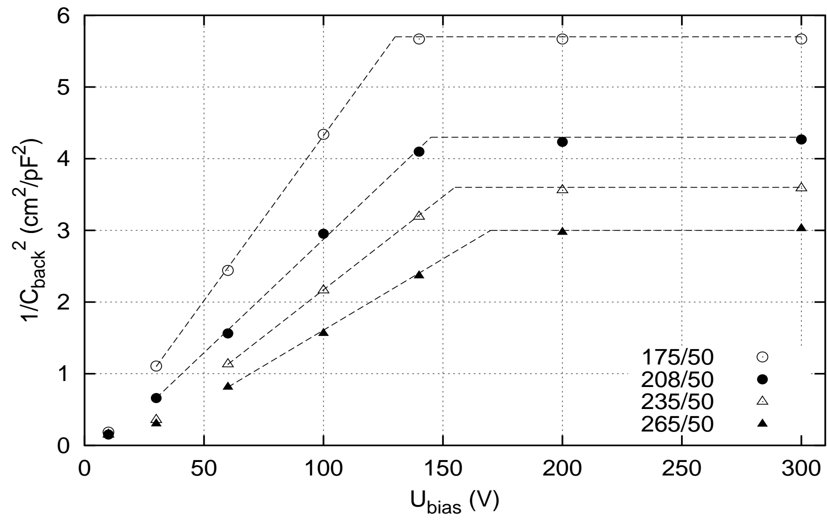

Figure 13: $1/C_{back}^2$ as a function of the bias voltage for structures having an implant $50\ \mu m$ wide.

Fig. 12 shows the backplane capacitance for a bias voltage of $250V$. It does not change substantially varying the width from 50 to $60\,\mu m$, while, as expected, increases with the pitch. C_{back} gives information concerning the depletion of the detector. Fig. 13 is a plot of $1/C^2_{back}$ as a function of the applied voltage for the structures having an implant $50\,\mu m$ wide. For each curve, the change of the slope indicates that the full depletion voltage of the detector is reached. Increasing the pitch from 175 to $265\,\mu m$ it rises from 130 to $170V$. These values depend slightly on the oxide charge concentration; in this case we used $Q_{ox} = 1 \times 10^{11} q/cm^2$.

The interstrip capacitance is plotted in figure 14. As one can see, the value depends consistently on both the implant width and pitch.

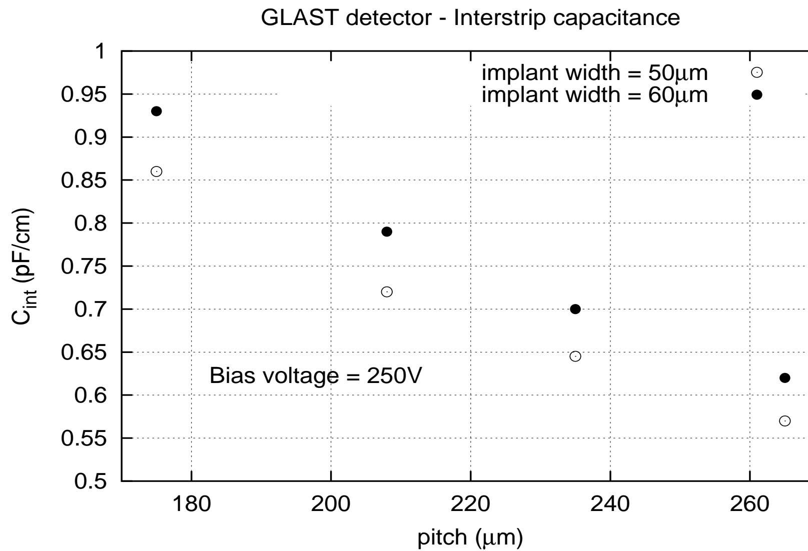

Figure 14: Interstrip capacitance as a function of the pitch using a bias voltage of $250V$ and an oxide charge $Q_{ox} = 1 \times 10^{11} q/cm^2$.

The total capacitance as a function of the pitch is presented in fig. 15. As it is evidenced experimentally in [4], this value depends only on the ratio between the two quantities, on the contrary to the electric field behaviour (fig. 8). The capacitance grows linearly with the w/p ratio, as demonstrated in fig. 16.

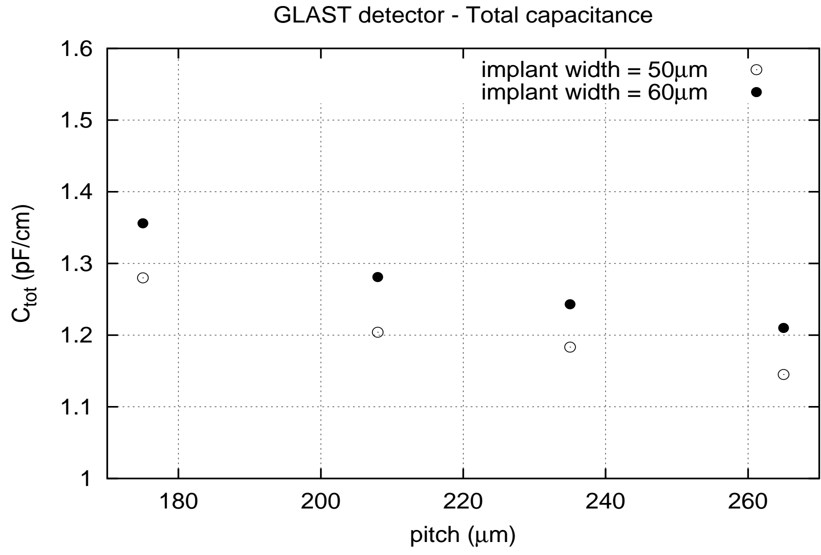

Figure 15: Total capacitance as a function of the pitch.

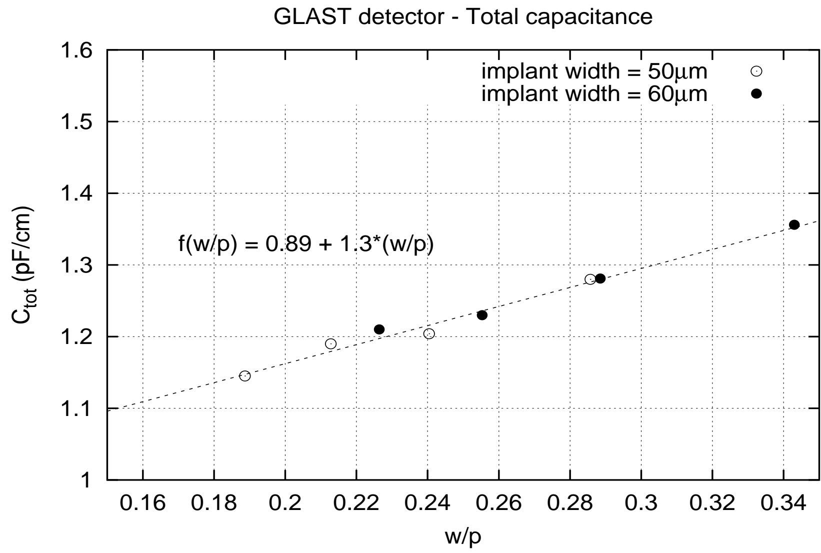

Figure 16: Total capacitance as a function of the width/pitch ratio.

5 Conclusions.

The results of the capacitance study indicate that the best-performing structure, among those analysed, has a pitch of $265\,\mu m$ and an implant $50\,\mu m$ wide. The DC analysis performed for this structure gives a maximum field under the critical value, being about $2.7 \times 10^5\,V/cm$ at a bias voltage of $300V$. Still, having such a high value of the electric field, we consider a pitch of $265\,\mu m$ as a limit for an implant width of $50\,\mu m$. For a larger pitch it is necessary to increase also the implant width.

6 Acknowledgements

The author would like to thank A. Vacchi for the continuous encouragement and support. Many thanks also to V. Bonvicini, L. Bosisio, and A. Rashevsky for the fruitful discussions.

References

[1] P. Michelson *et al.*, "GLAST LAT", Response to AO 99-OSS-03, Stanford Univ., (1999).

[2] E.D. Bloom *et al.*, "Proposal for GLAST", SLAC-R-522 (1998).

[3] SILVACO International, ATLAS User's manual (1998).

[4] CMS Collaboration, Addendum to the CMS tracker TDR, CERN/LHCC 2000-016 (2000).

[5] A. Bischoff *et al.*, Nucl. Instr. and Meth. **A326**, 27-37 (1993).