GLAST LAT PROCUREMENT SPECIFICATION	Document # **LAT-DS-00011-09**	Date Effective 9rd Draft – 3/27/01
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	Subsystem/Office Tracker	
Document Title **GLAST LAT Silicon Detector Specification**		

Gamma-ray Large Area Space Telescope

(GLAST)

Large Area Telescope (LAT)

Silicon Detector Specification

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes

1. PURPOSE

These Specifications will serve as the basis for the procurement of the GLAST LAT silicon strip detectors.

2. SCOPE

The specifications describe the layout, electrical and mechanical performance of the silicon strip detectors (SSD) for GLAST LAT and the tests required by the vendor.

3. DEFINITIONS

3.1 Acronyms

GLAST	Gamma-ray Large Area Space Telescope
LAT	Large Area Telescope
SSD	Silicon Strip Detector
TBR	To Be Resolved

3.2 Definitions

AC Coupling	The Al metal electrode is covering almost the whole length of the p+ implant, separated from it by a dielectric material
AC Pad	Pad to access the Al metal electrode on the strips
Active Area	Area of the Volume from which charge is collected on the strips in <<1us
Buyer	Institution procuring GLAST LAT SSD
C	Capacitance
Contract	Purchase agreement to procure GLAST LAT SSD's
Coupling Capacitor	Capacitor formed by Al metal electrode, dielectric and implant
Customer	Institution involved in the procurement and testing of GLAST LAT SSD's
C-V	Measurement of body capacitance (C) as a function of voltage (V)
DC coupling	Al metal electrode and implant in ohmic contact.
DC Pad	Pad to access the strip implant
Bias Resistor	Resistor connecting every implant to the bias ring
Bias Ring	Implant surrounding the active area, connects to bias resistors
Fiducial	Physical mark in the Al metal layers for alignment and metrology
Guard Ring	Implant ring outside the bias ring without bias connection ("floating")
I-V	Measurement of leakage current (I) as a function of voltage (V)
N-sub	Substrate contact on the detector front
Pad	Area of the Al metal layer accessible through the passivation The pad area is defined as the bondable area.
Pitch	Distance between strip centers
Passivation	Topmost layer covering of inert translucent material
Seller	SSD Manufacturer, Vendor
Sensor	Silicon Strip Detector (SSD)
um	Micro meter (10^{-6}meter)
us	Micro second (10^{-6}second)
V	Voltage, Volt

4. REFERENCES

GLAST LAT AO Response	P. Michelson *et al*, Nov 1999.
Strip Technology	T. Ohsugi *et al.*, NIM A, 383 (1996) 167.

BTEM prototype detectors	P. Allport *et al*, SLAC-Pub-8471, June 2000.
Flow-down of GLAST LAT SSD Spec's	H. Sadrozinski, SCIPP 00/33
Evaluation of LAT SSD Leakage Current Specification	LAT-TD-00122-01
LAT SSD Q/A Provisions	LAT-CR-00082-01
SSD Drawings	LAT-DS-00026-01
Test Structure Drawing	LAT-DS-00027-01

5. REQUIREMENTS

a. **Wafer**

i.	Doping	n-type
ii.	Surface orientation:	(1 0 0)
iii.	Wafer size:	6-inch
iv.	Bulk resistivity:	> 4 K? -cm
v.	Thickness:	400+20, -5 um
vi.	Bowing	<100um

b. **Type of the sensor**

i.	Coupling	AC
ii.	Biasing	Polycrystalline-silicon
iii.	Read-out	Single-sided
iv.	Read-out Implants	p+
v.	Surface covering (except for pads)	Passivation glass

c. **Sensor Size (nominal)**

i.	Outer size	8.95 cm x 8.95 cm
ii.	Dicing Tolerance	+- 20 um see LAT-DS-00026-01
iii.	Roughness of cut edge	< 10 um
iv.	Number of strips	384
v.	Strip pitch	228 um
vi.	Strip width (implant)	56 um
vii.	Width of strip Al electrode	64 um
viii.	Active area	87,552 um x 87,552 um
ix.	Uniformity of thickness of a single wafer	< 5 um

d. **Pads (sizes denote bondable area)**

i.	Position of bonding & probing pads	see Table 5.1 and LAT-DS-00026-01
ii.	Bias ring double row :	width 100 um x length 200 um

iii. DC pad on strip at connection of bias resistor 120um x 100um
iv. AC pads double row on both ends of the strip 100 um x 200 um
v. N-sub contact see LAT-DS-00026-01

e. **Process control of pads after automated ultra-sonic wire bonding with 25um Al wire**
i. Pull strength on wire >5grams, 7grams typ.
ii. No lift-off of pads
iii. Demonstrated # of bad channels due to wire bonding < 0.1%

f. **Processing Details**
i. Mask dimension error < 0.5 um
ii. Mask placement error in any direction: < 1.0 um*
iii. Bias ring implant ring DC coupled to an Al electrode.
iv. Guard ring: similar to the bias ring
v. Resistance of Al electrode on strips: < 50 ?
vi. Dielectric of coupling capacitor combination of SiO_2 + Si_3N_4
(preferred solution, different choice will be subject to electrical tests after wire bonding).
vii. Coupling capacitance: >500 pF
viii. Break down voltage of capacitor: >100V
ix. Bias resistance of poly-Si resistor: >20 M? ?< 80M?
x. Resistance variation within a detector <+- 10M? ?
xi. On the resistor side of the strips, the implants extend to within 40 micron of the bias ring.
* In lieu of satisfying the mask placement requirement, manufacturers can elect to test the DC current at 175V on every strip (see Sec 5.h.vii below)

g. **Fiducial marks 3 types, see** see Table 5.1 & LAT-DS-00026-01
i. Eye guiding mark: see LAT-DS-00026-01
Big box with "GLAST 2000 "Manufacturer"" followed by ID #, includes Mark C.
ii. The sensor ID is scratched on a binary scratch pad inside the Eye guiding box.

h. **Electric properties (at 25°C, humidity <60%, >40%)**
i. Full depletion voltage (measured by C-V): <150V, (<100V preferred)
ii. Leakage current per sensor at 150V, guard ring floating
Maximum: < 390nA
Averaged over every 100 detectors: < 200nA
iii. Breakdown voltage (change of slope of I-V curve) > 200V

iv. Total leakage current per sensor at 200V: < 500nA
v. Interstrip strip capacitance < 1.5pF/cm
vi. Interstrip isolation (@150V) > 1G?
vii. Single strip DC current < 10nA @175V
(applicable in case the manufacturer does not satisfy the 1um mask alignment requirement)

i. **Strip yield**

i. Bad channel rate (averaged over every 100 sensors): < 0.2%
ii. Maximum number of bad channels/sensor: < 3 channels (0.8 %)

(Note: Included in the bad channel count are:
short circuit of coupling capacitor
short circuit of strip implant or Al electrode to other strips or bias ring
open circuit of readout electrode
bad connection of bias resistor
strips with DC current >10nA @175V{in case the manufacturer does not satisfy the 1um mask alignment requirement})

j. **Implementation of test detectors and structures**

The following test detectors have to be implemented at the side of each full-size detector and supplied to GLAST LAT on a single cut-off.
Positioning is shown in LAT-DS-00027-01.

i. One narrow small ("Skinny") test detector (~5mm x 8.95cm) having all features of the full-size detectors, but only 8 strips, including fiducials etc. They are positioned next to the full size detector.
ii. One small ("Baby") test detector (~1.6cm x 3.5cm) having all features of the full-size detectors, including fiducials etc, but only 32 strips.
iii. One planar diode ~ 0.5cm x 0.5cm
iv. One gated diode ~ 0.5cm x 0.5cm
v. One MOS capacitor ~ 0.5cm x 0.5cm
vi. A bonding test area (~3.5 cm x 4mm) with 128 pairs of bonding pads.

k. **Information to be supplied for each sensor by vendor**

i. ID # scratched in the area provided on the full size detector
ii. ID # scratched in the area provided on the narrow small test detector
iii. Distances of edges parallel and normal to strips to fiducials "B".
iv. The total detector leakage current vs. bias voltage (I-V)

(in 5 volt steps up to 200V at 20 - 25°C, humidity <60%, > 40%)
and the measurement temperature.

v. A list of bad channels with their defects indicated

(Coupling capacitors tested up to +100V on AC pad, bias pad grounded)

vi. The body capacitance vs. bias voltage (C-V)
(in 5 volt steps up to 200V at a frequency of 1kHz)

vii. The depletion voltage extracted from the C-V plots

viii. Information supplied with every batch

Measured resistance values of poly bias resistor and Al electrode in the batch (average, minimum, maximum)

Tracebility data of processing (relative yield, start and end date, …) and wafer (batch number, boule QC, …).

l. **Radiation hardness**

The radiation hardness will be verified by GLAST LAT on the small test detectors. Those samples will be exposed to gamma-rays from a ^{60}Co radiation source up to 100 Gy in biased condition. The irradiated sample detector shall satisfy the following requirements (@150V, 25°C, humidity <60%, > 40%):

i. Total leakage current < 120nA/cm^2
ii. Total strip capacitance < 1.6pF/cm
iii. Interstrip isolation > 1G?

Table 5.1

GLAST2000 Location of Pad & Fiducials
(for reference only, see LAT-DS-00026-01)

(Ctr of Pad or Mark on left side only, dimensions in micron, size denotes bondable area)

X is normal to strips, y along strips
(0,0) is in the center of the detector
Resistor end is at negative y.

		Non-Resistor End		Resistor End	
	Size (x*y)	x	y	x	y
Pads					
First Bond	100x200	-43662	43615	-43662	-42940
First Probe	100x200	-43662	43315	-43662	-42640
DC	120x100	n.a.	n.a.	-43662	-43240
Bias 1	100x200	-43890	43615	-43890	-42940
Bias 2	100x200	-43890	43315	-43890	-42640
Fiducials					
Bond	"A"	-44550	43615	-44550	-42940
Probe	"A"	-44550	43315	-44550	-42640
Alignment	"B"	-44550	44450	-44550	-44450
Metrology	"C"	-44550	39750	-44550	-39750
Eye guiding mark	400 x 9900				

Pads are bondable area
Detector edge x = +- 44750 or y = +-44750
N-sub (Substrate contact) : 88000 x 200 with center at (0,- 44500) and at (0,+ 44500)
Metal cover plate within 150micron outside of outer edge guard ring, metal overhangs n-sub by 20um.
Bias ring contact along the entire detector width at the resistor side.

6. VERIFICATION STRATEGY

The verification strategy will test, inspect, or demonstrate all requirements of section 5 to ensure that the SSD meet their specified requirement. The matrix below indicates the methods of verification employed to verify the SSD technical performance.

Table 6-1. Requirements Verification Matrix

Summary of Requirements and Validation

Note: Verification Methods are

PC Process Control
DC Design Control
MAI Manuf/ass'y Inspection
MPMI Manuf/ass'y Prototype Mask Inspection
DI Delivery Inspection
ST Sample Test

Req't #	Requirement	Parameter	Validation	Verification
5.a.i	Doping	n-type	Prototype 99/00	PC
5.a.ii	Surface orientation	(1 0 0)	Prototype 99/00	PC
5.a.iii	Wafer Size	6"	Prototype 00	PC
5.a.iv	Bulk resistivity	>4 K? -cm	Prototype 00	MAI
5.a.v	Thickness	400 ?m	Prototype 00	MAI
5.a.vi	Bowing	<100 ?m	Prototype 00	MAI
5.b.i	Coupling	AC	Prototype 99/00	DC
5.b.ii	Biasing	Polycrystalling-silicon	Prototype 99/00	DC
5.b.iii	Read-out	Single-sided	Prototype 99/00	DC
5.b.iv	Read-out Implants	P+	Prototype 00	PC
5.b.v	Surface covering (except for pads	Passivation glass	Prototype 00	PC
5.c.i	Outer Size	8.95x8.95 cm	Prototype 00	MAI, DI
5.c.ii	Dicing Tolerance	+-20 ?m	Prototype 00	MAI, DI
5.c.iii	Uniformity of saw cut	< 10 ?m	Prototype 99/00	MAI
5.c.iv	Number of strips	384	Prototype 00	MPMI
5.c.v	Strip Pitch	228 ?m	Prototype 00	MPMI
5.c.vi	Strip Width (implant)	56 ?m	Prototype 00	MAI
5.c.vii	Width of AL Electrode	64 ?m	Prototype 00	MAI
5.c.viii	Active Area	87,552 ?m x 87,552 ?m	Prototype 00	MAI
5.c.ix	Uniformity of thickness	<5um	Prototype 00	MAI
5.d.i	Position of bonding and probing pads	See Table 5.1	Prototype 00	MPMI
5.d.ii	Bias ring double row	Width 120 ?m x length 200	Prototype 00	MPMI

		?m		
5.d.iii	DC pad on strip at connection of bias resistor	100 ?m x 100 ?m	Prototype 00	MPMI
5.d.iv	AC pad double row on both ends of the strip	100 ?m x 200 ?m	Prototype 00	MPMI
5.d.v	N-sub contact	See LAT DW-00026-01	Prototype 00	MPMI
5.e.i	Pull strength on wire	>5 grams, 7 grams typ.	Prototype 00	MAI, ST
5.e.ii	No pad lift-off		Prototype 00	MAI, ST
5.d.vi	Bad Channels due to bonding	<0.1%	Prototype 00	MAI, ST
5.f.i	Mask dimension error	<0.5 ?m	Prototype 00	MPMI
5.f.ii	Mask placement error	<1.0 ?m	Prototype 00	MPMI
5.f.iii	Bias Ring	Implant ring DC coupled to Al electrode	Prototype 00	DC
5.f.iv	Guard ring	Similar to the bias ring	Prototype 00	DC
5.f.v	Resistance of AL electrode on strips	<50 ?	Prototype 00	MAI, ST
5.f.vi	Dielectric of coupling capacitor	Combination of SiO_2 + Si_3N_4	Prototype 00	DC
5.f.vii	Coupling capacitance	>500pF	Prototype 00	MAI, ST
5.f.viii	Break down voltage of capacitor	>100 V	Prototype 00	MAI, ST
5.f.ix	Bias resistance of poly-Si resistor	> 20 M? ,< 80 M?	Prototype 00	MAI, ST
5.f.x	Resistance variation with in a detector	<+- 10 M?	Prototype 00	MAI, ST
5.f.xi	On the resistor side of the strips, the implants extend to	<40 ?m	Prototype 00	MPMI
5.g	Fiducial marks position & size	See table 5.1 & LAT-DS-00026-01	Prototype 00	MPMI
5.g.i	Eye guiding mark	See LAT-DS-00026-01 Big box with "GLAST 2000 "Manufacture"" followed by ID #, Includes Mark C	Prototype 00	MPMI

5.g.ii	Sensor ID	Scratched on binary scratch pad inside the Eye guiding box.	Prototype 00	MPMI, MAI
5.h	Electric properties	At 25 deg. C, humidity <60%, >40%	Prototype 00	Test Parameters
5.h.i	Full depletion voltage	<150V (<100) measured by C-V	Prototype 00	MAI, ST
5.h.ii	Maximum Leakage current per sensor	<390nA measured at 150 V with guard ring floating	Prototype 00	MAI, DI
	Leakage current per sensor averaged over 100 detectors	<200nA measured at 150 V with guard ring floating	Prototype 00	MAI, DI
5.h.iii	Breakdown Voltage	>200V	Prototype 00	MAI
5.h.iv	Total Leakage current per sensor	<500nA @ 200V	Prototype 00	MAI
5.h.v	Interstrip strip capacitance	<1.5 pF/cm	Prototype 00	MAI, ST
5.h.vi	Interstrip isolation	>1G? @150V	Prototype 00	MAI, ST
5.i.i	Bad channel rate	<0.2% (ave over every 100 sensors)	Prototype 00	MAI, ST
5.i.ii	Maximum number of bad channels/sensor	<3 channels (0.8%)	Prototype 00	MAI, ST
5.j	Test Detectors implementation	Implemented at the side of each full-size detector (see LAT-DS-00027-01	Prototype 00	MPMI
	Test Detector Delivery	Supplied to GLAST LAT on a single cut-off	Prototype 00	DI
5.j.i	One narrow test("skinny")	(~5 mm x 8.95 cm) all features of full-size detector, including	Prototype	MPMI

		fiducials etc, but only 8 strips.		
5.j.ii	One small test("Baby")	(~1.6 cm x 3.5 cm) all features of full-size detector, including fiducials etc, but only 64 strips.	Prototype	MPMI
5.j.iii	One planar diode	~0.5 cm x 0.5 cm	Prototype 00	MPMI
5.j.iv	One gated Diode	~0.5 cm x 0.5 cm	Prototype 00	MPMI
5.j.v	One MOS capacitor	~0.5 cm x 0.5 cm	Prototype 00	MPMI
5.j.vi	A bonding test area	~3.5 cm x 4mm with 128 pairs of bonding pads	Prototype 00	MPMI
5.k	Information to be supplied for each sensor by vendor			DI
5.k.i	Date, batch number etc		Prototype 00	MPMI, MAI, DI
5.k.ii	Full side Detector ID #	Scratch in the area provided on the detector	Prototype 00	MPMI, MAI, DI
5.k.iii	Narrow small test detector ID#	Scratched in the area provided on the detector	Prototype 00	MPMI, MAI, DI
5.k.iv	Total leakage current measurement	Total Detector leakage current vs. bias voltage (I-V) in 5V steps up to 200V @, humidity <50%	Prototype 00	MAI
5.k.v	Bad channel list	List of bad channels with indicated defects (coupling capacitors tested up to 100V	Prototype 00	MAI
5.k.vi	Resistance	Resistance of	Prototype 00	MAI, ST

	Measurement	one full-size bias resistor		
5.k.vii	Body capacitance measurement	Body capacitance vs. bias voltage (C-V)	Prototype 00	MAI, ST
5.l.i	Total Leakage current at 100Gy	<120 nA/cm^2	Prototype 00	MAI, ST
5.l.ii	Total strip capacitance at 100Gy	<1.6pF/cm	Prototype 00	MAI, ST
5.l.iii	Interstrip isolation at 100Gy	>1G Ohm	Prototype 00	MAI, ST

7. QUALITY ASSURANCE PROVISIONS

Quality Assurance (Q/A) and details of testing, delivery, shipping, handling etc are covered in LAT-CR-00082.