Signal-to-Noise Ratio in GLAST

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We are using the beam test data of the tracking efficiency in the GLAST BTEM and bench tests of the noise occupancy and trigger rates to derive a specification for the signal-to-noise ratio S/N for GLAST.

Signal

Figure 1 shows the tracking efficiency for electrons in layer 0 of BTEM, as a function of the threshold voltage. The efficiency is constant for thresholds values below 170V, the nominal threshold, corresponding to about 1.3fC, given a gain of about 130mV/fC. The median charge (50% efficiency) is at about 750mV, corresponding to 5.7fC, close to what is expected for 400micron thick detectors. (N.B.: the absolute calibration from threshold to charge is not important, as long as one uses consistently one scale for signal and noise.)



Fig. 1: The efficiency in layer 10 versus threshold, measured during the beam test from single electron tracks at normal incidence. The efficiency for each of the first three threshold values is greater than 99.9% for both the x and y layers. Inefficiency due to dead areas between detectors is not included.

The difference between the operating threshold and the threshold at which no performance degradation is observed is the threshold margin or "head room". Note that

we should check the same plot for inclined tracks where we expect less deposited charge (see below). We can define an efficiency floor, below which we don't want to operate the detector. Consideration of the trigger and the efficiency of the tracking sets the efficiency floor at the 98% level, which from Figure 1 is, at normal incidence, a threshold at 250mV, i.e. 1.9fC. With an efficiency floor of 95%, the threshold at normal incidence would be at 340mV, i.e. 2.6fC.

Noise

Figure 2 shows the noise rate as a function of threshold for three single channels and for the layer 0 OR with only 4 out of 1600 (0.25%) channels masked. Fig 3 shows the expected exponential behavior in the square of the threshold, with a noise RMS of 23.4mV, corresponding to 0.18fC, or about 1111 electrons. Taking into account noise contributions from the bias resistors, the finite resistance of the aluminum strip, the shot noise from the leakage current, this corresponds to a noise slope of 21.5 e-/pF and an offset of 140e-. This is somewhat lower than in previous chips, but has been confirmed by measurements on the new amplifier chip fabricated in 0.5micron CMOS.



Fig. 2 Noise rate from three individual channels and from the OR of three layers with no concurrent digital activity.

One can calculate an expected noise rate using the single channel noise rate from Fig. 2, and compare it with the observed rate of the OR, assuming an effective pulse width (ToT) of 300ns, as one would expect of the noise. This is done in Table 1, (where we converted the rates into occupancy in 0.3μ s time buckets,) and a reasonable agreement within a factor two is seen. The fact that the observed rate is larger than the calculated one might be due to a few channels with higher rate, or due to our assumption of the same gate

width for the two cases. It is also clear that at the nominal threshold of 170V, the layer 0 OR is entirely due to cosmic rays, i.e. we have plenty of "noise margin".



Fig 3: Noise rate vs. square of the threshold, showing good agreement with a gaussian behavior.

Table 1: Noise rates vs. Threshold:
Single channel, calculated Plane OR, observed Plane OR

Vthr	Singles	Singles Occ	OR Occ		16Tower
[mV]	Rate [Hz]	(0.3us)	calc	obs	Rate [Hz]
					in 500ns
94	180	5.4e-5	0.083	0.15	4.4k
104	20	6.0e-6	0.0095	0.024	<<1
115	2.0	6e-7	0.00096	0.003	<<1

Scaling of threshold values: Noise

As shown in Fig. 3, the noise rate is an almost gaussian function (actually an error function) of the ratio threshold voltage V_{th} over noise RMS σ :

Noise rate
$$\propto \exp(-0.5^{*}(V_{th}/\sigma)^{2})$$

.Thus the noise rate will stay the same if the ratio V_{th}/σ is kept constant. If the noise RMS increases, the threshold has to be changed by the same amount to keep the noise rate the same. What constitutes an acceptable noise rate in the plane OR? From Fig. 2 and Table

1, we find a layer noise occupancy of about 15% at 94mV, which gives a total noise rate for 16 towers of about 4.4kHz in a 500ns wide gate. At just slightly larger thresholds (e.g. 100mV), the 6 fold coincidence in 16 towers is negligible. There are several reasons why one would set the noise floor at a higher threshold: the final tracker trigger might be looser than planned now, for example due to mis-functioning layers, and to allow for threshold mis-match. The efficiency of the trigger requires that the deadtime of the OR's is fairly small, and we set the requirement for the noise occupancy to be 1%. From Fig 2, we see that for the BTEM, 1% occupancy in 1us is achieved at a threshold of 115mV. The difference between this minimum threshold (required to keep the noise occupancy down), which we call the noise floor, and the operating threshold is the noise margin. For the base line detectors with 36cm long strips, the noise floor has to be increased relative to the BTEM by the ratio of the respective noise RMS. In Table 2, we show the noise floor for different projections of the noise RMS. For example, the noise in the baseline silicon detectors will increase with respect to BTEM from 1111e- to 1233e-, and the noise floor will increase from 115mV to 128mV. At end-of-mission and 5x design margin of radiation dose, due to increase in leakage current, the noise floor will increase to 171mV at an operating temperature of 25deg C.

Increased Pitch

In Table 2 we have included the noise for three choices for the pitch (201, 235 and 282um). We assumed that the detectors with 235 and 282um pitch would be manufactured to a relatively safe geometry which tries to minimize breakdown. This is primarily an issue of the gap between the strips, which tends to enhance the maximum filed on the implants. Preliminary results from field calculations by T. Ohsugi indicate that an implant width of 64micron is as safe as the implant width of w=52micron on the present detectors of p=208micron pitch. (A reminder: in the 1997 beam test we employed detectors with 236micron pitch and 57micron implant). A much more tenuous extrapolation of the data to a pitch of p=282micron yields an implant width of w=100micron. We have been encouraged by experiences of the CMS project (LHC) with implants as low as 30micron on 240micron pitch. The projected capacitances are taken from the CMS data (CMS 2000-011) and are mainly a function of w/p, with a small dependence on the pitch. The resulting noise floors are given in Table 2, at the start of the program, and at end-of-mission for 1x and 5x radiation level design margins, respectively. Increasing the pitch actually decreases the noise occupancy requirement on the single channel, because the number of channels decreases (Table 2).

Scaling of the threshold values: Inclined tracks

For inclined tracks, the detector collects less charge and is less efficient at the nominal threshold. Any noise margin can be used to lower the threshold accordingly. The largest angle of incidence we can trigger on in the 3-trays-in-a-row trigger is 80deg relative to the normal. From simple geometric considerations, at large angles of incidence, the pulse height is determined by the pitch instead of the detector thickness. As shown in Table 2, the collected charge is then only 51% for 201micron pitch, 60% for 235micron and 72% for 282micron pitch. Thus the efficiency floor for 201 micron is decreased from 250mV to 127mV, while the one for 235 and 282micron pitch are 149 and 179mV, respectively. Clearly we should require that the efficiency floor be larger than the noise floor. Yet, the

end of mission noise floors for 1x (5x) radiation level design margin is 134mV (171mV) for 201micron pitch, 141mV (181mV) for 235micron pitch and 167mV (209mV) for 282micron pitch, indicating that the base line has no margin and can not satisfy the signal-to-noise requirements for inclined tracks. In all cases, the end-of-mission efficency at 5x design margin is below the desired 98%, with the pitch of 235micron showing the best performance.

It is important to check the efficiency for inclined tracks in the beam test data, to verify the drop in efficiency at the nominal threshold. Due to the fact that photon conversions yield two tracks rather than one, the trigger efficiency for photons might be much higher than assumed here. On the other hand, the need for high efficiency for tracking is still valid. Using the scaling employed above, we expect that for tracks with large incident angles in the BTEM, the efficiency at the nominal threshold of 170mV will be about 95% (effective threshold = 320mV, see Fig. 1).

Table 2 presents the relevant data for all three pitch values considered.

Pitch P [micron]	201	235	282
# of Channels per layer	1792	1536	1280
Channel Occ for 5% plane Occ	2.9 e-5	3.3 e-5	4.0 e-5
Channel Occ for 1% plane Occ	5.6 e-6	6.5 e-6	7.9 e-6
Width W [micron]	50	64	100
W/P	0.25	0.272	0.355
Capacitance/L c [pF/cm]	1.3	1.38	1.65
Noise RMS [e-]	1233	1284	1472
Signal @ 0deg [e-]	32,000	32,000	32,000
S/N	26.0	24.9	21.7
98%Efficiency Floor@0deg	250mV	250mV	250mV
Signal @80deg: S80	50.8%	59.7%	71.6%
98%Efficiency Floor @80deg	127mV	149mV	179mV
Noise Floor [mV]	128 /134 /171	133 /141 /181	152 /167 /209
Start / End 1x / End 5x			
End of Mission Efficiency,	98% / 96%	98% / 97%	98% / 95%
(25degC, 80deg Incl,) 1x / 5x			

Table 2 : Signal-to-Noise Comparisons for three Pitch Values

Conclusions

The BTEM data on tracking efficiency and noise rate (both for single channels and the plane OR) are used to predict signal and noise for the GLAST tracker. For normal incident photons, the noise margin will be very high. The limit on the efficiency comes from photons with large angle of incidence, and here detectors with pitch larger than the base line exhibit a somewhat larger noise margin. From trigger dead time consideration, we propose to set the noise rate such that the plane OR occupancy is limited to 1%. This will automatically guarantee a negligible noise rate of the tracker trigger.