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# Cells of the GTFE64C Design

This is a list of cells in the design of the GLAST Tracker front-end readout chip that was used in the BTEM Tracker. Included are some comments relevant to how the design can be migrated to a new process.

First a comment on the power and ground division. All of the amplifier-discriminator cells and the mask registers and DACs are on the analog power and ground. Only digital cells that switch during data taking, such as the command decoder, FIFO, output registers, and I/O circuits, are on the digital power and ground.

1. Standard CMOS logic gates and tri-state drivers, which were taken from the CMOSX standard library. These are used only in the command-decoder block.
2. Two D flip flops, one with set, one with reset, taken from the CMOSX standard library and used only in the command-decoder block.
3. Logic gates (AND2, NAND2, OR2, NOR2, NOT) of various drive capability, some with digital power and ground, some with analog power and ground, which were custom drawn. These can probably be replaced by standard cells from a library, but we will have to have two versions of some of the cells in order to keep those used on the analog half of the chip connected to the analog power supply and ground. The two versions might not be necessary in an SOI process (see below).
4. Power-on reset circuit, to generate a reset pulse when the power turns on. There are two versions, one on the digital supply, the other on the analog supply.
5. Voltage stepping circuit, to take digital signals from the digital side of the chip, with VDD=3V to the analog side of the chip, with VDD=5V. This is not needed in the new design, where both digital and analog supplies will be VDD=3.3V. However, it will be necessary in the case of an SOI process, where we truly isolate the analog and digital ground, to design a differential handoff of the digital signals that have to go into the analog section. Alternatively, in an SOI process we might keep *all* digital cells on the digital power and ground, which would require routing those up around all sides of the analog section to reach the calibration masks and so forth.
6. Differential receiver for clock and trigger signals arriving from the controller chip. There are two versions: one with power on/off capability and the other without. Associated with this is a bias circuit that includes a 48K resistor (to make the power consumption less sensitive to the input supply level than one would have with a purely MOSFET circuit).

7. 6-bit DAC with two ranges. This is purely a custom design that works by addition of currents. It includes some resistors, but the DAC setting depends on ratios of resistors and is not sensitive to the absolute value of resistance. Two versions, for threshold and calibration, differ only in load section, where the current is turned into a voltage.
8. Configuration register memory cell. There are two versions, one with set, one with reset, in order to implement the default configuration setting. This needs to be replaced with a custom SEU-safe cell. In the new design there are 209 instances, of which 71 used for calibration don't really need to be SEU-safe. However, it may be simplest to make all of them the same.
9. Chip-to-chip differential driver-receiver pair.
10. Analog amplifier-discriminator chain, plus bias circuit.
11. CMOS switch for the injection of the calibration charge into the test-input capacitor of the preamp.
12. Output shift-register cell with parallel load.
13. Clock generator with dual-non-overlapping clocks for the output shift register.
14. Clock generator with dual-non-overlapping clocks for the FIFO pointer registers.
15. Pointer register cell for addressing the FIFO (the read and write pointers). This register has to be modified to encode and output the addresses with the data, as well as to reduce the FIFO from 8 events to 4 events.
16. Dual-ported FIFO memory cell.