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September 16, 2000

Road Map for Redesign of the GTFE64 Chip

1) HP 0.5 micron analog test chip
   a) Design, layout, fabrication (Vallon). Done.
   b) Performance testing (Masa). Done.
   c) SEL testing (Tsune). Done.
2) Analog/Digital test chip
   a) Design, layout, fabrication (Vallon). Done.
   b) Test board layout. Done.
   c) Testing: noise, functionality of digital cells, crosstalk, SEL/SEU?
3) Command Decoder test chip
   a) Design and simulation (Robert/Ned). Done.
   b) Layout, fabrication (Ned). Done.
   c) Testing of functionality. Nearly done.
   d) SEL testing?
4) New Front-end test chip
   a) Design and simulation (Dieter). Done.
   b) Design review. Done.
   c) Test-chip layout and fabrication in HP 0.5 micron. Done.
   d) Test-chip layout and fabrication in Peregrine. In progress.
   e) Testing.
5) System Design
   a) Requirements and specifications (Robert). In progress.
   b) Block diagrams.
   c) System description.
   d) Interface specifications.
   e) Grounding and shielding plan.
   f) Preliminary test plan.
   g) Cost estimate and schedule.
   h) Design review.
6) GTFE64D design and layout
   a) Tanner standard cells (Ned)
      i) Enter the Tanner transistor-level schematics into the Viewlogic builtin logic symbols, separately for cells on digital and analog supplies.
      ii) Modify the layout of cells on the digital supply to separate the substrate contact from the digital ground return.
   b) FIFO/output register (Ned, Robert)
      i) Add two columns at each end for trigger code (done)
      ii) Add trigger code input to the symbol (done)
      iii) Replace CMOS output drivers with a single standard-cell inverter (done)
      iv) Move all non-standard-cell schematics for this block to a separate library (done)

v) Update transistor-level schematics for new process (done by Ned, but needs to be combined with Robert’s work).

vi) Simulate a reduced schematic in Spice?

vii) Update the VHDL models for the RAM and output registers

viii) Layout in Tanner and DRC/LVS. (Done for all blocks in the old design. Needs update for the new schematic.)

c) Amplifier/discriminator cell and analog bias cell (Dieter, Dave)

i) Finalize the layout for the full chip (done?)

ii) Incorporate the new design into the full Viewlogic schematic.

d) Configuration register

i) Make a schematic of an SEU-safe D-flip-flop and simulate in Spice as a shift register.

ii) Check the Viewlogic digital model for D-flip-flops for correct behavior and timing.

iii) Make a standard-cell layout for the SEU-safe flip-flop.

iv) Make Viewlogic schematics of the reset and preset register cells, with non-destructive read capability.

v) Make Viewlogic schematics of each of the 5 registers.

vi) Check specifications of the register default settings.

e) Calibration mask

i) Update the CMOS switch schematic for the new process

ii) Translate the CMOS switch layout to Tanner and update as necessary.

iii) Combine the CMOS switch layout with the configuration-register cell layout and a Tanner standard gate to make a cell of the calibration mask.

f) Trigger and Data Masks

i) Combine the configuration-register cell with Tanner standard logic cells to make the mask cell.

g) Command decoder (Ned, Robert)

i) Test the chip done in Tanner by Ned.

ii) Reverse the order of the command and address bits.

iii) Break the load and read register commands up into 5 separate commands each.

iv) Add a signal to the read register commands to parallel shift from the configuration registers to the readout registers before starting the output clock.

v) Replace all logic cells with Tanner standard cells, putting all command-decoder schematics into a separate library.

vi) Check the digital simulation of all cells.

vii) Update the Tanner schematic to be identical.

viii) Run a Spice simulation of the whole block, if possible.

ix) Auto place and route, DRC, and LVS against both the Tanner and Viewlogic schematics.

h) Trigger receiver

i) Make and simulate a Viewlogic schematic of a state machine to pull the trigger ID bits from the bit stream, using standard logic cells. (done)

ii) Check the design with a Spice simulation, using Tanner standard cells.

iii) Enter the schematic into Tanner and auto place and route the block. LVS against the Viewlogic schematic.

i) Voltage-translator cell.

i) Check the existing cell for compatibility with requirements in the new process.

ii) Update the schematic for the new process.

iii) Simulate the cell in Spice.

iv) Translate the layout into Tanner and update, if necessary.

j) Power-on-reset cells

i) Document and check the timing requirements.

ii) Update the schematics for the new process.

iii) Simulate in Spice and check against the requirements.

iv) Translate the layout to Tanner and update as necessary.

k) Pad frame

i) Fix the chip long dimension (done)

ii) Estimate the short dimension and prepare a Auto-Cad drawing of the desired pad layout (Gwelen, in progress)

iii) Specify the input-protection requirements.

iv) Modify the Tanner standard cells to fit our needs and requirements.

l) I/O cells

i) Revise the resistor layout to give the correct resistance in the new process.

ii) Revise the logic (using Tanner standard cells) for the trigger-input power-off according to the new number of chips on the hybrid (i.e. chips with address 0 and 23 should turn off their trigger inputs).

iii) Simulate the data shift register with the low-voltage chip-to-chip driver and receiver.

iv) Import the chip-to-chip drivers and receivers, clock and trigger receivers, bias circuit, and tri-state output driver cells into Tanner and modify as necessary.

m) DACs

i) Specify the gains (Wilko)

ii) Modify the schematics to use the new configuration register.

iii) Import the cell layouts into Tanner and modify as necessary.

n) Global schematic

i) Move only schematics actually used to new libraries, putting major blocks separately into special libraries.

ii) Replace all standard logic and driver cells (that have not already been done in sub-blocks) with Tanner library cells, using a minimum set of different driver sizes.

iii) Update the VHDL models of all modules that have changed in design.

iv) Simulate digitally the full chip with all commands and features.

v) Simulate 3 chips triggering and reading out together.
vi) Simulate a chip together with the GTRC VHDL model
vii) Make sure that each sub-module (such as a shift register or a command decoder) buffers all input signals that fan out internally.
viii) Check the fanout of each driver, develop a rule for needed driver strength, and size the drivers accordingly.

o) Global layout and routing
i) Place each of the blocks in roughly the same arrangement as in the GTFE64C chip.
ii) Check the drivers of each global-routing trace for adequate drive, and update the schematic and layout if necessary.
iii) Build up the pad frame, and complete the internal routing.
iv) Full-chip DRC and LVS.

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July 10, 2000

Cells of the GTFE64C Design

This is a list of cells in the design of the GLAST Tracker front-end readout chip that was used in the BTEM Tracker. Included are some comments relevant to how the design can be migrated to a new process.

First a comment on the power and ground division. All of the amplifier-discriminator cells and the mask registers and DACs are on the analog power and ground. Only digital cells that switch during data taking, such as the command decoder, FIFO, output registers, and I/O circuits, are on the digital power and ground.

1. Standard CMOS logic gates and tri-state drivers, which were taken from the CMOSX standard library. These are used only in the command-decoder block.
2. Two D flip flops, one with set, one with reset, taken from the CMOSX standard library and used only in the command-decoder block.
3. Logic gates (AND2, NAND2, OR2, NOR2, NOT) of various drive capability, some with digital power and ground, some with analog power and ground, which were custom drawn. These can probably be replaced by standard cells from a library, but we will have to have two versions of some of the cells in order to keep those used on the analog half of the chip connected to the analog power supply and ground. The two versions might not be necessary in an SOI process (see below).
4. Power-on reset circuit, to generate a reset pulse when the power turns on. There are two versions, one on the digital supply, the other on the analog supply.
5. Voltage stepping circuit, to take digital signals from the digital side of the chip, with VDD=3V to the analog side of the chip, with VDD=5V. This is not needed in the new design, where both digital and analog supplies will be VDD=3.3V. However, it will be necessary in the case of an SOI process, where we truly isolate the analog and digital ground, to design a differential handoff of the digital signals that have to go into the analog section. Alternatively, in an SOI process we might keep *all* digital cells on the digital power and ground, which would require routing those up around all sides of the analog section to reach the calibration masks and so forth.
6. Differential receiver for clock and trigger signals arriving from the controller chip. There are two versions: one with power on/off capability and the other without. Associated with this is a bias circuit that includes a 48K resistor (to make the power consumption less sensitive to the input supply level than one would have with a purely MOSFET circuit).

7. 6-bit DAC with two ranges. This is purely a custom design that works by addition of currents. It includes some resistors, but the DAC setting depends on ratios of resistors and is not sensitive to the absolute value of resistance. Two versions, for threshold and calibration, differ only in load section, where the current is turned into a voltage.
8. Configuration register memory cell. There are two versions, one with set, one with reset, in order to implement the default configuration setting. This needs to be replaced with a custom SEU-safe cell. In the new design there are 209 instances, of which 71 used for calibration don't really need to be SEU-safe. However, it may be simplest to make all of them the same.
9. Chip-to-chip differential driver-receiver pair.
10. Analog amplifier-discriminator chain, plus bias circuit.
11. CMOS switch for the injection of the calibration charge into the test-input capacitor of the preamp.
12. Output shift-register cell with parallel load.
13. Clock generator with dual-non-overlapping clocks for the output shift register.
14. Clock generator with dual-non-overlapping clocks for the FIFO pointer registers.
15. Pointer register cell for addressing the FIFO (the read and write pointers). This register has to be modified to encode and output the addresses with the data, as well as to reduce the FIFO from 8 events to 4 events.
16. Dual-ported FIFO memory cell.