SCIPP 98/34
August, 1998

Power consumption of the GLAST Tracker Front-End Readout Chip, GTFE64

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Draft: August 28, 1998

1 Introduction

The power consumption of the GLAST Tracker front-end readout chip GTFE64 was measured. Two chips were mounted on a hybrid and operated at the nominal voltages.

- 2V and 5V for the analog section
- 3V for the digital section.
- LVDS signals: 1.1 V -> 1.43 V

The front-end chip has six differential input receivers, which were all connected. The data and fastOr drivers and receivers were connected as shown in Table 1.

Table 1: Data and FastOr connections.

Data left input	DLI	Floating
Data left output	DLO	Floating
Data right input	DRI	Floating
Data right output	DRO	Connect to LCDS -> CMOS driver
FastOr left input	TLI	FastOr right output
FastOr left output	TLO	Floating
FastOr right input	TRI	Biased by external voltage source
FastOr right output	TRO	FastOr left input

Some of the static power measurements were obtained using a single chip mounted in a carrier.

2 Analog power

The analog power was measured in a quiescence state. All masks were disabled and the threshold dac was set to 20 counts (~ 116 mV).

Table 2: Analog power consumption

	Analog 2V	Analog 5V
Current I [mA]	1.4	1.435
Power P [mW]	2.8	7.18
Power per channel P_{chan} [μW]	44.	112.

The total power for the analog section is 156 μW per channel.

3 Digital power

3.1 Static power of the input receivers

The differential input receiver i.e., clock, command and trigger acknowledge, are operated with LVDS signal levels. There are three states of the receivers.

1. The receiver is switched of if both input lines are at zero voltage.
2. The low state (p-line at 1.1 V, n-line at 1.43 V)
3. The high state (p-line at 1.43 V, n-line at 1.1 V)

The following table shows the change in current, if all of the receivers are switch from one state to another state. One of the trigger acknowledge receivers is always switched off, therefore only five out of the six receivers contribute.

Table 3: (results from single chip).

Receiver state change	I [μA]	I [μA] per receiver
Off state ⟶ low state	215	43
Low state ⟶ high state	220	44

The change in static power if an individual receiver is switched from the low to the high state is shown in the next table. The chip controller direction is set to the right, therefore the left trigger acknowledge is switched of.

Table 4: Static Power for the input receivers

Input line	Current I [μA]	Power P [μW]
Clk left	39.0	117.0
Clk right	43.0	129.0
Cmd left	40.0	120.0
Cmd right	42.0	126.0
Tack left	0.0	0.0
Tack right	37.0	111.0

3.2 FastOr drivers / receivers

The following figure shows the connections of the fastOr inputs and outputs.

The right fastOr output was connected to the left input, providing the correct termination. The right fastOr driver is switched on only if the controller direction is set to the right side, otherwise it is off and the left fastOr driver is switched on.

Controller direction	TROP [V]	TRON [V]
Right	1.35	1.67
Left	0	0

The right fastOr input is biased to the logical 0 state by an external voltage source:

TRIP : 1.0 V I ~ 26 [μA]
TPIN : 1.7 V I ~ 26 [μA]

In this configuration the quiescence power depends on the controller direction, as discussed in the next section.

3.3 Quiescence Power

The quiescence power of the chip depends on the state of the input receivers, the data and fastOr receivers and drivers. In order to measure the quiescence power the termination of the fastOr and data lines has to be taken into account. The following table shows the termination of the input and output lines.

The quiescence power has been measured for both readout directions.

Readout direction	Power for two chips
Right	2.550 mW
Left	2.424 mW

The increase in power in he right direction is due to the termination of the fastOr output.

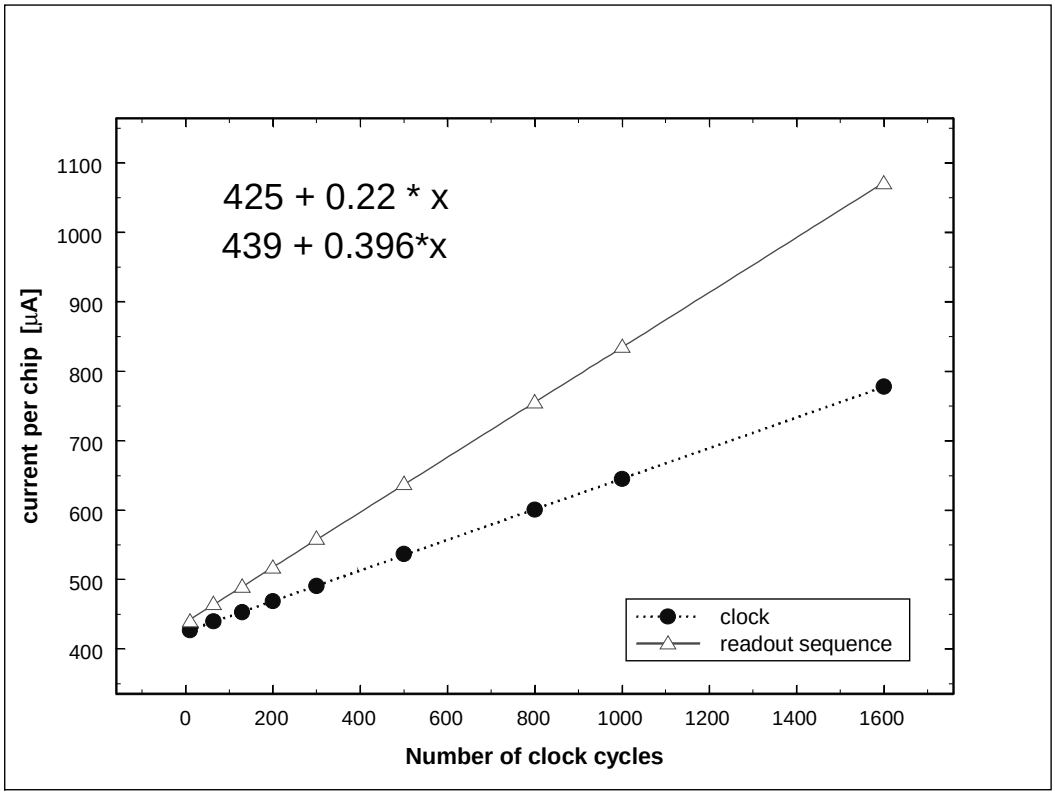
The quiescence power was measured to 19.9 μW per channel (1.27 mW per chip). All input receivers (clock, command and trigger acknowledge) are in the low state.

3.4 Power during digital activity

Two experiments were performed to measure the dynamic power consumption.

1. The chip was clocked for a certain number of clock cycles, but there was no activity on the command line or the trigger acknowledge line.
2. A readout sequence was issued. It consisted of a *read event* command followed by n-clock cycles and an *end read* command. The fifo of each chip had two hits, one in channel 20 the other in channel 40. Therefore data were shifted out of the register.

The rate was fixed to 12.5 kHz. The current values are the measured current divided by two. The quiescence power was 423 μA (1.27 mW).



The same experiment were also performed at dvdd = 5V. In Table 5 the slopes are compared. The expected current ratio is 5/3 = 1.67.

Table 5: comparing dynamic power consumption at dvdd = 2V and dvdd = 5V

	Slope, dvdd = 3V	Slope Dvdd = 5V	Ratio
Clock sequence	0.22	0.37	1.68
Readout seq.	0.396	0.64	1.61