Heavy-ion beam test for newly developed 0.5 μm processed chip.

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1 Introduction

Instruments on-board GLAST should work properly under severe radiation environments. The radiation effects are grossly divided into two types; one is the radiation damage and the other is a single-event effect, such as a single-event upset (SEU) and a single-event latch-up (SEL [1] [2] [3]). On July 29th, we performed a heavy-ion beam test at NIRS (National Institute of Radiological Science) in Japan. We first examined a SEL on the readout electronics, and them investigated a radiation damage on Si-strip sensors. Here, we make a report about the SEL test.

2 Experimental Setup

We used a Fe ion beam with kinetic-energy of 500 MeV/nucleus. A radiation-induced latch-up is caused by the large amount of charge-injection on the electronics, hence large LET (Linear Energy Transfer) is needed to test SEL property. The maximum LET that can be obtained by Fe ion is $\geq$ 20 MeV cm^2 mg^{-1} in Si, whereas 500 MeV/n Fe beam has LET of only $\sim$1.5 MeV cm^2 mg^{-1}. Hence, we placed acryl absorbers in front of the chip (see Figure 1) to decrease the beam energy, or to increase the LET. Hereafter, we express the depth of the acryl absorber in terms of water equivalent length. The depth can be adjusted with $\sim$ 0.6 mm step automatically, and with $\sim$ 0.03 mm step manually. The beam intensity before the absorber was monitored by an operator of the accelerator, and that after the absorber was monitored by ourselves using the plastic scintillator with PMT (Hamamatsu R1635) placed near the chip (Figure 1). In advance of the irradiation, we measured the dose profile by an ion-chamber placed at the position of the chip.

Chips to be irradiated were newly-developed 0.5 μm processed ones ([4]), mounted on the test board that was equipped with by-pass capacitances. There are 6 channels in one chip, although the final version should contain 64 channels. The test chip needs three power-lines to be operated; two for analog circuit (3.3 V for AVDD and 1.5 V for AVDD2) and one for digital circuit (3.3 V for DVDD). Reference voltage ($V_{\rm ref}$) and threshold voltage for the comparator ($V_{\rm th}$) are also should be provided.

During irradiation, the chip was powered through series resistors (protection circuit). If the supplied current increases, the voltage drop at the resistors also increases. Therefore, they will limit the current and prevent the burning of the chip even if latch-up occurs (otherwise extremely large current will be induced and the chip will be burned out). We also lowered the value of capacitance of by-pass condensers, since large amount of charge stored in caps could also be a current source in case of latch-up. We adjusted the values of resistance of series resistor so that all of the supplied voltages at the power supply become same (4.6 V). As shown in Figure 2a, AVDD and AVDD2 were bundled into "analog-part", and DVDD, $V_{\rm ref}$ and $V_{\rm th}$ into "digital-part". We set the value of $V_{\rm ref}$ at $\sim$ 250 mA and $V_{\rm th}$ $\sim$ 1.3 V. Through protection circuit, each part was powered by Keithley 617 electrometer controlled by a computer through GPIB interface. As shown in Figure 2a, the protection circuit also worked as a voltage divider

for AVDD2 (analog part) and $V_{\rm ref}$ and $V_{\rm th}$ (digital part). The typical loaded current of the analog part was ~ 750 μA, whereas that of the digital part is ~ 85 μA; almost all of the current for the digital part was consumed at the voltage divider that supplied $V_{\rm ref}$ and $V_{\rm th}$. In case of latch-up, the loaded current will not increase infinitely, but ΔI is limited ~ 100 μA by the series resistor. We hence set the threshold for the current increase as $\Delta I \leq 50$ μA. If ΔI exceeds this threshold, the power supply will be turned off automatically to recover the chip into normal state. We measured and recorded the supplied current every 1 second during irradiation, in order to monitor the latch-up.

We also irradiated a chip that was equipped with nominal capacitances and powered directly by the power supply (Figure 2b), in order to investigate the SEL property in normal conditions. This time we used three power supply for AVDD (3.3 V), AVDD2 (1.5 V), and digital part (3.3 V), and monitored the current for the latter two. The supplied current for AVDD2 is typically ~ 150 μA, whereas that of the digital part is ~ 400 μA. For the latter, almost all the loaded current is consumed at the voltage divider that made $V_{\rm ref}$ and $V_{\rm th}$.

The size of the digital area of the chip, which might be the weakest part to SEL, is ~ 0.115 mm^2. Since the size of the plastic scintillator is 20 mm $\times$ 20 mm, $\sim$1/3300 of the beam counted by PMT is irradiated to the digital area.

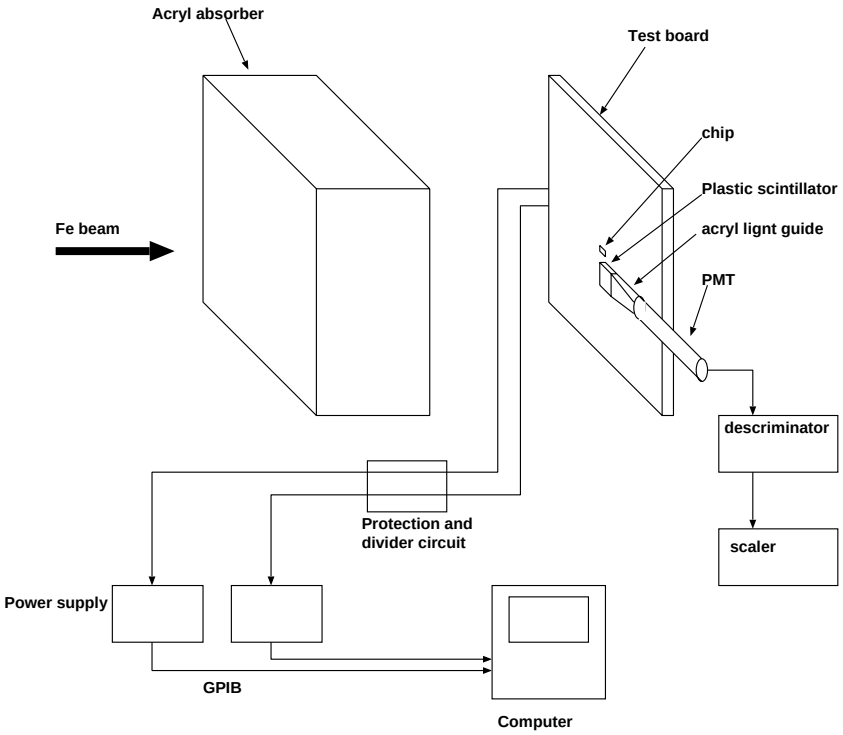

Figure 1: Schematic view of the SEL test setup

3 Test and Result

In advance to the chip irradiation, we had measured the dose profile in order to determine the appropriate depth of the absorber. We had measured the integrated amount of charge generated in the ion-chamber by the beam irradiation. Dividing it by the beam flux before the absorber, we can obtain the relative dose profile as a function of the the absorber depth (hereafter d). The obtained profile is shown in Figure 3. The dose reaches maximum at $d \sim 73$ mm, then drops

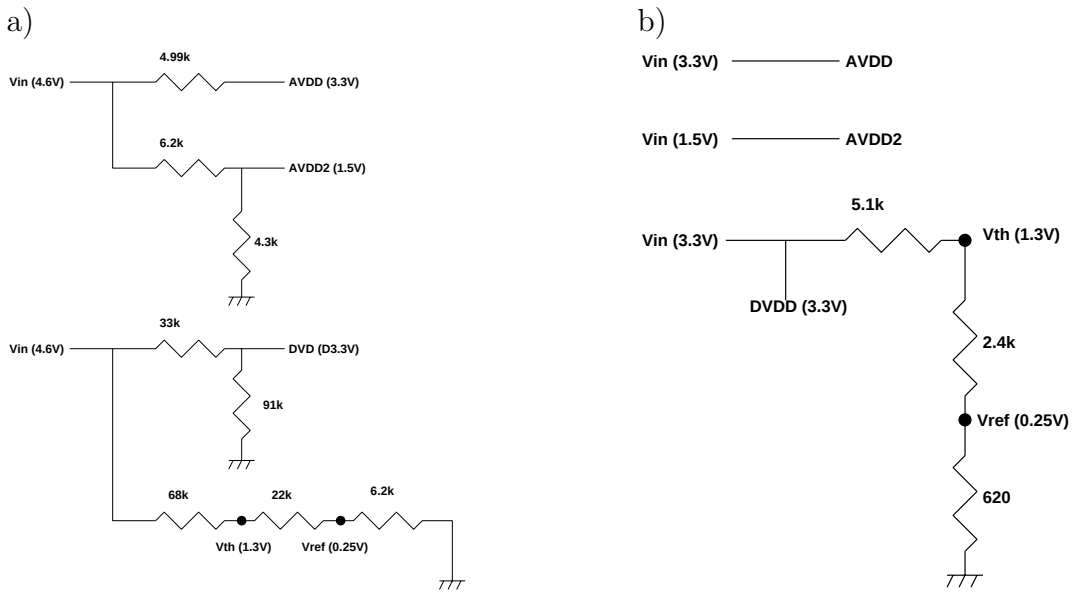

Figure 2: Drawings of power lines. Panel (a) indicates the power lines for the test with protection circuit, and (b) for the test under normal condition.

sharply within $\sim$ 1 mm; this would corresponds to the range struggling generated in the thick absorber. We adjusted d near the dose peak, where the most energetic Fe ion has $\sim$ 1.0 mm range in water (corresponds to the LET of $\sim$ 8 MeV cm^2 mg^{-1} in Si), and the weakest one would stop at the end of the absorber. Thus, the LET of the Fe ion would distribute from $\sim$ 8 MeV cm^2 mg^{-1} to $\sim$ 20 MeV cm^2 mg^{-1}, although we did not have any information about the energy (LET) distribution.

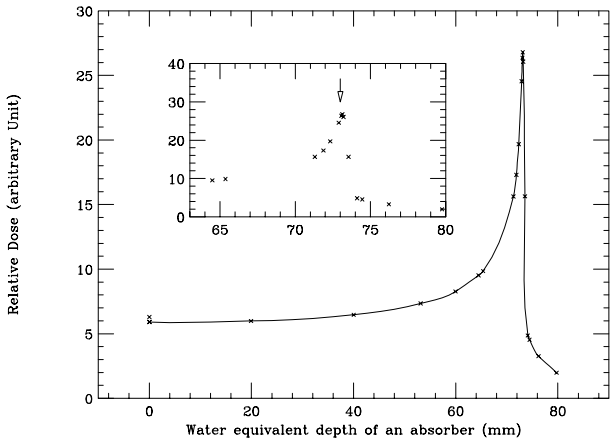

Figure 3: Obtained dose profile. The small panel shows the detailed profile near the dose peak. By an arrow, we indicate where we adjusted the depth of the absorber.

We first utilized the board with the protection circuit (Figure 2a), and radiated the beam for about an hour. The rate of the beam counted by PMT is $\sim 10^5$ c s^{-1}, thus that irradiated to the digital area is $\sim$ 30 c s^{-1}. Total number of the beam irradiated to the digital area is hence $\sim 10^5$. We had monitored the current of both the analog and digital part, and no indication of

the latch-up (increase of the current beyond the threshold) were observed. We also utilized the board without the protection circuit (Figure 2b), and, again, did not observe the latch-up.

All the obtained time profile of the current are shown in Figure 4. There, the digital part showed gradual decrease of current ($\sim$0.4%/hour), whereas the current of the analog part weakly increased by $\leq$0.1%/hour. We have not obtained the full explanation of this phenomena, but they are at least partly due to the stability of the electrometer. When we powered a resistor by the electrometer and monitored the current in a laboratory where the room temperature is controlled within $\pm 1^{\circ}$C, we found that the electrometer that had been used for the analog part showed weak current increase ($\leq$ 0.1%/h), whereas that for the digital part exhibited gradual current decrease ($\sim$0.8%/h).

We can see another, noticeable property in the current profile. The digital part showed small current increases ($\Delta\ I \sim 0.5\ \mu$A), especially when operated with the protection circuit. whereas others rarely exhibited such phenomena. We thus examined the current profile in detail, and showed the expanded one in Figure 5. Thus, current increased abruptly, then dropped to nominal value within a few seconds. We suspect this is because with the series resistor, it took some amount of time to charge-up the by-pass (or, internal) capacitance from which some amount of charge had been derived when comparator is fired. Anyway, the degree of current increase is much smaller than the threshold for the latch-up ($\Delta I = 40\ \mu$A, see § 2).

After the irradiation, we performed a functional test on the chip. We inputted the test pulse, and looked at preamp out, shaper out, and comparator out of all the channels. Then, all looked fine except for one channel of the chip irradiated without the protection. There, we could not see any shaper output signal on the pad, although its comparator output turned on and off depending on the threshold level. Since the comparator output was still working, the channel is still functional, we guess. We also checked out the power lines after the chip irradiation, by measuring the current of AVDD+DVDD (3.3 V) and AVDD2 (1.5 V). All the current took nominal values, hence seemed to be normal.

According to the calculation of a member of NIRS, 2/3 of the incident Fe would suffer nuclear interaction, since the depth of our absorber is somewhat large (equivalent to 74 mm water). Therefore, we say that we did not observe the indication of latch-up for the irradiation of $\geq 3 \times 10^4$ Fe ion having LET of 8–20 MeV cm^2 mg^{-1}.

4 Discussion

We estimate the number of ion that will be irradiated to the chip in-orbit. According to NASA's IRD (Interface Requirement Document), number of incident heavy ions having LET of $\geq$ 8 MeV cm^2 mg^{-1} in the worst case (Solar event worst day) is $\geq 3 \times 10^{-3}$ cm^{-2} day^{-1}. Hence, number of heavy charged particles expected to the digital area of our chip (whose size is 0.115 mm^2) is 0.012 for ten years. Even if we sum up all the chips (24/layer $\times$ 18 layer $\times$ 2(xy) $\times$ 16 towers = 13824), and assume that all the active area of GTFE (11.4 $\times$ 2.0 mm) is sensitive to SEL equally with the digital part, 3×10^4 ions correspond to 10 years irradiation in-orbit. Thus our chip showed no indication of latch-up for LET of $\leq$ 8 MeV cm^{-2} mg^{-1}, after irradiating the sufficient amount of particles expected in-orbit,

Although our tested chip thus exhibited a fair immunity to SEL as described above, we still cannot guarantee that readout chips on-board GLAST will be free from SEL. First, we had monitored the current not continuously, but every 1 second. Thus, there might exist the possibility that we missed a small-scale latch-up; if the electronics was burned out immediately after the latch-up and recovered to the normal state quickly (all processes occurred within 1 second), we could not detect the latch-up. However, a latch-up of this type may not have occurred during our test, since our chips look to be functional after the irradiation. There is another probability that we might miss the indication of latch-up. When the consumed

current reaches the current limit of the electrometer ($\leq$ 4 mA) during the irradiation without protection, the electrometer will lower the supplied voltage and hence the latch-up will be solved. If this process occurred quickly (all within 1 second), we also would miss such phenomena. Furthermore, chips utilized in this test are of test version containing only 6 channels in one chip. Readout chips on board GLAST must have increased number of active transistors. Then, a interelement separation will become smaller, hence the chip will be more sensitive to SEL. Therefore, further experiments irradiating heavier ions on the chip essentially the same with that on board GLAST is necessary.

References

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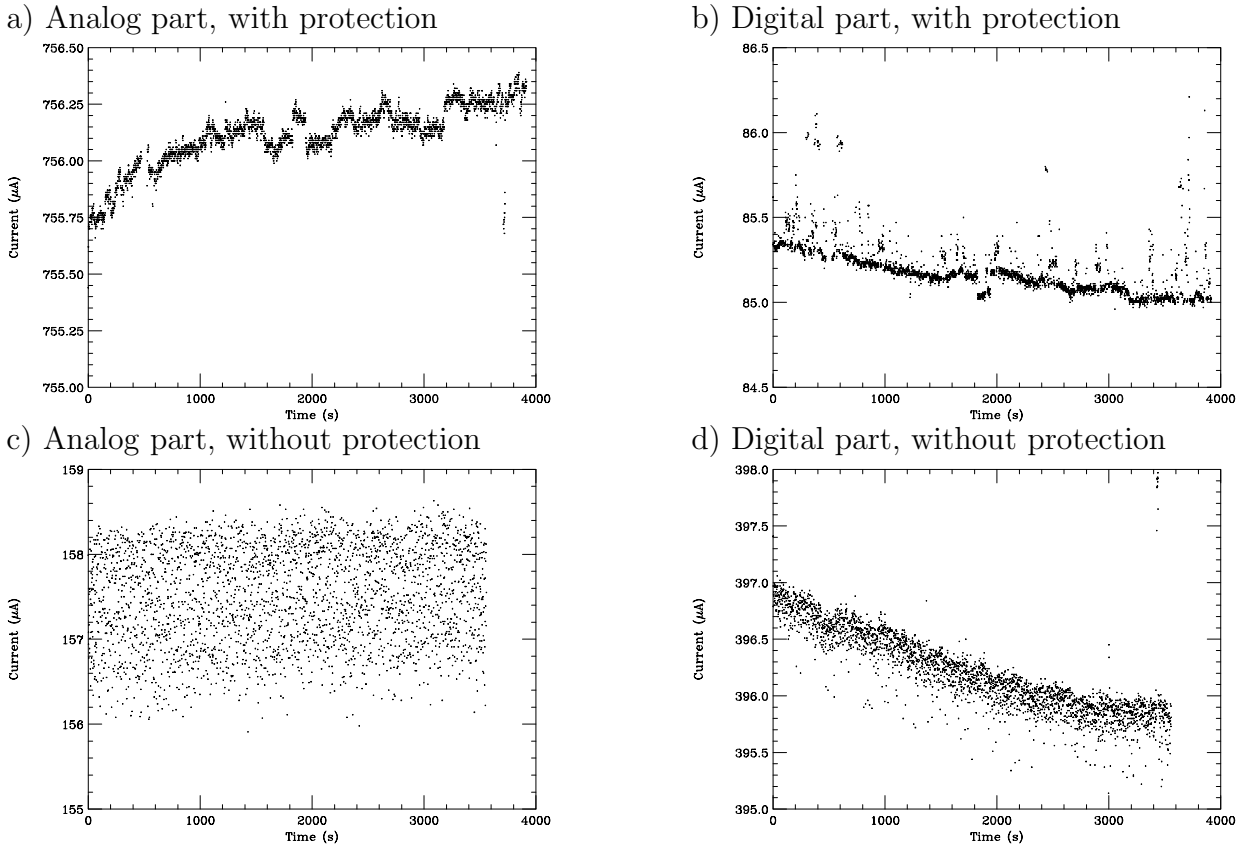

Figure 4: Monitored time profile of the loaded current.

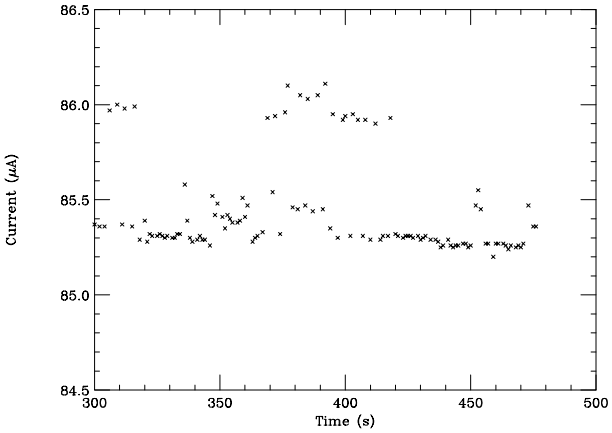

Figure 5: Expansion of the time profile of loaded current for digital part with protection circuit.