SCIPP 98/06
March 5, 1998

Irradiation Test of a GLAST Front-end Electronics GTFE32 Chip

M. Hirayama
Research Center for the Early Universe
University of Tokyo

and

W. Kröger, W. Rowe, R. Johnson, and H.F.-W Sadrozinski
Santa Cruz Institute for Particle Physics
University of California, Santa Cruz

Abstract

A 2nd generation prototype of the GLAST readout electronics GTFE32 was irradiated up to 50 krad to investigate radiation hardness of the chip. At the UC Santa Cruz ^{60}Co facility the chip was irradiated to 20 krad on Feb. 20, 1998 and 30 krad on Feb. 21, 1998. As a result of 50 krad irradiation in total, the chip stopped functioning. Based on simple tests of the chip taken place before and after these irradiations, we found that irradiation did damage mostly to a comparator stage, and almost none to the shaping amplifier and digital readout section.

1 Introduction

A converter/tracker for the GLAST satellite will consist of silicon microstrip detectors with front-end readout electronics. Although those could be exposed to radiation in orbit up to 10 krad over the life of GLAST, the prototype readout electronics has been proven to be durable by irradiation test of a GTFE16 chip (see SCIPP 98/05). A 2nd generation GLAST readout electronics GTFE32 was irradiated by up to 50 krad at the UC Santa Cruz ^{60}Co facility to investigate durability of our readout electronics against radiation. In this report, results from the irradiation test of a GTFE32 chip are presented.

A front-end readout electronics "GTFE32" (Glast Tracker Front-end Electronics 32 channel version) was designed as a 2nd generation prototype of the GLAST front-end electronics. Its design is almost identical to that of the GTFE16 chip, a first generation prototype, except that the GTFE32 chip has 32 channels of readout instead of 16. Each channel consists of charge sensitive preamplifier and a shaping amplifier, which acts as a CR-RC filter, followed by a comparator to discriminate signals. One readout chip was used throughout all the measurements in this report.

2 Setup and Pre-irradiation measurements

A GTFE32 chip was mounted on a printed circuit board for the irradiation test. The PC board is connected to a data acquisition system built on VME which was used for the GLAST beam test at SLAC. The data acquisition system supplies all power needed, register settings, and passes calibration signals from a LeCroy 9210 pulse generator.

A printed circuit on the board is quite simple; it basically consists of filters for power supplies, capacitive loads for input of a chip, and differential receiver/driver. Eight capacitors were placed on the PC board as a capacitive load for the chip inputs. However, only one of those (33 pF) was used for measurements in this report. The PC board carries differential receiver and driver chips to interface between differential inputs/outputs on the chip and TTL signals from/to the data acquisition system.

The methods of measurement of readout noise, gain numbers, and comparator offsets are similar to those for the irradiation test of GTFE16 (SCIPP 98/05) except for scanning threshold voltages instead amount of charges injected (threshold scan). We chose charge injection of 0.75, 1.125, 1.5, 1.875, and 2.25 fC to measure the gain number and comparator offset. For better noise measurements, we ran threshold scans without charge injection to reduce noise pickup from a pulse generator to be used to inject charges.

Before irradiation, we investigated the fundamental functions of the chip. The pulse shape of preamplifier outputs and shaping amplifier outputs were fine for all channels with no capacitive load on input. However, once 33 pF of capacitive load was connected to ch26 of the chip, the chip picked up unexpected signals (and noise) on the channel. After investigations, we found that these came from the analogue ground bouncing by about 40 μV in RMS; even 40 μV bouncing of analogue ground could cause significant charge injection of up to $\sim$ 1 fC through a capacitive load of 33 pF. We improved the grounding on the PC board to reduce such extra charge injection (compare pulse shapes in figure 1). However, we concluded that the improvement was not enough to precisely measure noise and gain numbers of the chip, and that we should remove all capacitive loads from the inputs of the chip.

3 Irradiation of a GTFE32 chip

A GTFE32 chip was irradiated by 20 krad on Feb. 20, 1998 and 30 krad on Feb. 21, 1998 at the UC Santa Cruz ^{60}Co facility, so that functions of the chip were checked at total radiation level of 0 krad, 20 krad, and 50 krad. During the irradiation, the readout chip was powered in the same way as normal operation (5 V for AVDD and DVDD and 2 V for AVDD2). The differential receiver/driver chips on the board were removed from the board before each of the irradiations, and restored after each.

3.1 Readout noise, Gain number, and comparator offset

Results from threshold scans are summarized in figures 2, 3, and 4. Before irradiation (figures 2), all channels except for ch2[1] had gain numbers around $\sim$ 110 mV/fC and comparator offsets ranging from 0 to 20 mV as expected. The readout noise is higher than expected; an equivalent noise charge of approx. 200 electrons, which was measured for GTFE16, is expected, since the analogue design is almost identical to that for GTFE16[2]. This higher noise is probably due to noise pickup on the PC board which we used for this irradiation test. Also, one can notice non-uniformity over channels. It is unlikely that this is due to non-uniformity of the chip itself[3]. Instead, it is likely due to noisy environment of the GTFE32 chip on the PC board.

After 20 krad irradiation (figure 3), gain numbers were slightly reduced, while comparator offsets were still in a range between 0 and 20 mV. As we see below in § 3.3, smaller gain numbers are not due to actual reduction of amplifier gain, but due to some unknown change in the comparator functioning. Also, one can notice that gain number is significantly low every 4th channel. As seen below in § 3.3,

[1]The calibration input for ch2 was somehow dead.

[2]The gain and time constants were reduced on GTFE32 with respect to GTFE16.

[3]Although some non-uniformity was seen in the noise distribution when GTFE32 chips were used for the GLAST beam test in Oct. 1997, the noise distribution was symmetric across channels.

this was not seen in pulse height of shaping amplifier output, so that we conclude that this happens also in a comparator stage. The readout noise was still high at this time.

After 50 krad irradiation, the chip stopped functioning (figure 4); gain numbers measured by threshold scans went down to essentially zero, and comparator offsets remained in a range between 0 and 20 mV. On the other hand, the readout noise was reduced by a factor of three, down to the noise level which is consistent with results from noise measurements without charge injection (see below in figure 5 in § 3.2). This could happen if there is significant radiation damage to a comparator stage, so that pulses at the shaping amplifier output due to charge injection are completely discarded.

3.2 Readout noise measurement with no charge injected

Readout noise was also measured without charge injection through a calibration input. This was done to avoid noise pickup from the calibration input and to reduce noise from outside the chip. Results are plotted in figure 5 and no change by irradiation can be seen up to 50 krad. However, the readout noise is still much higher than the expected equivalent noise charge of approximately 200 electrons, and non-uniformity over channels remains. These are likely due to noisy environment of the GTFE32 chip on the PC board.

3.3 Pulse shape of shaping amplifier output

After 20 krad and 50 krad irradiation, the pulse shapes at the shaping amplifier outputs of ch27 and ch28 were probed with a pico-probe (figures 6 and 7). Although slight changes are seen in pulse shape and pulse height (decrease by a couple of percent), the CR-RC shaping filter is working even after 50 krad irradiation. Also, note that the difference in pulse height is only $\sim 1\%$ after 50 krad (figure 7). This means that no significant difference is seen in gain number between ch27 and ch28, whose gain numbers obtained by threshold scans are different from each other by about 10% (figure 4). We conclude that decrease of gain number by irradiation is not due to a decrease in the actual amplifier gain in the CR-RC filter circuit, but due to some unknown change in a comparator stage.

The threshold receiver response was also measured before and after 50 krad irradiation to the readout chip to confirm the conclusion, since gain numbers obtained by threshold scans also depend on the threshold receiver response. Figure 8 shows the threshold receiver response measured before the irradiation, and figure 8 shows that measured after the irradiation. In conclusion, no significant changes are seen in the threshold receiver.

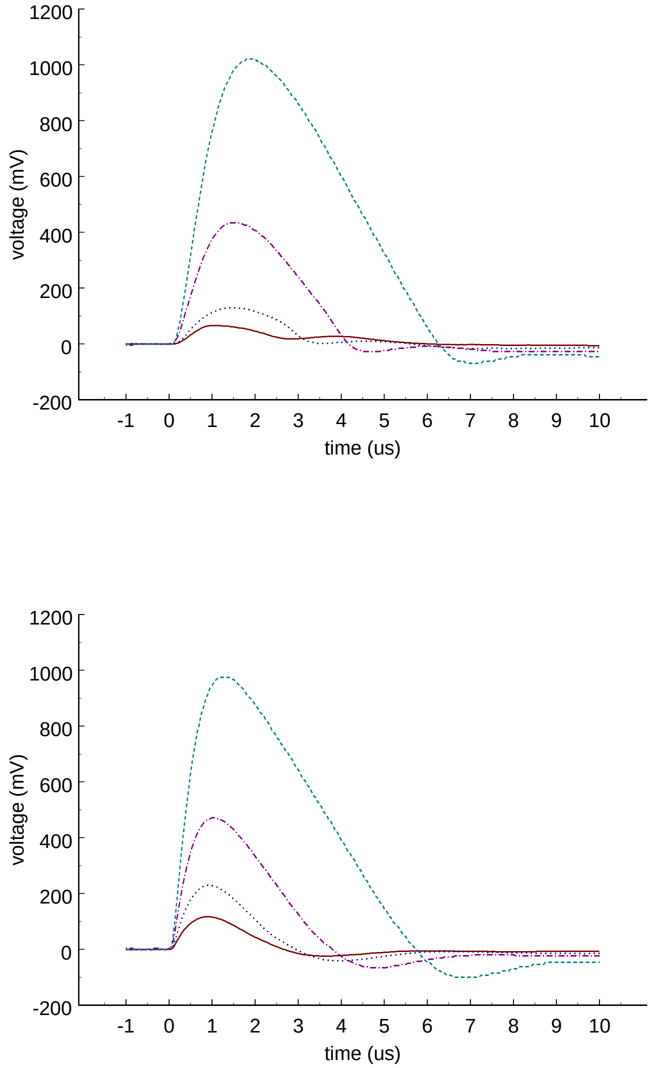

Fig. 1. Pulse shapes of shaping amplifier outputs on ch26 (upper panel), which is connected to pure capacitive load of 33 pF, and those on ch27 (lower), which has no capacitive load, before irradiation. Each curve corresponds to charge injection of 1 fC, 2 fC, 4 fC, and 8 fC, respectively.

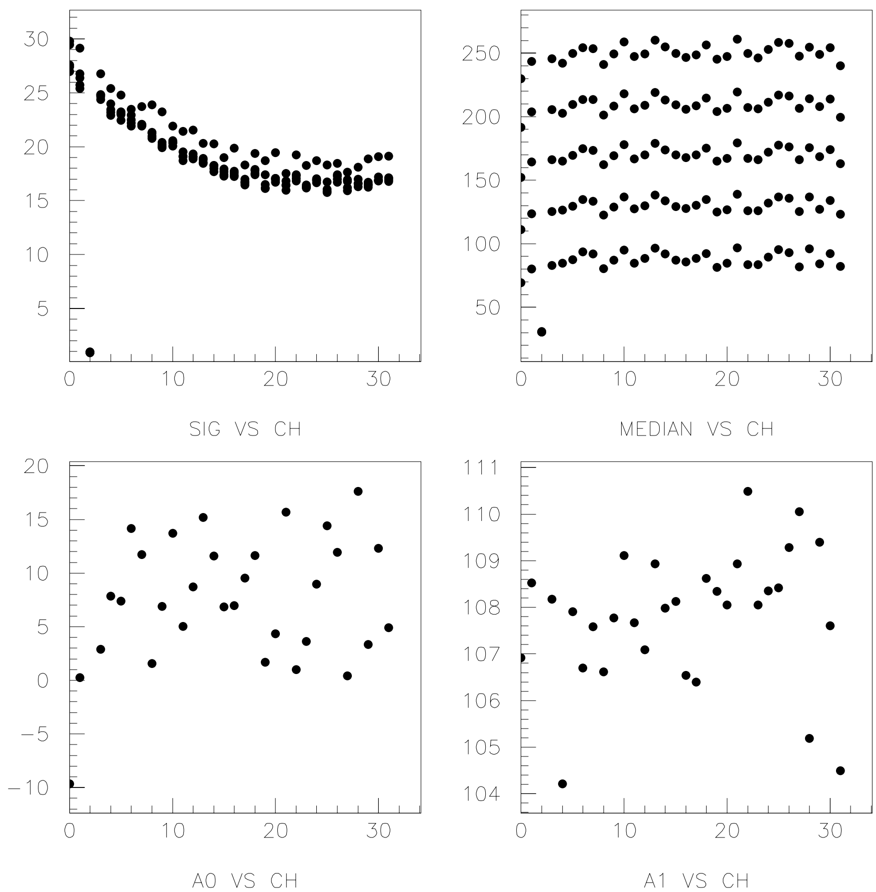

Fig. 2. Results from threshold scans with charge injection of 0.75, 1.125, 1.5, 1.875, and 2.25 fC. In the figure are plotted readout noise (mV) versus channel obtained from each scan in the upper left panel, threshold voltage corresponding to 50% occupancy (mV) versus channel in the upper right panel, gain number (mV/fC) versus channel in the lower right panel, and comparator offset (mV) versus channel in the lower left panel. Since the calibration input for ch2 was dead, the results for ch2 in the plots are meaningless.

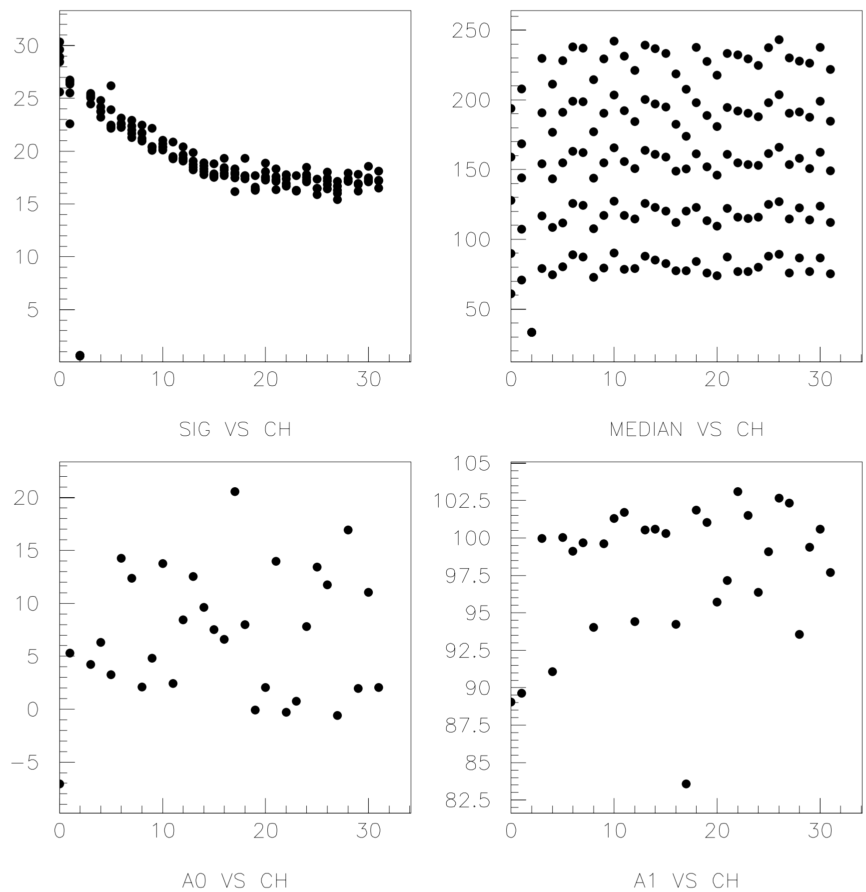

Fig. 3. The same plot as figure 2 but after 20 krad irradiation by the ^{60}Co source.

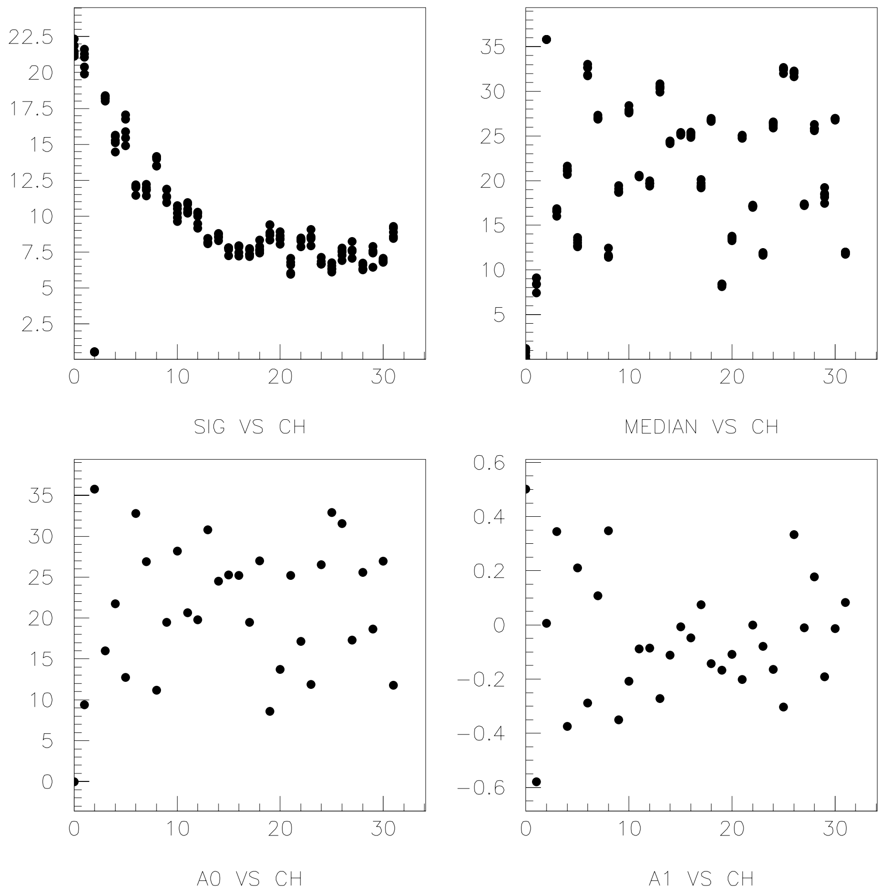

Fig. 4. The same plot as figure 2 but after 50 krad irradiation by the ^{60}Co source.

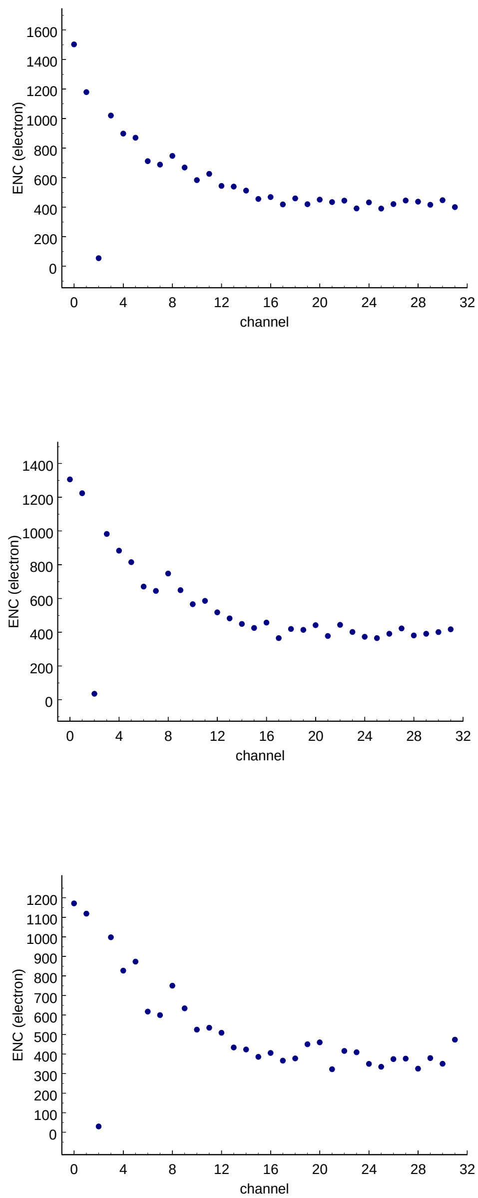

Fig. 5. Readout noise measured without charge injection versus channel number. A plot at the top shows readout noise measured before irradiation, at the middle shows that after 20 krad irradiation, at the bottom shows that after 50 krad irradiation on the chip. All results in the plots are identical and much higher than the expected value of ~ 200 electrons. Since the calibration input for ch2 was dead, the results for ch2 in the plots are meaningless.

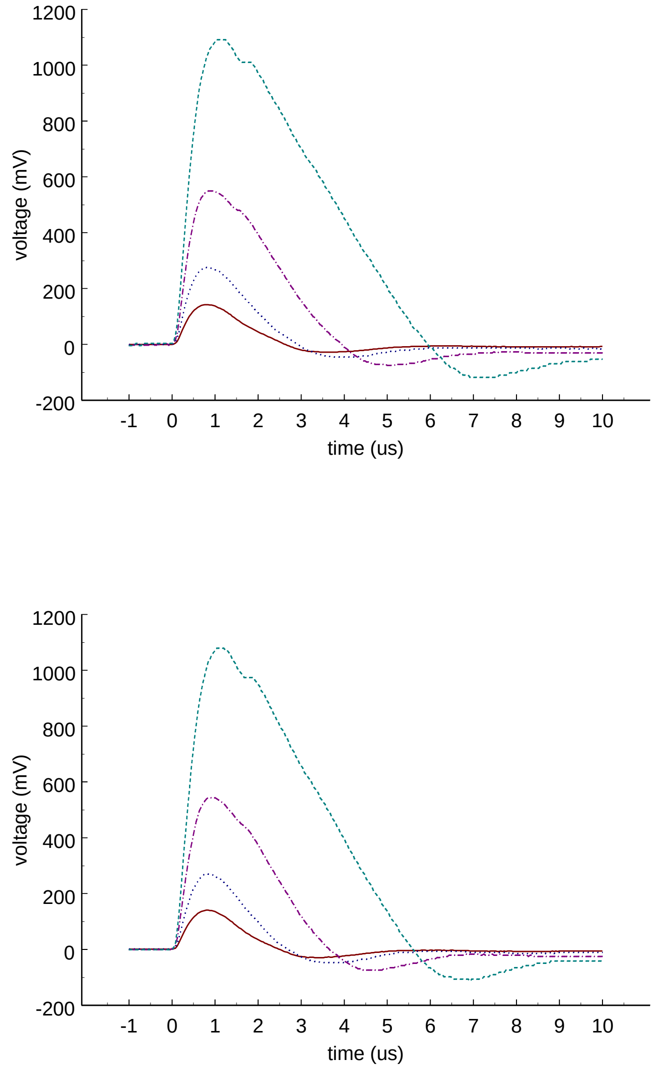

Fig. 6. Pulse shapes of shaping amplifier outputs on ch27 (top panel) and ch28 (bottom) after 20 krad irradiation by ^{60}Co source. Each curve corresponds to charge injection of 1 fC, 2 fC, 4 fC, and 8 fC, respectively.

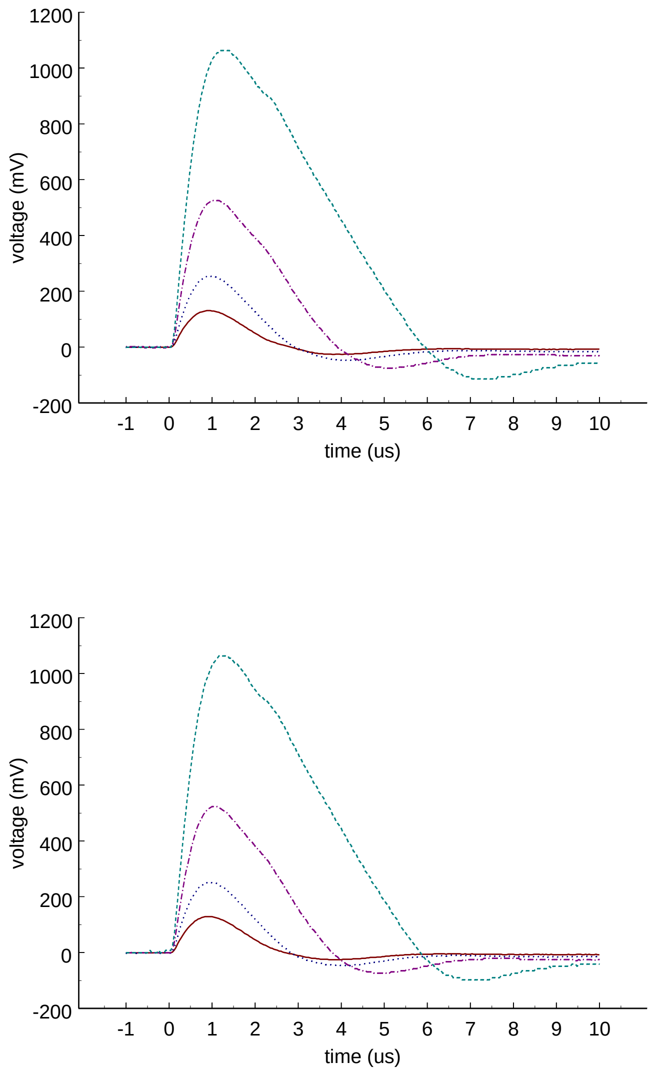

Fig. 7. The same plot as figure 6 but after 50 krad irradiation by ^{60}Co source.

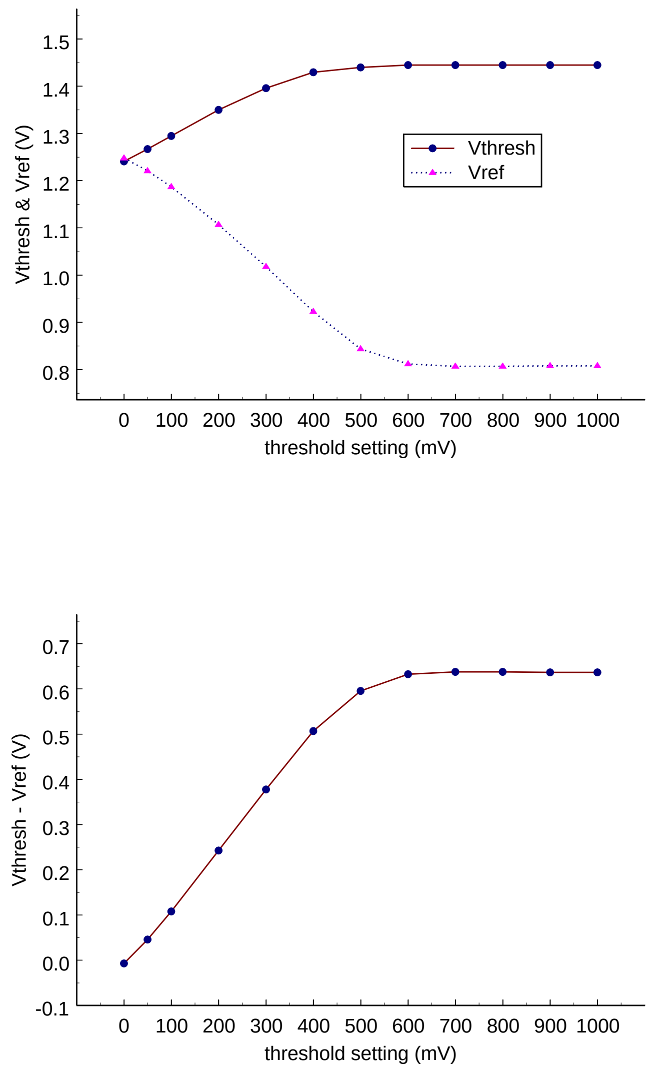

Fig. 8. Threshold receiver response before irradiation. Voltages on V_{thresh} (pad #9) and V_{ref} (pad #8) are separately plotted against threshold set by high voltage supplier Keithley 237 in upper panel. Lower panel shows $V_{\mathrm{thresh}} - V_{\mathrm{ref}}$ versus the threshold setting. A threshold receiver respond linearly up to 500 mV in setting and its amplification factor is 1.25.

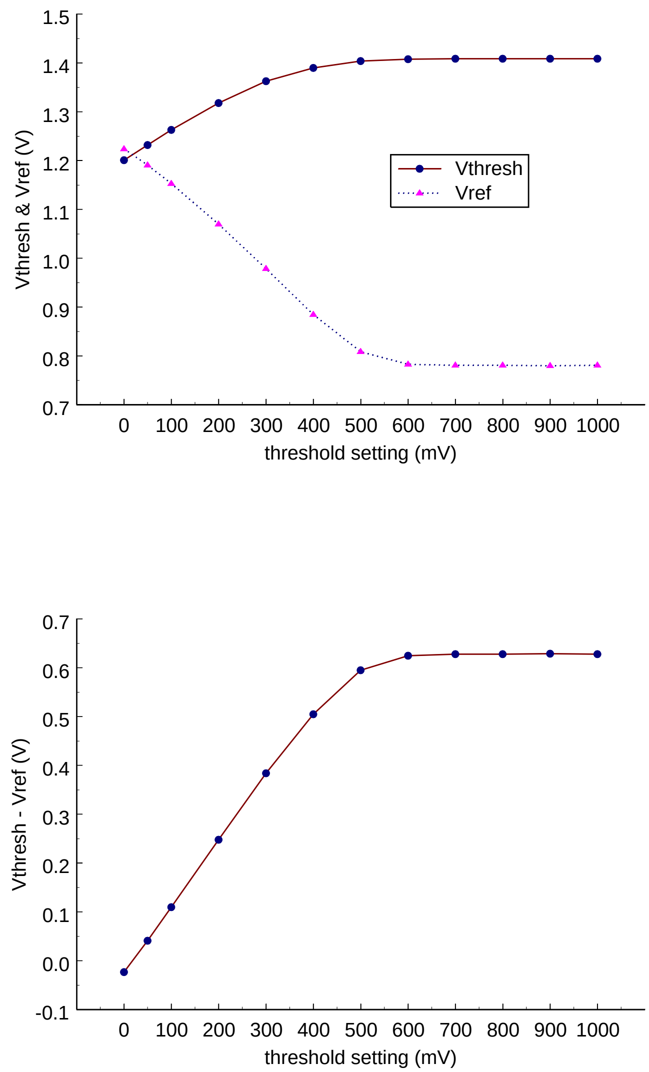

Fig. 9. Threshold receiver response after 50 krad irradiation by ^{60}Co source. See a caption for figure 8 for explanation of the plot.