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Document Title **Tracker Front End Readout ASIC Specification**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Conceptual Design and Specification of the GLAST Tracker Front-End Electronics (GTFE) ASIC

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CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
4	April 4, 2001	Initial release

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1 PURPOSE

This document documents the conceptual design and specifications for the GLAST Large Area Telescope (LAT) Tracker Front-end Electronics (GTFE) ASIC.

2 SCOPE

This document describes the architecture of the GLAST LAT Tracker Front-end Electronics (GTFE) ASIC. The electrical, logic, and mechanical interfaces to the ASIC also are specified.

3 DEFINITIONS

3.1 Acronyms

GLAST – Gamma-ray Large Area Space Telescope

GRB – Gamma-Ray Burst

LAT – Large Area Telescope

TBR – To Be Resolved

TKR – Tracker subsystem

TRG – L1 Trigger

GLB-TRG – Global L1 Trigger

ASIC – Application Specific Integrated Circuit chip.

TEM – Tower Electronics Module

MCM – Multi-Chip Module (in this context a Tracker front-end readout module)

GTFE – GLAST Tracker Front-End readout ASIC.

GTRC – GLAST Tracker Readout Controller ASIC.

3.2 Definitions

μsec, μs – Microsecond, 10^{-6} second

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations.

s, sec – seconds

4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the GTFE concept and its requirements include the following:

4.1 Requirements Documents

GLAST00010, “GLAST Science Requirements Document”, P.Michelson and N.Gehrels, eds., July 9, 1999.

LAT-SP-00010, “GLAST LAT Performance Specification”, August 2000

LAT-SS-00017, “LAT TKR Subsystem Specification – Level III Specification”, January 2001

LAT-SS-00152, “LAT TKR Subsystem Specification – Level IV Readout Electronics Specification”

4.2 Conceptual Design Documents

[1] LAT Electronics System – Conceptual Design

[2] LAT Tracker Electronics System

[3] LAT TKR-CAL Tower Electronics Module – Conceptual Design

[4] LAT Control Protocol within LAT – Conceptual Design

[5] LAT Data Protocol within LAT – Conceptual Design

[6] LAT Housekeeping within LAT – Conceptual Design

[7] LAT L1 Trigger System – Conceptual Design

[8] LAT-SS-00168, "Conceptual Design of the LAT Tracker Electronics Readout System."

[9] LAT-SS-00170, "Conceptual Design of the GLAST Tracker Readout Controller Electronics ASIC (GTRC)," September 30, 2000.

[10] LAT-SS-00171, "Specification of the LAT Tracker front-end readout Multi-Chip Module (TMCM)."

[11] LAT-SS-00175, "GLAST Tracker Flex Cable Specification," April 10, 2001.

[12] LAT-SS-00176, "Tracker Electrical Interface Specification," April 1, 2001.

4.3 Documentation of the Preceding Design Iteration (GLAST BTEM)

[13] V. Chen, et al., "The Readout Electronics for the GLAST Silicon-Strip Pair-Conversion Tracker," SLAC PUB 8549 (August 2000).

[14] Interface Description for the GLAST Tracker Front-End Readout Chip, GTFE64, SCIPP 98/25, September, 1998.

[15] Interface Description for the GLAST Tracker Readout Controller Chip, GTRC, SCIPP 98/26, September, 1998.

[16] R.P. Johnson, "An Amplifier-Discriminator Chip for the GLAST Silicon-Strip Tracker," IEEE Trans. Nucl. Sci. **45**, 927 (1998).

5 INTRODUCTION

The GLAST electronics system is described in [1]. The Tracker sub-system electronics are documented in [2]. One of the two custom ASICs required is the Glast Tracker Front-End Electronics (GTFE) ASIC. Refer to Figure 1 for a block diagram of the ASIC. The functions of the GTFE include charge-sensitive preamplifier, shaping amplifier, discriminator, channel mask registers for trigger and data, trigger generation, channel-hit data readout, calibration, and event buffering. The key challenges for the ASIC are low noise, low power, and discriminators with small offset variations. The GTFE is manufactured using the 0.5 μm Agilent CMOS process. The GTFE described in this document serves 64 adjacent silicon strips from the GLAST 228 μm pitch sensors.

The ASIC design described in this document is based upon the design of the front-end readout ASIC used in the GLAST BTEM prototype Tracker module, which is described in 4.3.

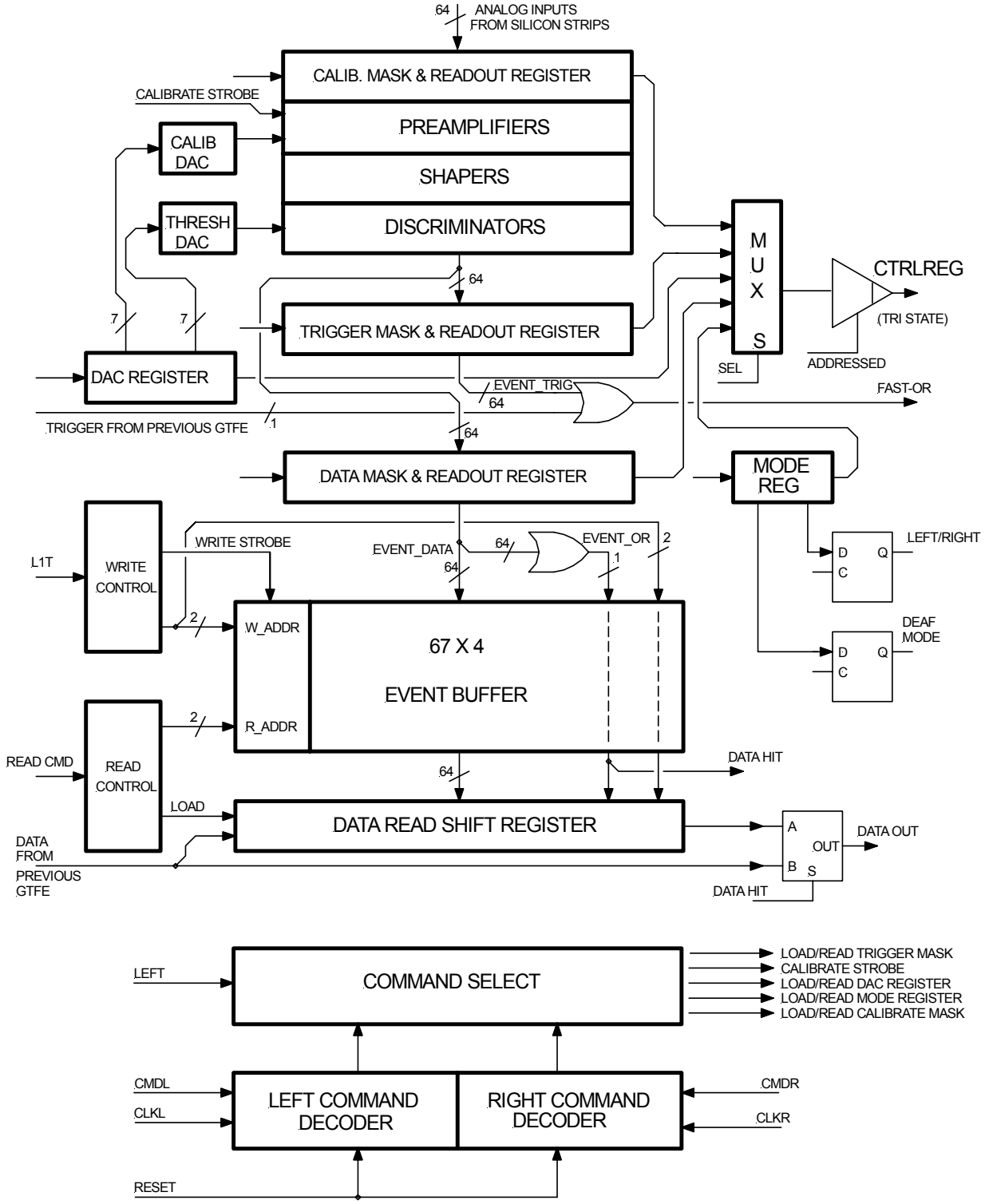

Figure 1. GTFE top-level block diagram.

6 GTFE Description

6.1 Overview

Refer to Figure 1. The ASIC amplifies signals from 64 silicon strips. The signals from each strip are converted into voltages by charge-sensitive preamplifiers. The output signal of each preamplifier is filtered with a simple $(RC)^2$-CR shaper with a peaking time of about 1.5-μsec. Each shaper output signal is converted to a digital signal with a discriminator, which is AC coupled to the shaper output. The threshold of all 64 discriminators is controlled by a seven-bit THRESH DAC that is normally set to about 4 to 5 σ about the RMS noise floor. This DAC output is controlled by the contents of the DAC REGISTER, which holds 7 bits for the THRESH DAC setting plus 7 bits for the CALIB DAC setting (see below).

The outputs of the discriminators are used for two purposes:

[1] Each channel discriminator is AND'ed with one bit of the TRIGGER MASK REGISTER to form EVENT_TRIG, then OR'ed with all other channels as well as the FAST-OR of the preceding GTFE chip. This signal is forwarded to the next GTFE and is in turn OR'ed with its channel hits. This process continues across 24 GTFEs to form a Tracker Tower Layer FAST-OR.

[2] Each channel discriminator is AND'ed with one bit of the DATA MASK REGISTER to form EVENT_DATA. This signal, one for each channel, is then stored in the four-deep EVENT BUFFER whenever the trigger, L1T, is received. The buffer write address, W_ADDR, is provided as two additional bits on the serial L1T line. W_ADDR is also written with the event into the buffer as a mechanism for identifying the event later for diagnostic purposes. In addition, all 64 EVENT_DATA signals are OR'ed together into one signal, and this HIT BIT is written into the EVENT BUFFER as well. This bit is used during readout to check whether any channels have been hit. Note that the EVENT_DATA signal is not held unless L1T is received. Hence the L1T must be received before the shaper output falls below the discriminator threshold.

When a READ_CMD is received event data are retrieved from the EVENT BUFFER and stored in a temporary holding register for shifting out serially. The READ CONTROL block transmits through the DATA READ SHIFT REGISTER the two-bit W_ADDR first, which was written into the memory along with the data, followed by the HIT BIT. The READ CONTROL block uses the HIT BIT to see if any channels have been hit. It transmits all 64 channel bits if the hit bit is true; otherwise data from the previous GTFE are forwarded. This provides some data sparsification. There are actually two DATA READ SHIFT REGISTERS. One is used to read out to the left and the other is used to read out to the right. Redundant DATA READ SHIFT REGISTERS and two independent COMMAND DECODERS provide fault tolerance at the GTFE level.

The GTFE has two COMMAND DECODERs, LEFT & RIGHT, as mentioned previously. Each is controlled from an independent Readout Controller, GTRC. Both the LEFT and RIGHT COMMAND DECODERs are allowed to load the MODE register at any time, regardless of which COMMAND DECODER has been selected to be active via the LEFT bit. The inactive COMMAND DECODER ignores all other commands. Note that the readout system is required never to attempt to load the MODE REG simultaneously via the LEFT and RIGHT COMMAND DECODERs. The DEAF bit in the MODE REG is used to disable reception of the EVENT_TRIG and EVENT_DATA signals from the adjacent GTFE chips.

Each analog channel can be independently calibrated. The active COMMAND DECODER can generate a CALIBRATE STROBE, which is a step function lasting 512 clock cycles. One seven-bit DAC is used to set the signal level according to the bits stored in the DAC REGISTER. The CALIBRATION MASK REGISTER is loaded to select any subset of channels to receive the injected signal. Each channel has a 46 fF capacitor to translate the voltage step into an injected charge.

All configuration registers are read back non-destructively and are Single Event Upset, (SEU), hard registers. The CALIBRATE, TRIGGER, & DATA MASK registers are 68 bit long. The MODE REG is two bits long, and the DAC REGISTER is 14 bits long.

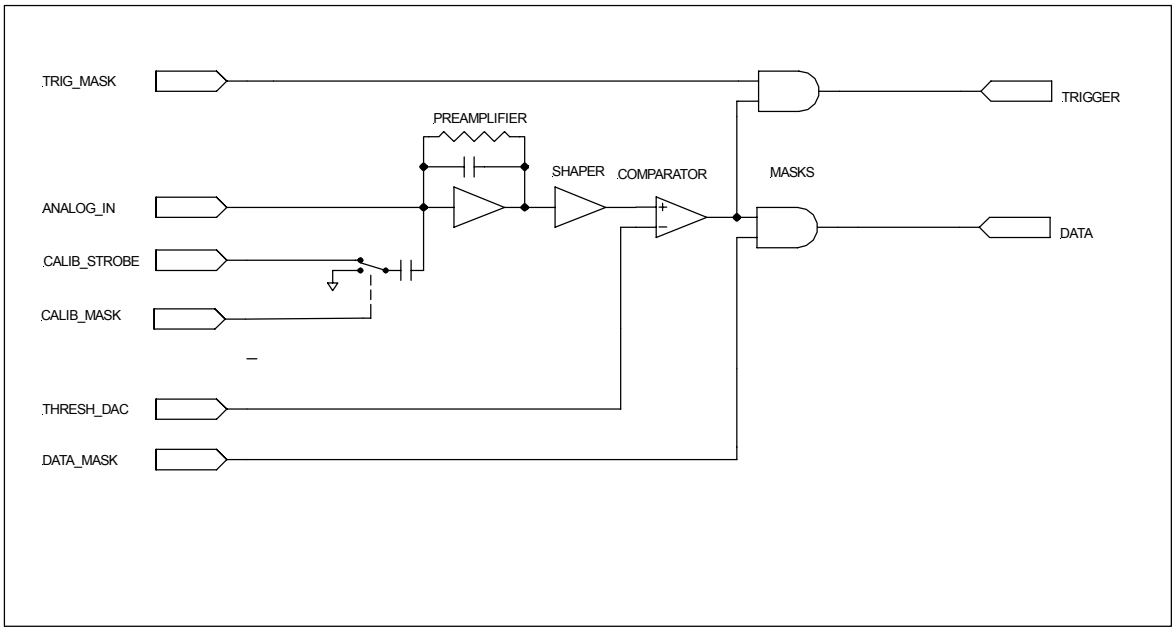

Figure 2: Single Channel Block Diagram

6.2 Charge Amplifier

Figure includes a simplified view of the charge-amplifier. The gain is determined by the 0.13 pF feedback capacitor, which provides about 37 mV per MIP. The feedback resistor is implemented using a transistor with the gate connected to a dc-reference voltage. An additional current is switched in, (not shown in the figure), when the discriminator is above threshold. This current is used to achieve faster discharge of the feedback capacitors in saturation conditions. The preamplifier is AC coupled to the following shaping amplifier, and the shaper is AC coupled to the comparator, to minimize offset voltage errors. Each channel has a 46 fF calibration capacitor for injection of charge. The calibration pulse level is controlled by a seven-bit DAC, CALIB_DAC, and each channel has a mask bit to control whether it sees the calibration pulse.

6.3 Shaping Amplifier

The peaking-time of the shaping amplifier, SHAPER, is set via capacitors and transistors used as resistors. The shaping is single pole RC-CR with a peaking time of about 1.5 μsec. The shaping amplifier is AC coupled to the following comparator. The signal amplitude out of the shaper is about 70 mV per fC at 1 fC input charge.

6.4 Discriminator

The shaper output is AC coupled to the discriminator, which is implemented as a two-stage comparator consisting of a differential amplifier followed by an inverting amplifier. A seven-bit DAC, THESH_DAC, is used to set the threshold. Noise referred to the input is about 1000 electrons, or about 15 mV RMS out of the shaper. The nominal setting for this DAC is 4 to 5 sigma above the noise floor of 15 mV, which is 60 mV to 70 mV.

6.5 Trigger Mask

Refer to Figure and Figure . The output of the discriminator is AND'ed with the TRIGGER MASK bit for the particular channel and passed on to be OR'ed with all other channel trigger-masked outputs, to form the "FAST-OR" signal. The FAST-OR is passed to the next GTFE (or the GTRC if at the end of the MCM). This mask is used to prevent a noisy channel from contributing to the trigger rate. It may also be used for diagnostic purposes.

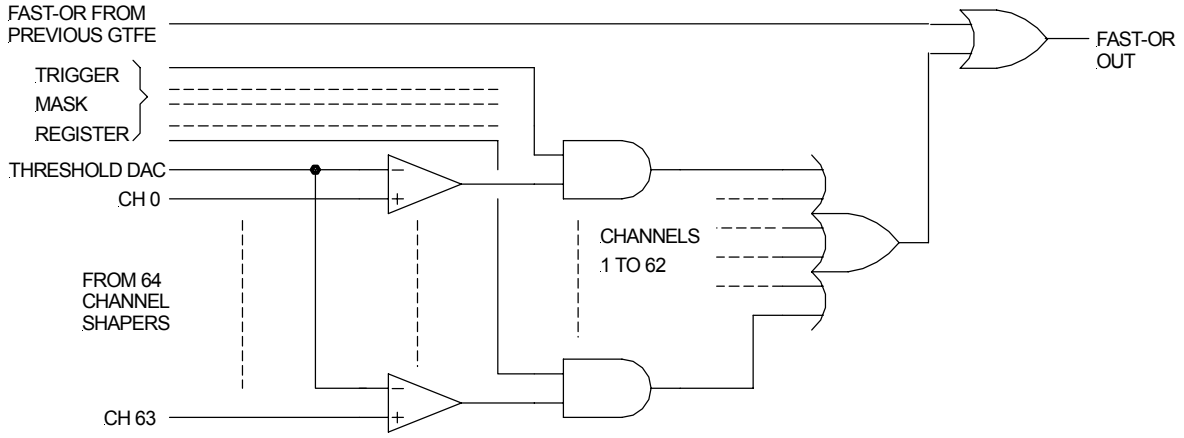

Figure 3: Trigger Output (FAST-OR) Block Diagram

6.6 Data Mask

Refer to Figure and Figure . The output of the discriminator is also ANDed with the DATA MASK bit for the particular channel. This mask is used to prevent a noisy channel from generating undue data volume for the readout. All 64 channels are OR'ed to indicate if any channel was hit. A single hit channel causes all channels of the entire GTFE to be read into the controller chip when a readout command is received, but channels without hits do not contribute to the data volume beyond the controller chip.

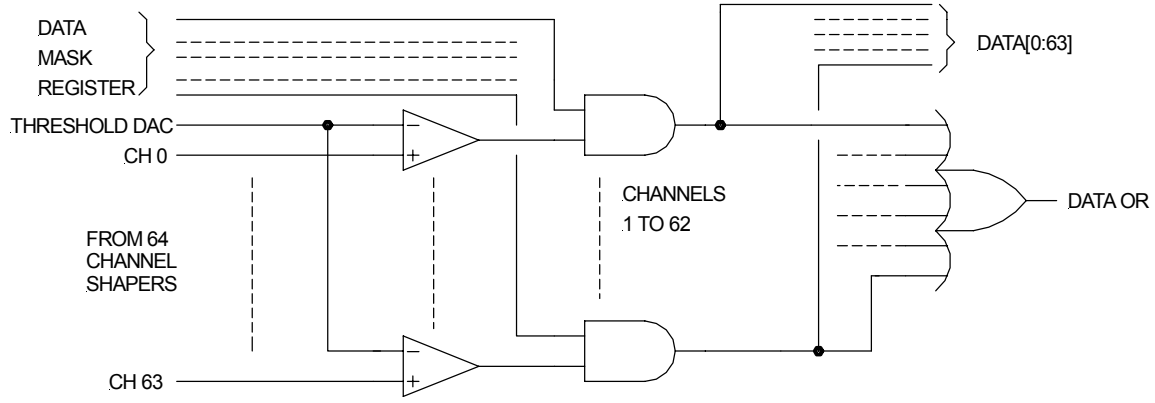

Figure 4: Data Block Diagram

6.7 Trigger, Data, and Calibration Mask Registers

Refer to Figure and Figure . Each of these three registers is 68 bits long and is loaded and read out MSB (B67) first. There is one bit for each of the 64 channels and one additional bit after each group of sixteen mask bits. The extra bits, B16, B33, B50, and B67, are used to guarantee that at least one bit is set for every thirty-two bits. This feature is needed for the readout system, which looks for a minimum of 32 zeros as a data transfer terminator. The configurations are read out non-destructively by parallel loading the data from the MASK register to an associated readout register. The 68-bit configuration registers are Single Event Upset (SEU) hardened, while the readout registers are not.

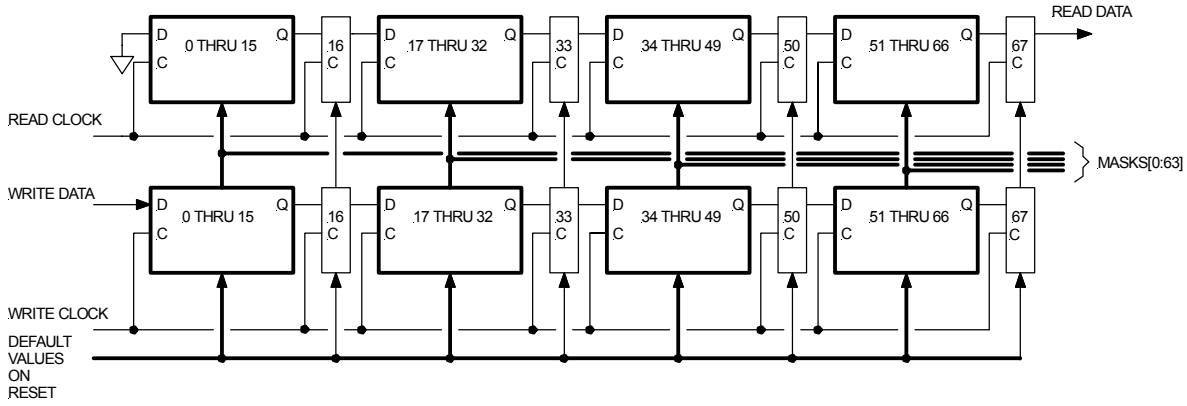

Figure 5: Mask Registers.

The MASK register bit positions are shown in Table 1. The default setting of the register when reset is logic-0 (channel disabled) for every channel of the Trigger, Data, and Calibration Mask Registers (except B16, B33, B50, and B67, which are set to logic-1).

Table 1: Mask Registers.

B0	B15	B16	B17	B32	B33	B34	B49	B50	B51	B66	B67
Ch-0	Ch-15	1	Ch-16	Ch-31	1	Ch-32	Ch-47	1	Ch-48	Ch-63	1

6.8 DAC REGISTER

The DAC REGISTER shown in Figure 1 is a 14-bit register. This register is loaded with the MSB of the command data field first and is treated as if it were 68 bits in length. The DAC bits are captured as the last 14 bits in the command data field. Each DAC has a 6-bit binary code for the voltage setting, plus a range-setting bit (BR) to choose between low and high ranges. Those map onto the data field as shown in Table 2. During read back the COMMAND DECODER clocks the readout register 68 times. The contents come out with the first 14 clock pulses (B13 first), followed by zeros.

Table 2: DAC Register Contents. The MSB (B13) is loaded first and is the first bit read out.

	THRESHOLD DAC	**CALIBRATION DAC**
DAC Setting Bits	BR B5 B4 B3 B2 B1 B0	BR B5 B4 B3 B2 B1 B0
Bits in CMD data field	B0 B1 B2 B3 B4 B5 B6	B7 B8 B9 B10 B11 B12 B13

6.9 MODE REG

The MODE REG is two bits in length, but for loading and reading it is treated as a 68 bit long register, loaded MSB (B67) first. The relevant bits appear in the last two locations of the 68-bit command data field—all others are ignored. B0, the last bit in the field (B0), controls the DEAF mode, while B1 (LEFT/RIGHT) is used to select which COMMAND DECODER, LEFT or RIGHT, is active. LEFT is the default value. The DEAF bit prevents data and trigger bits from being serially received from the previous GTFE. The purpose of this is to prevent a broken "upstream" GTFE from corrupting either the trigger or the data.

6.10 COMMAND DECODERs

Two COMMAND DECODERs, one left and one right, are implemented as shown in Figure 1 and Figure . Each command decoder receives independent CMD and CLKs from two independent readout controllers, GTRCs. This feature provides for one level of fault tolerance. The external hard RESET signal sets the LEFT COMMAND DECODER as active.

Each COMMAND DECODER is controlled by a synchronous state machine with the following four states:

1. Waiting for a start bit, which is a single logic-1 bit.
2. Clocking the 10-bit command/address field into a register, where they are presented to the command and address decoders.
3. Clocking the 68-bit data field into one of the five configuration registers.
4. Loading one of the five configuration output registers and clocking its contents out of the chip.

In addition, a COMMAND DECODER contains logic to decode command and address bits, logic to direct the clock and control signals to the configuration registers, a counter for controlling the 512-bit length of the calibration signal, and logic to provide properly timed signals for movement of data from the EVENT BUFFER into the DATA READ SHIFT REGISTER when a READ-EVENT command is decoded. The latter logic uses the two bits following the command/address field, MSB first, to form the row address for reading the EVENT BUFFER RAM.

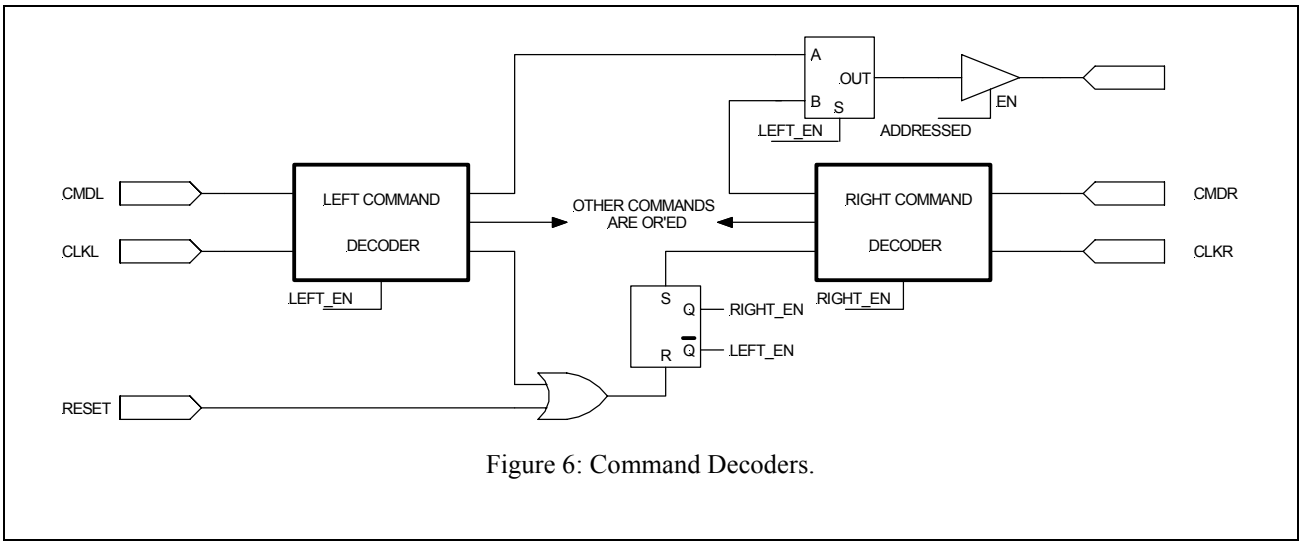

Figure 6: Command Decoders.

6.11 TRIGGER RECEIVERs

A trigger receiver circuit receives each of the L1T inputs. Each of the receivers is a synchronous state machine with two states:

1. Waiting for a start bit, which is a single logic-1 bit signaling an L1T.
2. Clocking into a register the two WRITE_ADDR bits that follow the start bit, MSB first.

At the conclusion of the second state the machine returns to the first state and produces a pulse to gate the WRITE_ADDR bits to the input of a 2-to-4 decoder, the outputs of which form the row-select write lines for the EVENT BUFFER RAM. Hence the L1T causes the discriminator/DATA-MASK outputs to be written into the appropriate row of the EVENT BUFFER.

6.12 EVENT BUFFER

Refer to Figure 1 and Figure . The EVENT BUFFER is a four-deep by 70-bit wide random-access static memory. Each of the four rows of the memory stores one complete event. When an L1T is received and decoded, the 64 bits of event data from the masked discriminators, the two bits of the WRITE_ADDR from the L1T and one bit from the OR'ed data are written into the row of the event buffer selected by WRITE-ADDR, with the latter 3 bits written into duplicate locations at each end of the memory (columns 0–2 and columns 67–69). The reason for the duplication of those 3 bits is to be able to match up with both the left and right EVENT READOUT SHIFT REGISTERS when the contents of a row of the RAM are parallel loaded into one or the other of the shift registers.

Data are transferred to the left or right 67-bit EVENT READOUT SHIFT REGISTER and then shifted out when a READ_EVENT command is received by the active command decoder. The READ_EVENT command carries the two bits of read address, READ_ADDR, immediately following the command/address field. Unless the logic in the GTFE chip glitches somehow, the READ_ADDR bits should always match the WRITE_ADDR bits stored in the EVENT BUFFER along with the data. That is because the WRITE_ADDR bits selected the row when writing to the RAM while the READ_ADDR bits selected the same row when reading. The two address bits are loaded into the leading position of the EVENT READOUT SHIFT REGISTER (the MSB in the lead), followed by the HIT bit. If the HIT bit is logic-0, then only those 3 bits are shifted out, followed by the contents of the following GTFE chip. If it is logic-1, then the 3 bits are shifted out with the 64 data bits following.

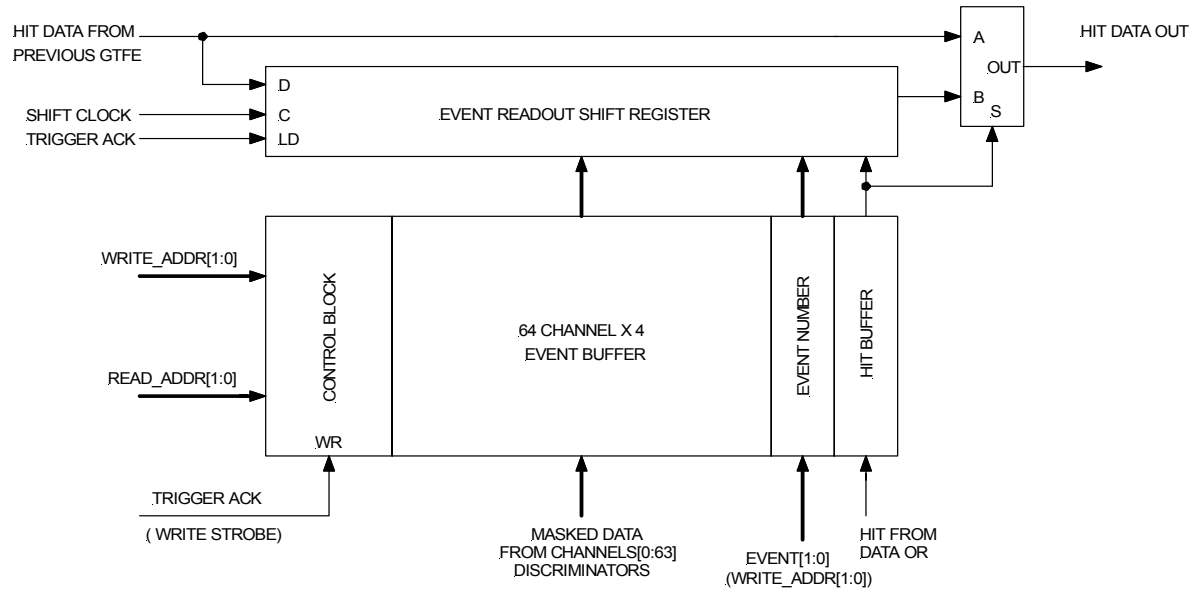

Figure 7: Event Buffer & Readout

6.13 Resets

The RESET command does nothing more than reset the contents of the configuration registers, NOT including the 2-bit MODE register. It is of limited utility, since the reset state is unlikely to be useful—the configuration registers normally must be loaded by external command, and the load commands always overwrite the previous contents.

The hard reset, via the external pad, resets everything within both command decoders (the state machines, storage registers, and the calibration-strobe counter) and resets the MODE register. It does not reset the other four configation registers.

Turning on either the analog VDD supply or the digital VDD supply results in an internal generation of a reset pulse, which in this case resets the command decoders and all 5 of the configuration registers. Hence the chip powers up in a known state regardless of the power-on sequence.

6.14 Calibration

Refer to Figure 1 and Figure . Each channel can be enabled for calibration via the CALIBRATION MASK register. The active COMMAND DECODER produces a CALIBRATION STROBE when the active COMMAND DECODER receives the CALIB_STROBE command from the associated controller, GTRC. This signal is a digital step function that remains high for 512 clock cycles. The downward step at the end injects a charge signal of the wrong polarity. Hence it must be delayed long enough to allow the amplifiers and discriminator to respond normally to the correct polarity of the upward step. The digital signal is used to gate the analog output of a seven-bit DAC to produce the controlled voltage step that is applied to the calibration capacitor of every channel with logic-1 stored within its corresponding cell of the CALIBRATION MASK register. The GTFE also has an external calibration input, to which an LVDS signal can be applied to generate asynchronously (even with the GTFE clock turned off) a CALIBRATION

STROBE, independently of the COMMAND DECODERs. This LVDS receiver normally is powered off. To be used, a high level must be applied to the external EPOM pad. It is foreseen only to be used in initial bench tests of the chip.[1]

7 GTFE Pin Assignment

The GTFE is 13 mm by 2.5 mm. The pads are wire-bonded to the MCM module, consisting of a Printed Wire Board (PWB) and pitch adapter (the latter used to connect the GTFE input pads to the silicon-strip detectors). The pads 1-8 and 49-56 are spaced at 180 μm pitch. The pads 9-48 are spaced at 300 μm pitch, and the pads 57-120 are spaced at 201 μm pitch.

Figure 8: GTFE64D Pin layout

[1] In contrast with the BTEM version of the GTFE, the new chip cannot receive an L1T without the clocks running, which limits the advantage of the external calibration input for noise studies. However, the discriminator output can still be seen at the Fast-OR without clocking the chip.

8 GTFE Pin assignment

Name	Pin	Type	Dir	Pol	Description
TRIG_RIP TRIP_RIM	1 2	LVDS	In	H	Trigger Right Input This trigger travels to the right
TRIG_LOP TRIG_LOM	3 4	LVDS	Out	H	Trigger Left Output This trigger travels to the Left
DATA_RIP DADA_RIM	5 6	LVDS	In	H	Data Right Input These data travel to the right
DATA_LOP DATA_LOM	7 8	LVDS	Out	H	Data Left Output These data travel to the left
AVDDL	9	POWER	In	N/A	Analog +2.5 volts (left side input)
QVDD	10	POWER	In	N/A	Analog +2.5 volt for input transistor well bias
AVDD2L	11	POWER	In	N/A	Analog +1.5 volts (left side input)
AGNDL	12	POWER	In	N/A	Analog ground (left side input)
A[4..0]	13-17	CMOS	In	H	GTFE address
DGNDL	18	POWER	In	N/A	Digital ground (left side input)
DVDDL	19	POWER	In	N/A	Digital 2.5 volts (left side input)
CMDLP CMDLM	20 21	LVDS	In	H	Serial command from the GTRC on the left end of the MCM
CLKLP CLKLM	22 23	LVDS 20 MHz	In	H	20 MHz clock from the GTRC on the left end of the MCM
TACKLP TACKLM	24 25	LVDS	In	H	Trigger Acknowledge (L1T, left side input)
CTRLREG	26	CMOS	Out/Tri	H	Serial control register readout
TRIG_OUTP TRIG_OUTM	27 28	LVDS	Out	H	Trigger output from the GTFE for addresses 0 and 23 only. (The two end GTFEs)
DATA_OUTP DATA_OUTM	29 30	LVDS	Out	H	Data output from the GTFE for addresses 0 and 23 only. (The two end GTFEs)
TACKRM TACKRP	31 32	LVDS	In	H	Trigger Acknowledge (L1T, right side input)
CLKRM CLKRP	33 34	LVDS 20 MHz	In	H	20 MHz clock from the GTRC on the right end of the MCM.
CMDRM CMDRP	35 36	LVDS	In	H	Serial command from the GTRC on the right end of the MCM.
EINM EINP	37 38	LVDS	In	H	Test bench calibration strobe input
EPOM	39	CMOS	In	H	Hold high to enable the EINM and EINP inputs. Internal low bias if not connected.
DVDDR	40	POWER	In	N/A	Digital 2.5 volts (right side input)
DGNDR	41	POWER	In	N/A	Digital ground (right side input)
RESET	42	CMOS	In	H	Reset GTFE. Hold high to reset. Internal low bias if not connected.

Name	Pin	Type	Dir	Pol	Description
SUBSTRATE	43	POWER	In	N/A	Substrate connection (wire bond to AGND)
AGNDR	44	POWER	In	N/A	Analog ground (right side input)
AVDD2R	45	POWER	In	N/A	Analog +1.5 volts (right side input)
AVDDR	46	POWER	In	N/A	Analog +2.5 volts (right side input)
IBIAS	47	BIAS	In	N/A	Bias input for current mirrors, 2.5µA, 0.7 volt drop
IFET	48	BIAS	In	N/A	Bias input for input transistor, 37µA 1.0 volt drop
DATA_LIM DATA_LIP	49 50	LVDS	In	H	Data Left Input These data travel to the left
DATA_ROM DATA_ROP	51 52	LVDS	Out	H	Data Right Output These data travel to the right
TRIG_LIM TRIG_LIP	53 54	LVDS	In	H	Data Left Input This data travels to the left
TRIG_ROM TRIG_ROP	55 56	LVDS	Out	H	Trigger Right Output This trigger travels to the right
ANALOG_IN[63..0]	57-120	SIGNAL	In	N/A	Analog inputs from the silicon strips

Table 4 GTFE Pin Assignment Continued

9 Command Protocol

The serial command bits received on the CMD line are as follows:

- Start-bit (‘1’)
- 5 address bits, MSB first
- 5 function bits, MSB first
- 0, 2, or 68 data bits, depending on the function, MSB first

9.1 Address Bits

The 5 address bits in a command select a particular GTFE chip from the set of 24 on an MCM, corresponding to one Tracker layer. The address of the GTFE is programmed by 5 hard-wired external CMOS input levels. The left-most GTFE has address “0000”. Address ‘11111’ signals a broadcast, which causes the command to be accepted simultaneously by all those chips on the MCM that are programmed to listen to the GTRC sending the command (or in the case of a LOAD_MODE command, all 24 chips regardless of their LEFT/WRITE bit setting). Commands for reading out configuration registers cannot be used in broadcast mode (they are ignored if sent with address ‘11111’).

That is because all 24 chips on an MCM drive the same output line, via tri-state drivers. Only one at a time can output configuration data.

Table 5. Command Function Bit Definitions

Function Bits (5 bit binary)	Command Meaning	Data Field
00000	No-op	None
00010	Reset Chip	None
00011	Generate Calibrate strobe	None
00100	Start the Event Readout sequence in the GTFE	2-bit binary address to select one of 4 event registers to be output. MSB first.
01000	Load GTFE Channel Mask	68 bits, MSB first
01001	Load GTFE Calibration Mask	68 bits, MSB first
01010	Load GTFE Trigger Mask	68 bits, MSB first
01011	Load GTFE Threshold and Calibration DACs	68 bits, of which only the last 14 are stored.
01100	Load GTFE MODE register	68 bits, of which only the last 2 are stored.
10000	Read GTFE Channel Mask	None
10001	Read GTFE Calibration Mask	None
10010	Read GTFE Trigger Mask	None
10011	Read GTFE Threshold and Calibration DAC	None
10100	Read GTFE MODE register	None

9.2 Function Bits

The definitions of the functions and their 5-bit values are shown in Table 5. The table also specifies the data field associated with the function.

9.3 Configuration Register Specification

The data fields for the three mask registers are 68 bits long, as shown in Table 1. Bits B0-B15 map to channels 0-15, bits B17-B32 map to channels 16-31, bits B34-B49 map to channels 32-47, and bits B51-B66 map to channels 48-63. Bits B16, B33, B50, and B67 are only used to guarantee that at least one bit is a logic-one for every thirty-two bits. The GTFE relies upon the GTRC to write these bits and does not enforce the requirement that they be set to logic-one. This requirement of needing at least one bit set for every thirty-two bits is due to the use by the readout system of a continuous string of 32 zeros as a data-read terminator. The data bits are written and read-back MSB first. The DAC REG (Table 2) and MODE REG are 14 bits and 2 bits long, repetitively. The GTFE treats these registers as if they

were 68 bits in length by capturing the last 14 bits or 2 bits. Hence the GTRC must always supply a complete string of 68 bits, and all but the last 14 bits or 2 bits are ignored in the case of the DAC REG and MODE REG.

9.4 Configuration Register Read back

When the two short registers are read back, the GTFE control circuitry clocks the read register 68 times, and the first bits to come out are the valid 14 bits or 2 bits, with the remainder being zeros. Hence, the read-back format is

- Data mask, trigger mask, and calibration registers: 68 bits, with the MSB first. Thus the first bit output is B67 (which should be a logic-1 if the register was correctly loaded) followed by the register setting for Channel 63, and so forth.
- DAC REG: the 14 DAC setting bits are output, MSB first, followed by 54 zeroes. Hence the first bit output is B13, the LSB of the CALIBRATION DAC (see Table 2).
- MODE REG bits: the first bit output is the LEFT/RIGHT setting, followed by the DEAF bit, followed by 66 zeroes.

The read back is via the CTRLREG pin, which is single ended CMOS with a tri-state driver. There is no start bit. Only one GTFE chip on an MCM can be read back at a given time.

9.5 Data Output Format

The data output format depends upon the value of the HIT bit, which is the OR of all 64 data outputs. It also depends on whether the chip is being read out from left to right versus from right to left. With TB0 and TB1 representing the 2-bit code supplied in the L1T (*i.e.* the EVENT BUFFER address), the four possibilities for the output bit ordering are

Shift Left (LEFT/RIGHT BIT=0, the default setting):

- HIT=1: TB1, TB0, HIT, Ch0, Ch1…Ch63.
- HIT=0: TB1, TB0, HIT

Shift Right (LEFT/RIGHT BIT=1)

- HIT=1: TB1, TB0, HIT, Ch63, Ch62…Ch0
- HIT=0: TB1, TB0, HIT

9.6 Calibration Range and Resolution

B6 of the Calibration DAC setting chooses between two ranges, with bits B0 through B5 providing in binary the DAC_Value (0 to 63) for the voltage:

Low Range (B6=0): DAC output voltage in mV = 4.5 + 4.5*DAC_Value

High Range (B6=1): DAC output voltage in mV = 12.9 + 12.9*DAC_Value

9.7 Discriminator Threshold Range and Resolution

Each GTFE contains one DAC to program the common threshold to all 64 discriminators. B6 of the DAC setting chooses between two ranges, with bits B0 through B5 providing in binary the DAC_Value (0 to 63) for the voltage:

Low Range (B6=0): DAC output voltage in mV = 4.5 + 4.5*DAC_Value

High Range (B6=1): DAC output voltage in mV = 12.9 + 12.9*DAC_Value

10 Current setting IO

Table 6 describes the external current sources required for the bias setting of the amplifiers. Resistors from the analog supply AVDDB to the corresponding GTFE pin are used on the MCM to source the desired current. Table 6 gives the approximate value required for the resistors. IFET sets the bias current of the input transistor, so its value directly impacts the noise performance. IBIAS controls other internal currents. Its value in particular affects the differentiation time constants.

Table 6. Current-setting Pin Definitions

Name	Pin#	Current	Internal Voltage Drop	Voltage Source	Bias Resistor
IBIAS	47	2.5 μA	0.7 volt	AVDDB	680 kΩ
IFET	48	37 μA	1.0 volt	AVDDB	39 kΩ

11 Power

The GTFE uses three separate power supplies. Each supply is fed into the GTFE from both the left and right sides. Note that each supply name except QVDD ends with L or R to indicate the input side. Each pair of supply pins, such as AVDDAL and AVDDAR, is connected internally in the GTFE. AVDDA(L/R) supplies power to the front-end transistor. AVDDB(L/R) pins supply power to the rest of the analog circuitry, including the two DACs, plus the calibration mask register. The noise on the AVDDA(L/R) shall be less than 200 μV RMS from DC to 1.0 MHz (TBR). The maximum peak noise shall be less than 1.0 mV (TBR). The voltage regulation shall be better than 0.05% from DC to 1 kHz (TBR).

The DVDD(L/R) pins supply power to the digital circuitry (except for the calibration mask and DAC register). The regulation shall be better than 1% from DC to 1 kHz. The noise shall be less than 1.0 mV RMS from DC to 1.0 MHz. The maximum peak noise shall be less than 5 mV.

Table 7: Power Pin Definitions.

Name	Pin#	Voltage	Power
AVDDAL	11	1.5 V ± 5%	3.5 mW
AVDDAR	45	1.5 V ± 5%	
AVDDBL	9	2.5 V ± 5%	0.75 mW
AVDDBR	46	2.5 V ± 5%	
QVDD	10	2.5 V ± 5%	none
DVDDL	19	2.5 V ± 5%	1.75 mW (TBR)
DVDDR	40	2.5 V ± 5%	
AGNDL	12	0	
AGNDR	44	0	
DGNDL	18	0	
DGNDR	41	0	
SUBSTRATE	43	0	

Table 8: Nominal Performance and Timing Specifications

RMS Equivalent Noise Charge	1300 electrons or 0.21 fC (TBR)
Gain from channel input to the discriminator input	70 mV/fC at 1 fC input signal (TBR)
Shaper output peaking time	1.7 μs (TBR)
Threshold dispersion across a chip (includes effects of gain variation as well as discriminator offsets).	10 mV rms (TBR)
Time delay from the beginning of the start bit of a READ_EVENT command and the first bit of the output data.	TBR ns
Phase of the output data bits relative to the input clock.	? ns after the rising clock edge
Time delay from the beginning of the start bit of a READ_REG command and the first bit of the output data.	TBR ns
Phase of the register output bits relative to the input clock.	? ns after the rising clock edge

12 Performance and Timing Specifications

Table 8 gives nominal values for the GTFE performance specifications plus some timing information relevant to reading data and configuration register contents from the chip.