GLAST LAT SYSTEM SPECIFICATION	Document # **LAT-SS-00170**	Date Effective Draft 9/30/00
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	Subsystem/Office Electronics System	
Document Title **Conceptual Design of the GLAST Tracker Readout Controller Electronics ASIC**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Conceptual Design of the

Glast Tracker Readout Controller Electronics (GTRC)

ASIC

DOCUMENT APPROVAL

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CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
	03/29/2001	Added Token Parity Error to the Control Register
	08/23/2000	Version 2 Document changes. New Protocol from TEM to GTRC.
	08/24/2000	Defined 68 Bit Data read Redefined the Read Event Formats
	08/28/2000	Added GTFE to GTRC Readout Data Format
	09/05/2000	Added GTRC Register control of Fast-OR Stretching Added Fast-OR Rate Register Fixed Error in Bit encoding for GTRC and GTFE Commands (0x20) => 0x10, (0x10) => 0x08
	09/11/2000	Added Parity Bit for the Command Field
	09/13/2000	Added Parity defined
	09/26/2000	Swapped MSB and LSB AGAIN
	09/29/2000	Added Reset differential to chip layout Added differential reset output to GTFE
	10/04/2000	Removed Rate counter 3 Bit Tags
	10/20/2000	2 Bit Tags; Single ended reset to GTFE; Changed signal names; Revised Event Data Definitions; Read_Event becomes a Load command, not dataless.
	11/07/2000	Update Pin numbers and other stuff per Dave Nelson
	11/27/2000	Clearified Command/Data bit definitions
	01/05/2001	Changed Tag and Hit bits around from GTFE
	04/12/2001	Added logic type to pin definitions
	05/07/2001	Changed Pin definitions of TOKEN and SDATA

TABLE OF CONTENTS

1 PURPOSE

This document describes the conceptual design for the GLAST Large Area Telescope (LAT) Tracker Readout Controller Electronics (GTRC) ASIC.

2 SCOPE

This document gives an overrview over the conecptual architecture of the GLAST LAT (LAT) Tracker Readout Controller Electronics (GTRC) ASIC.

3 DEFINITIONS

3.1 Acronyms

GLAST – Gamma-ray Large Area Space Telescope

GRB – Gamma-Ray Burst

LAT – Large Area Telescope

TBR – To Be Resolved

CAL – Calorimeter Detector

TRG – L1 Trigger

GLB-TRG – Global L1 Trigger

TEM – Tower Electronics Module

3.2 Definitions

μsec, μs – Microsecond, 10^{-6} second

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations..

s, sec – seconds

4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the GTRC concept and its requirements include the following:

4.1 Requirement Documents

GE-00010, “GLAST LAT Performance Specification”, August 2000

GLAST00010, “GLAST Science Requirements Document”, P.Michelson and N.Gehrels, eds., July 9, 1999.

Add more

4.2 Conceptual Design Documents

[1] LAT Electronics System – Conceptual Design

[2] LAT TKR-CAL Tower Electronics Module – Conceptual Design

[3] LAT Control Protocol within LAT – Conceptual Design

[4] LAT Data Protocol within LAT – Conceptual Design

[5] LAT Housekeeping within LAT – Conceptual Design

[6] LAT L1 Trigger System – Conceptual Design

5 INTRODUCTION

6 GTRC Description

6.1 GTRC Overview

7 List of Bonding Pads

List of Bonding Pads					
Name	Pin #	Type	Dir	Pol	Description
SDI	2				SCAN Chain Debugging pad
TREQ_INP TREQ_INM	3 4	2	I	H	Trigger Request input from GTFE's
RD_INP RD_INM	5 6	2	I	H	Event Data input from the GTFE's
CTRLREG	7	6	I	H	Input from GTFE Control Register read
RESETB	8	5	O	H	Reset Output to GTFE's
LEFT	9	6	I		1 => Left Side, 0 => Right Side
DRV_BIAS	10	7			Current Bias for LVDS Drivers
NTOKENP NTOKENM	11 13	8	I	L	Token input from layer below or TEM.
NTOKEN_OUTP NTOKEN_OUTM	14 15	3(L)	O	L	Token output to the layer above.
NSDATA_INP NSDATA_INM	16 17	8	O	L	Data input from the layer above.
NSDATAP NSDATAM	18 19	3(P)	I	L	Data output to the layer below or TEM
NSCMDP NSCMDM	20 21	1	I	L	Serial Command input from TEM
CLKP CLKM	22 24	1	I	H	Clock input from TEM
NTACKP NTACKM	25 26	1	I	L	Level-1 Trigger strobe from TEM
NTREQP NTREQM	27 28	3(H)	O	L	Trigger Request output to the TEM
NRESETP NRESETM	29 30	1	I	L	Reset Chip input from TEM. Must be at least 3 Clocks Wide.
A0 A1 A2 A3	31 32 33 35	6	I	H	Chip Address If Address = 0x00, GTRC is driving the Cable to the TEM, then increase the current drive capability.
CLKBP CLKBM	38 39	4	O	H	Clock output to the GTFE's
SCMD_OUTP SCMD_OUTM	40 41	4	O	H	Serial Command output to the GTFE's
TACKBP TACKBM	42 43	4	O	H	Level-1 Trigger Strobe output to the GTFE's.
SE	44				SCAN Chain Debugging pad

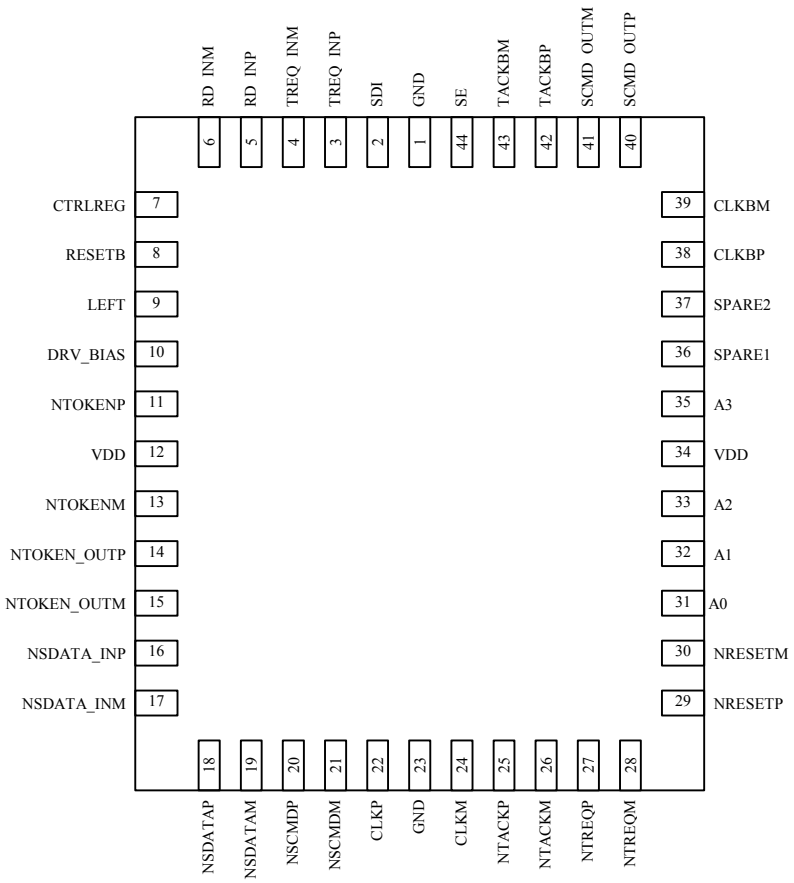
7.1 List of Bonding Pads (Continued)

List of Bonding Pads (Continued)					
Name	Pin #	Type	Dir	Pol	Description
GND	1, 23				Digital Ground
VDD	12, 34				Digital Power
SPARE	36, 37				Spare Pins. Leave unconnected.

7.2 Definition of PAD Types

TYPE	Cell Name	Definition
1	LVDS_RX	LVDS Receiver No Clamping
2	LVDS_RXLC	LVDS Receiver Light Clamping (3ua)
3	LVDS_TXP	LVDS Driver with Programmable Drive (L) Always Low Drive (H) Always High Drive (P) High Drive for GTRC address=0
4	LVDS_TX	LVDS Driver
5		CMOS Driver
6		CMOS Receiver W/Pull Down
7		Analog Bias Current Input
8	LVDS_RXHC	LVDS Receiver with Heavy Clamping (200ua)

8 Bonding Pad Layout and Placement



Bonding Pad Layout
for the GTRC Chip
(not to scale)

8.1 Die Size

4.5mm X 4.5mm

9 Command Format

Commands are received by the GTRC. The GTRC decodes the command and if, necessary, transmits the command to the GTFE. Command to the GTFE begin with a Start Bit, however, data from the GTFE to the GTRC is Dead-Reckoned since the timing between the GTRC and the GTFE on reads is deterministic.

9.1 GTRC Command Format from TEM to GTRC

Command Format from TEM to GTRC			
Bit	Name	Definition	Value
	Start		1
[15..12]	GTRC_ADDR	4 Bit GTRC (Layer) Address. Address 0x0 is the GTRC closest to the TEM. Address 0xF is a Broadcast address	[0000] ↓ [1000] [1111]
11	GTFE_FUNC	0 => Following Function is for the GTRC 1 => Following Function is for the GTFE	
[10..06]	GTFE_ADDR	5 Bit GTFE Address If GTFE_FUNC = 0; this field is ignored If GTFE_FUNC = 1; Address and function passed to GTFE Address 0x1F is a Broadcast address	[00000] ↓ [10111] [11111]
[05..00]	FUNCTION	5 Bit Function code If GTFE_FUNC = 0; GTRC Function If GTFE_FUNC = 1; GTFE Function [00xxx] => Dataless Functions [01xxx] => Load Functions [10xxx] => Read Functions	See following tables
68	CMD_PARITY	ODD Parity for the Command Field. The Command is not executed if there is a Command Parity Error	
[67..00]	DATA	68 Bit Data field. This field is only sent on Load Functions	See 68 Bit Data format table
	DAT_PARITY	ODD Data Parity	

9.2 Parity Bit

Both the Command Field and the Data Field have ODD Parity. The Command Field Parity, CMD_PARITY, includes Bits 00-15. The Data Field Parity, DAT_PARITY includes Bits 17-84. In

the case of Read functions, the DAT_PARITY will also include the SUM_PARITY bit that is attached to the end of the Data Field.

If there is a CMD_PARITY error, the GTRC will ignore the command and wait 68+ clock cycles before looking for a new start bit. The command will not be forwarded to the GTFE's. If there is a DAT_PARITY error while loading the GTRC control register, the control register will not be loaded. However, if the DAT_PARITY error occurs on a load command to the GTFE, the command and data will have already been sent to the GTFE.

The TOKEN and the L1Trigger also have parity bits associated with them. Errors in these signal's parity bit will set the corresponding bit in the control register. The value attached to the signal will be used however.

9.3 GTFE Command Format from GTRC to GTFE

Command Format from GTRC to GTFE			
Bit	Name	Definition	Value
	Start		1
[77..73]	GTFE_ADDR	5 Bit GTFE Address Address 0x1F is a Broadcast Address	[00000] ↓ [10111] [11111]
[72..68]	FUNCTION	5 Bit Function to be performed. [00xxx] => Dataless Functions [01xxx] => Load Functions [10xxx] => Read Functions	See following table
[67..00]	DATA	68 Bit Data field. This field is only sent on Load Functions.	

Address 0x1F is a broadcast address for both the GTRC and GTFE. Broadcast Reads of the GTFE are ignored by the GTFE, however, the GTRC will send back a zero data word since the tri-state input of the CNTRLREG is pulled low (logical '0'). If the GTRC address is a Broadcast address, the first GTRC will respond and send back a Zero data word.

9.4 Data Format

The data is always sent out as a 64 Bit number with a '1' inserted every 17th bit. Since in all cases the data word is preceded by a non-zero function field, this makes the data word 68 Bits without the possibility of 32 '0's in a row. This means that 32 Bits of '0' in a row can be used as a unique trailer. The data is right justified. When loading a register, the receiving chip always shifts by 68. The resulting N-bit word will end up in the correct location in an N-bit shift register.

9.4.1 68 Bit Data Format

68 Bit Data Format			
Bit	Name	Definition	Value
67		'1'	1
[66..51]		DATA[63..48]	
50		'1'	1
[49..34]		DATA[47..32]	
33		'1'	1
[32..17]		DATA[31..16]	
16		'1'	1
[15..00]		DATA[15..00]	

10 GTRC Function Definitions

GTRC Commands are sent from the TEM to the GTRC with ODD Parity. The command is not executed if there is a Command Parity Error. The parity bit is stripped off of commands that are passed on to the GTFE. If a Command Parity Error is detected, the CMD_ERR bit in the GTRC Control Register is set (probably all GTRC's will see the parity error). This bit will stay set until the GTRC Control Register is read. The SUM_ERR bit is returned in every read operation from the GTRC.

GTRC Function Definitions			
Function	CODE	Name	Definition
Dataless			
0x00	[00000]	NOP	
0x01	[00001]	RST_GTRC	Reset GTRC Chip. Sets Control register to default value.
0x04	[00100]	READ_EVENT	Starts the Event Readout sequence in GTRC
Load			
0x08	[01000]	LD_GTRC_REG	Load the GTRC Control Register
0x09	[01001]	LD_GTFE_SYNC	Load the GTFE Sync Register
Read			
0x10	[10000]	RD_GTRC_REG	Read the GTRC Control Register
0x11	[10001]	RD_GTFE_SYNC	Read the GTFE Sync Register

11 GTFE Function Definitions

GTFE Commands are passed from the TEM through the GTRC to the GTFE.

GTFE Function Definitions			
Function	CODE	Name	Definition
Dataless			
0x00	[00000]	NOP	
0x01	[00001]		
0x02	[00010]	RST_CHIP	Reset GTFE Chip.
0x03	[00011]	CALIBRATE	Starts the Calibration sequence in the GTFE
0x04	[00100]	READ_EVENT	Starts the Event Readout sequence in GTFE
Load			
0x08	[01000]	LD_CHN_MSK	Load GTFE Channel Mask
0x09	[01001]	LD_CAL_MSK	Load GTFE Calibration Mask
0x0A	[01010]	LD_TRG_MSK	Load GTFE Trigger Mask
0x0B	[01011]	LD_TH/C_DAC	Load GTFE Threshold and Calibration DAC's
0x0C	[01100]	LD_MUTE	Load GTFE Mute and Shift Control
Read			
0x10	[10000]	RD_CHN_MSK	Read GTFE Channel Mask
0x11	[10001]	RD_CAL_MSK	Read GTFE Calibration Mask
0x12	[10010]	RD_TRG_MSK	Read GTFE Trigger Mask
0x13	[10011]	RD_TH/C_DAC	Read GTFE Threshold and Calibration DAC's
0x14	[10100]	RD_MUTE	Read GTFE Mute and Shift Control

12 GTRC Commands

12.1 GTRC Dataless Functions

Dataless functions are not really dataless. A 64 bit data word of zeros is sent. This 64 bit word is sent in the standard 68 bit field with ODD parity. The Data parity is checked and the DAT_Err Bit in the Control register is set if there is an error. The command is executed if there is a data parity error but not if there is a command parity error.

12.1.1 RST_GTRC

Resets the GTRC. This command will set the Control Register to the default value.

Reset GTRC			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	0 => GTRC Function follows	0
[09..05]	GTFE_ADDR	Unused	
[04..00]	FUNCTION	RST_GTRC	0x01
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	Zero value in 68 Bit Data Format	See 68 Bit Data Format
	DAT_PARITY	ODD Data Parity	

12.2 GTRC Load Functions

12.2.1 Load GTRC Control Register from TEM to GTRC

Loads the Control register in the GTRC. Both Command and Data parity is checked. The command will not be executed if there is any parity error.

Load GTRC Control Register			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	0 => GTRC Function follows	0
[09..05]	GTFE_ADDR	Unused	
[04..00]	FUNCTION	LD_GTRC_REG	0x08
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	33 Bit GTRC Control Register value in 68 Bit Data Format	See 68 Bit Data Format
	DAT_PARITY	ODD Data Parity	

12.2.2 GTRC Control Register

GTRC Control Register Format			
Bit	Name	Definition	Default
33	LD_FT	Enable loading FORCE and TOT bits	
32	LD_DELAY	Enable loading READ_DELAY	
31	LD_STRETCH	Enable loading STRETCH	
30	LD_CNT	Enable loading GTFE_CNT	
29	LD_SIZE	Enable loading SIZE	
28	SUM_ERR	Read only Logical OR of TAG, TRIG, DAT and CMD errors Cleared by reading Control Register	
27	CMD_ERR	Read only Sum Cmd Parity Error Set if there is a Cmd Parity Error Clear by reading Control Register	
26	DAT_ERR	Read only Sum Data Parity Error. Set if there is a Data Parity Error Cleared by reading Control Register	
25	TRIG_ERR	Read only Sum Trigger Parity Error Set if there is an L1T Parity Error Cleared by reading Control Register	
24	TOK_ERR	Read only Sum Token Parity Error Set if there is a Token Parity Error Cleared by reading Control Register	
23	TAG_ERR	Read only Sum Tag Error Set if there is a comparison failure in the TAG from the GTFE's. Cleared by reading Control register	
22	SHIFT_MODE	Read only. Bonded pad to determine side	
21	TOT_EN	1 => Enable TOT Delay	1
20	FORCE_NO_ERR	0 => Normal operation 1 => Forces Normal Event readout	0
[19..17]	READ_DELAY	Delay from Read Event to start of Read Command in 6.4us steps	0
[16..12]	OR_STRETCH[4..0]	Fast-OR Stretch in 50ns steps. 0 => No Deglitch, No Stretch	10
[11..07]	GTFE_CNT	Number of GTFE chips to read	12
[06..00]	SIZE	Number to set maximum number of Hits from GTFE	64

12.2.3 Load GTRC GTFE_SYNC from TEM to GTRC

Loads the GTFE SYNC register in the GTRC. The value in this register is used to align the data coming from the GTFE with the GTRC. The default value of 8 should work but if something changes in the GTFE, this value can be changed so that a new GTRC does not have to be produced. Both Command and Data parity is checked. The command will not be executed if there is any parity error.

Load GTFE SYNC Control Register			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	0 => GTRC Function follows	0
[09..05]	GTFE_ADDR	Unused	
[04..00]	FUNCTION	LD_GTFE_SYNC_REG	0x09
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	5 Bit GTRC GTFE_SYNC Register value in 68 Bit Data Format	See 68 Bit Data Format
	DAT_PARITY	ODD Data Parity	

12.3 GTRC Read Functions

Reads the contents of the GTRC Registers. This command puts data out on the DOUT line. Unaddressed GTRC chips will clock NSDATA_IN to NSDATA. The addressed GTRC will transmit its Control Register contents and send it as Dout to the next GTRC in the following format. No broadcast address allowed for Read GTRC. The SUM_ERR bit is returned in the all read functions. This bit is the SUM of Parity errors in all previous commands, including the current read, since the last read of the GTRC Control Register.

If a read is attempted on a nonexistant GTRC register, the command will be echoed back and a data value of zero will be returned.

12.3.1 Read GTRC Control Register from TEM to GTRC

Read GTRC Register Data Format from TEM to GTRC			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	0 => GTRC Function follows	0
[09..05]	GTFE_ADDR	Unused	
[04..00]	FUNCTION	RD_GTRC_REG	0x10
	CMD_PARITY	ODD Command Parity	

12.3.2 Read GTRC Control Register from GTRC to TEM

Read GTRC Register Data Format from GTRC to TEM			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	0 => GTRC Function follows	0
[09..05]	GTFE_ADDR	Unused	
[04..00]	FUNCTION	RD_GTRC_REG	0x10
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	Bit GTRC Control Register value in 68 Bit Data format	
68	SUM_ERR	Status of SUM_Err in the Control Register.	
	PARITY	ODD Data Parity	

12.3.3 Read GTRC GTFE_SYNC Register from TEM to GTRC

Read GTRC Register Data Format from TEM to GTRC			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	0 => GTRC Function follows	0
[09..05]	GTFE_ADDR	Unused	
[04..00]	FUNCTION	RD_GTFE_SYNC	0x11
	CMD_PARITY	ODD Command Parity	

12.3.4 Read GTRC GTFE_SYNC Register Data from GTRC to TEM

Read GTRC Register Data Format from GTRC to TEM			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	0 => GTRC Function follows	0
[09..05]	GTFE_ADDR	Unused	
[04..00]	FUNCTION	RD_GTFE_SYNC	0x11
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	4 Bit GTRC GTFE_SYNC value in 68 Bit Data format	
68	SUM_ERR	Status of SUM_Err in the Control Register.	
	PARITY	ODD Data Parity	

13 GTFE Commands

13.1 GTFE Dataless Functions

Start Bit, GTFE Address, and GTFE Function are sent to the GTFE.

13.1.1 Dataless Functions from TEM to GTRC

Dataless Function Format from TEM to GTRC			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	1 => GTFE Function follows	0
[09..05]	GTFE_ADDR	5 Bit GTFE Address	
[04..00]	FUNCTION	5 Bit Function code	
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	4 Bit GTRC GTFE_SYNC Register value in 68 Bit Data Format	See 68 Bit Data Format
	DAT_PARITY	ODD Data Parity	

13.1.2 Dataless Functions from GTRC to GTFE

Dataless Function Format from GTRC to GTFE			
Bit	Name	Definition	Value
	Start		1
[09..05]	GTFE_ADDR	5 Bit GTFE Address	
[04..00]	FUNCTION	5 Bit Function code	

13.1.3 READ_EVENT Command

The READ_EVENT Command is a special case. Only the 2 MSB's of the data are used. These bits define the EVENT Number that is to be read from the GTFE. The entire 68 bit data field is sent.

13.2 GTFE Load Register Functions

13.2.1 Load Register Function from TEM to GTRC

Load Register Function Format from TEM to GTRC			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	1 => GTFE Function follows	1
[09..05]	GTFE_ADDR	5 Bit GTFE Address	
[04..00]	FUNCTION	5 Bit Function code	
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	64 Bit Data in 68 Bit Data Format	
	DAT_PARITY	ODD Data Parity	

13.2.2 Load Register Function from GTRC to GTFE

Load Register Function Format from GTRC to GTFE			
Bit	Name	Definition	Value
	Start		1
[77..73]	GTFE_ADDR	5 Bit GTFE Address	
[72..68]	FUNCTION	5 Bit GTFE Function	
[67..00]	Data	64 Bit Data in 68 Bit Data Format	

13.3 GTFE Read Register Functions

The Addressed GTFE Chip puts it's data out on it's CNTLREG output pin. The GTRC receives this data on it's CNTLREG pin and then sends it to the TEM. The GTFE and GTRC address sent with the Read command is 'echoed' back. Unaddressed GTRC chips clock the data from Din to Dout. The Addressed GTRC, will clock data from it's CNTLREG input to Dout. No broadcast address accepted by the GTRC or GTFE.

13.3.1 Read GTFE Register Function from TEM to GTRC

Read Register Function Format from TEM to GTRC			
Bit	Name	Definition	Value
0	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	1 => GTFE Function follows	1
[09..05]	GTFE_ADDR	5 Bit GTFE Address	
[04..00]	FUNCTION	5 Bit Function code	
	CMD_PARITY	ODD Command Parity	

13.3.2 Read GTFE Register Function from GTRC to GTFE

Read Register Function Format from GTRC to GTFE			
Bit	Name	Definition	Value
	Start		1
[09..05]	GTFE_ADDR	5 Bit GTFE Address	
[04..00]	FUNCTION	5 Bit Function code	

13.3.3 Read GTFE Register from GTFE to GTRC

Read Function Format from GTFE to GTRC			
Bit	Name	Definition	Value
[67..00]	DATA	64 Bit Data in 68 Bit Data Format	

13.3.4 Read GTFE Register from GTRC to TEM

Read GTFE Command Format from GTRC to TEM			
Bit	Name	Definition	Value
	Start		1
[14..11]	GTRC_ADDR	4 Bit GTRC (Layer) Address.	
10	GTFE_FUNC	1 => GTFE Function follows	1
[09..05]	GTFE_ADDR	5 Bit GTFE Address	
[04..00]	FUNCTION	5 Bit GTFE Read Function	
	CMD_PARITY	ODD Command Parity	
[67..00]	DATA	64 Bit Data in 68 Bit Data Format	
68	SUM_ERR	Status of SUM_Err in the GTRC Control Register.	
	PARITY	ODD Data Parity	

14 TRIGGER

The NTACK includes the Event TAG and parity. If a parity error is detected, the TAG_ERR bit in the GTRC Control Register is set. The ERROR bit is set in the Event Data as well as the TAG_ERR bit.

14.1 Trigger Format

Trigger Format			
Bit	Name	Definition	Value
0	TACK_START	Start Bit for Trigger	1
[2..1]	EVNT_TAG	2 Bit Event TAG	
3	EVNT_PARITY	ODD Event Parity	

14.2 READ Data Packet

The contents of the READ Data Packet depends on the status of the DAV (Data AVailable) bit from each GTFE, the ERROR bit, the FORCE_NOERR bit in the GTRC Control register, and the actual amount of data in each GTFE. The FORCE_NO_ERR bit in the GTRC Control Register will prevent the GTRC from checking for TAG Compare errors forcing the Normal Operating mode. 24 TAG Bit values are sent regardless of the number of GTFE chips set to be read in the GTRC Control Register.

The TRIG_ERR is set if there is a parity error on the Trigger word at the GTRC. The TAG_ERR bit is set if the TAGs from the GTFE and GTRC don't all match.

14.2.1 Read GTFE Event Data from GTFE to GTRC

Read GTFE Event Data from GTFE to GTRC			
Bit	Name	Definition	Value
[01..00]	EVNT_TAG0	Event Tag for data	
2	DAV0	Data Available	
[66..03]	EVNT_DATA0	If DAV0 = 1; Event Data	
	EVNT_TAG1	Event Tag for data	
	DAV1	If DAV0 = 0; No Event Data.	
	EVNT_DATA1	If DAV1 = 1; Event Data	

Note: There is no Start Bit, EVNT_TAG0 is dead-reckoned from begining of the command. The GTFE_SYNC value is used to change the alignment of EVNT_TAG0 with respect to the end of the Read_Event command.

14.2.2 Normal Operating Mode without Data

Normal Operating - ERROR=0, DAV=0			
Word	Name	Bits	Definition
	START		Start Bit
1	Layer Header	[10..00]	Layer Header
	PARITY		ODD Parity of Word 1

14.2.3 Normal Operating Mode with Data

Normal Operating - ERROR=0, DAV=1			
Word	Name	Bits	Definition
	START		Start Bit
1	Layer Header	[10..00]	Layer Header
	PARITY		Odd Parity of Word 1
2	Number of Words	[10..00]	Number of words to follow
	PARITY		Odd Parity of Word 2
[N..3]	Strip Data	[10..00]	Hit Strip Numbers
N+1	TOT	[10..00]	TOT
	PARITY		Odd Parity of words 3 thru N+1

14.2.4 Error Mode without Data

Error Operating - ERROR=1, DAV=0			
Word	Name	Bits	Definition
	START		Start Bit
1	Layer Header	[10..00]	Layer Header
	PARITY		Odd Parity of Word 1
2	Number of Words	[10..00]	Number of words to follow
	PARITY		Odd Parity of Word 2
[7..3]	Tags	[10..00]	Tag words from GTFEs
	PARITY		Odd Parity of words 3 thru 7

14.2.5 Error Mode with Data

Error Operating - ERROR=1, DAV=1			
Word	Name	Bits	Definition
	START		Start bit
1	Layer Header	[10..00]	Layer Header
	PARITY		Odd Parity of Word 1
2	Number of Words	[10..00]	Number of words to follow
	PARITY		Odd Parity of Word 2
[7..3]	Tag	[10..00]	Tag words from GTFEs
[N..8]	Strip Data	[10..00]	Hit Strip Numbers
N+1	TOT	[10..00]	TOT
	PARITY		Odd Parity of Words 3 thru N+1

14.2.6 Layer Header Format

Layer Header Format		
Bits	Name	Definition
[03..00]	GTRC_ADDR	4 Bit GTRC Address
4	DAV	Data Available
5	ERROR	SUM_ERR status in GTRC Control Register
6	TAG_ERR	TAG compare Error
[08..07]	GTRC_TAG	2 Bit TAG word received by GTRC
[10..09]	SPARE	Spare Bits

14.2.7 Strip Data Format

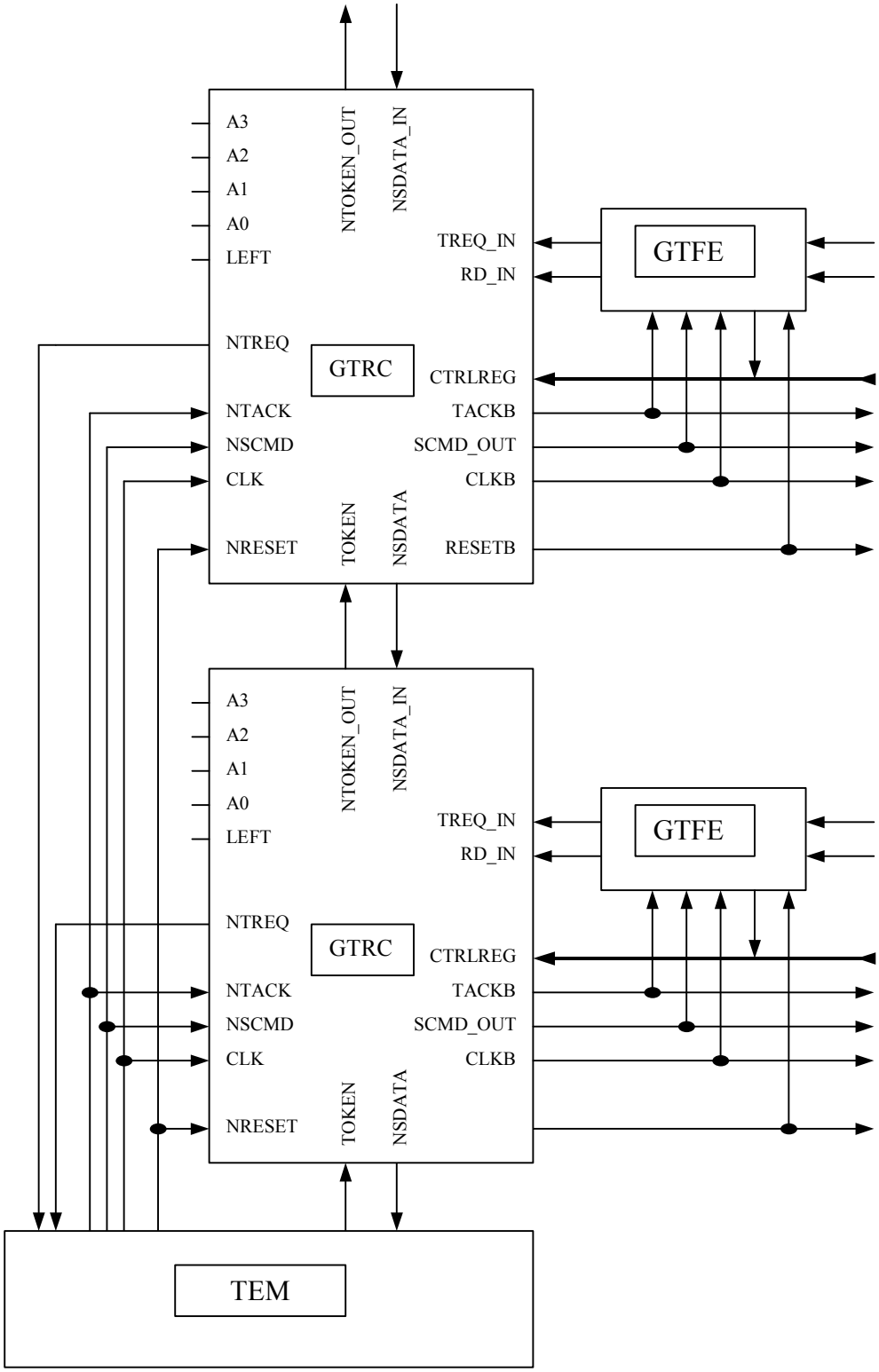
Strip Data Format		
Bits	Name	Definition
[04..00]	GTFE_ADDR	5 Bit GTFE Address
[10..05]	STRIP	6 Bit Strip Number

14.2.8 TAG word Format

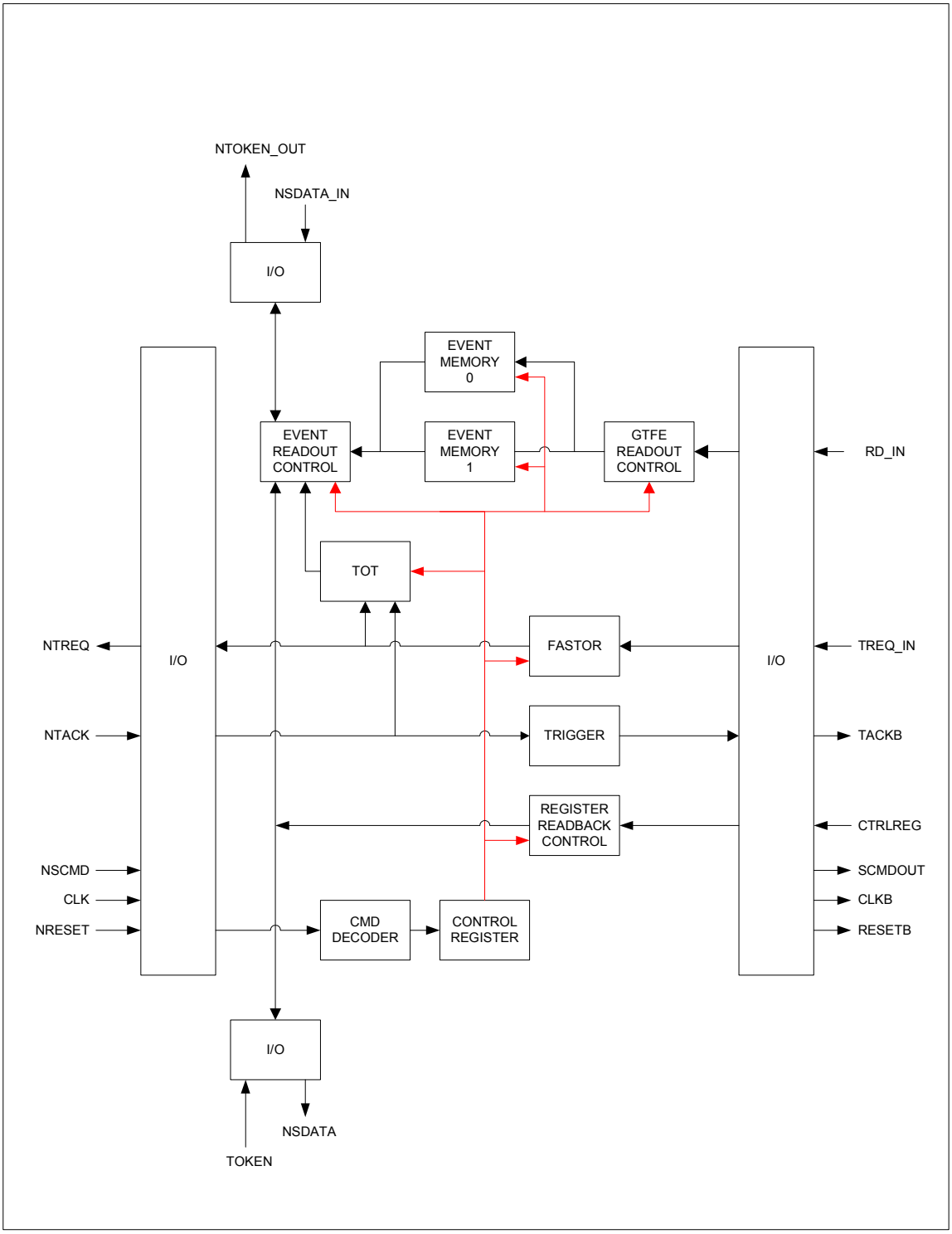
The TAGs are read from each of the GTFE chips during the Read Event, even if the maximum number of hits has been exceeded. If the number of GTFE's to be read is less than 24, the unread GTFE TAGs will be set to the last read GTFE's TAG. For example, if GTFE_CNT is set to 12 in the GTRC Control Register, then TAG[11..00] will be the TAGs read from GTFE[11..00] and TAG[23..12] will be the TAGs from GTFE[11].

TAG Word Format			
Word	Name	Bits	Definition
0	TAG0	[01..00]	GTFE0
		[03..02]	GTFE1
		[05..04]	GTFE2
		[07..06]	GTFE3
		[09..08]	GTFE4
		10	'1'
1	TAG1	[01..00]	GTFE5
		[03..02]	GTFE6
		[05..04]	GTFE7
		[07..06]	GTFE8
		[09..08]	GTFE9
		10	'1'
2	TAG2	[01..00]	GTFE10
		[03..02]	GTFE11
		[05..04]	GTFE12
		[07..06]	GTFE13
		[09..08]	GTFE14
		10	'1'
3	TAG3	[01..00]	GTFE15
		[03..02]	GTFE16
		[05..04]	GTFE17
		[07..06]	GTFE18
		[09..08]	GTFE19
		10	'1'
4	TAG4	[01..00]	GTFE20
		[03..02]	GTFE21
		[05..04]	GTFE22
		[07..06]	GTFE23
		[10..08]	[100]

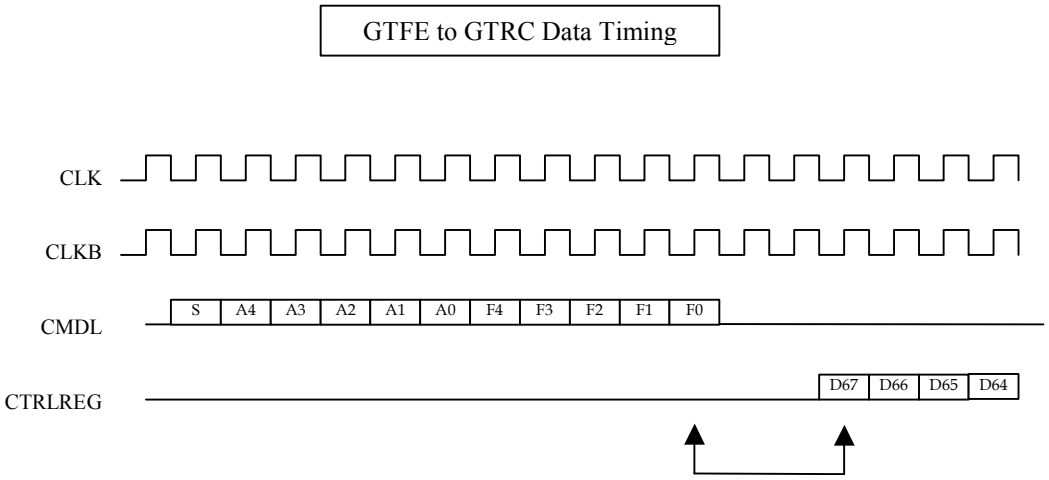
15 System Block Diagram



16 GTRC Internal Block Diagram



17 Timing



18 Operation

18.1 Time-Over-Threshold

The Time-Over-Threshold (TOT) is a 7-Bit counter clocking at CKI/4 (200ns). This gives a full scale TOT of 25.4Us (127*200ns). The TOT Counter starts when the TOT_EN bit is set in the control register and there is a Trigger and a Fast-OR signal. The counter stops when the Fast_OR signal ends or the counter over-flows. If the TOT_EN bit is set in the control register, the event data will not be sent out until the TOT ends.

18.2 TOKEN

The TOKEN is a 3 bit command. It starts with a start bit and ends with a parity bit. The second bit is the buffer number that the GTRC will transmit back to the TEM. Normally, the data on the NSDATA_In pin is shifted out the NSDATA pin on the GTRC. If a valid TOKEN is received, the GTRC will shift the contents of the requested buffer out to the TEM on the NSDATA pin. When finished, the GTRC will pass the TOKEN to the next GTRC in the chain. If the TOKEN is invalid (not 100 or 111) it is ignored, it will not get passed to the next GTRC.

19 Interface

20 Signal Name Changes from V1 to V2

Old Name	New Name
TRIP TRIN	TREQ_INP TREQ_INM
RDIP RDIN	RD_INP RD_INM
DVDD	DVDD
DGND	DGND
SDI	SDI
SE	SE
TOKIP TOKIN	NTOKENP NTOKENM
TOKOP TOKON	NTOKEN_OUTP NTOKEN_OUTM
DINP DINN	NSDATA_INP NSDATA_INM
DOUTP DOUTN	NSDATAP NSDATAM
CMDIP CMDIN	NSCMDP NSCMDM
CLKIP CLKIN	CLKP CLKM
TACKIN TACKIP	NTACKP NTACKM
TOUTP TOUTN	NTREQP NTREQM
CMDLP CMDLN	SCMD_OUTP SCMD_OUTM
CLKLP CLKLN	CLKBP CLKBM
TACKLP TACKLN	TACKBP TACKBM
CTRLREG	CTRLREG
New Signal	NRESETP NRESETM
New Signal	RESETB
New Signal	LEFT
A3 A2 A1 A0	A3 A2 A1 A0
New Signal	DRV_BIAS