Test results of power consumption and differential receiver of GTFE64D

(Section numbering is accorded to LAT-TD-246)

7 Power Consumption

7.1 Purpose

The power consumption is measured for different conditions.

7.2 Tests and Results

7.2.1 Quiescent Power TP2000

Objective The GTFE is powered in the quiescent state. The power is measured for different configuration.

Method Two GTFE64D chips on the test board were powered and reset (reset signal). The current draws of three power lines (DVDD, AVDD, AVDD2) were measured in the following configurations.

- clock on, chip address = 0, 23, DVDD is varied ± 300 mV, ± 200 mV, ± 100 mV
- clock on, chip address = 0, 23, AVDD is varied ± 300 mV, ± 200 mV, ± 100 mV
- clock on, chip address = 0, 23, AVDD2 is varied ± 300 mV, ± 200 mV, ± 100 mV,

where both the left and the right clock signals were turned off.

Results Figure 1 shows the observed current draws of the three (AVDD, AVDD2, DVDD) power lines for each voltage configuration.

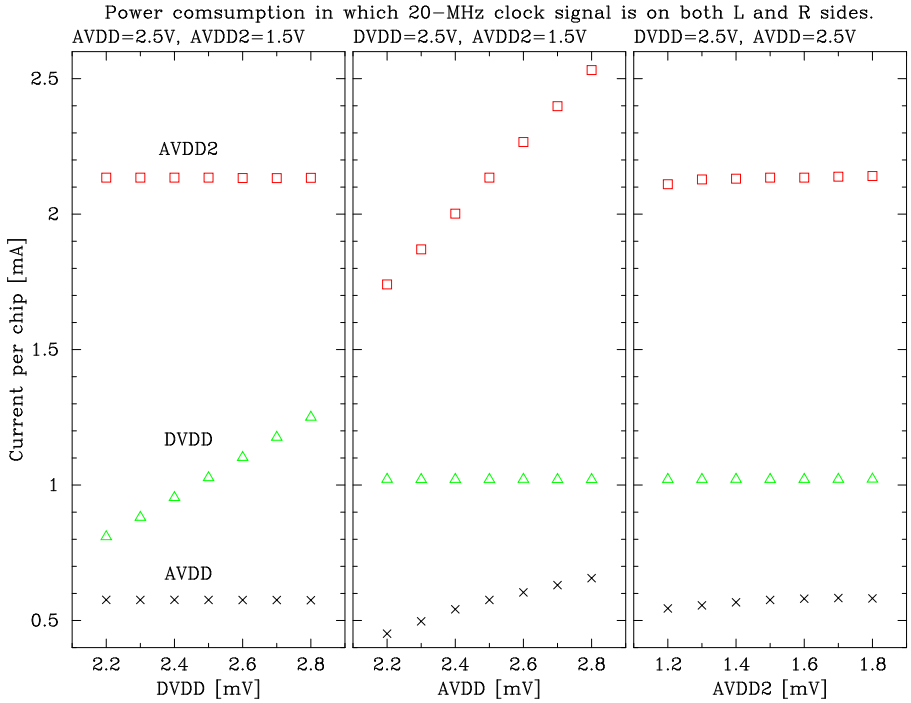

Figure 1: Change of current draw of AVDD, AVDD2, DVDD when the voltage is varied by ±100, ±200, ±300 mV from the nominal value.

7.2.2 Power during Readout TP2001

Objective The current increase due to the readout task is determined.

Method The current draw of the DVDD was measured when calibration strobe is issued repeatedly in a frequency from 0 to 20 kHz and the data stored in the event-buffer is read out. The measurements were performed on the test board in the following condition.

- Chip configuration:
  - All the termination resistors for LVDS drivers are removed or set at 10 kΩ.
  - Two chip-addresses were set at 0(00000) and 23(10111), or at 1(00001) and 22(10110). If resistances of all the series resistors used to set the chip address are same, the power consumed in these resistors should be kept between these two conditions. The current expected to be consumed in these resistors is 1 mA.
- Command operation:
  - 20-MHz clock signals were put into both of the left and the right clock lines, only the left, or none.
  - Both two chips on the test board were operated in the LEFT-mode. Thus, Command signals were put into the LEFT command decoder.
  - Calibration strobe signals were put to generate pseudo-events in a frequency of 0–20 kHz. The CAL-DAC and THR-DAC values were set at 62 (=4.5 fC) and 30 (=140 mV) respectively. The calibration mask registers were set to be 0101...01 from CH63 to CH0. Although such a hit pattern as 0101...01 should be impossible in a real operation, it was tested as the worst case.
  - At the time delayed by 2.5 us from each calibration strobe signal, a L1T signal was put into the trigger acknowledge. The data stored in the event buffer of each chip was read for each calibration-strobe signal. It was checked that the output data was agreed with the pattern of the calibration mask (0101...01).

Results Figure 2 shows the results of the measurements of the current increase against the calibration-event rate in various configurations.

7.2.3 Power at different clock frequencies TP2002

Objective The clock frequency is varied and the quiescent power is measured.

Method Clock signals in a frequency of 0–50 MHz were put into both of the left and the right clock lines and current draws of the three (AVDD, AVDD2, DVDD) powers line were measured.

Results Figure 3 shows the results of the measurements of the current increase against the clock frequency.

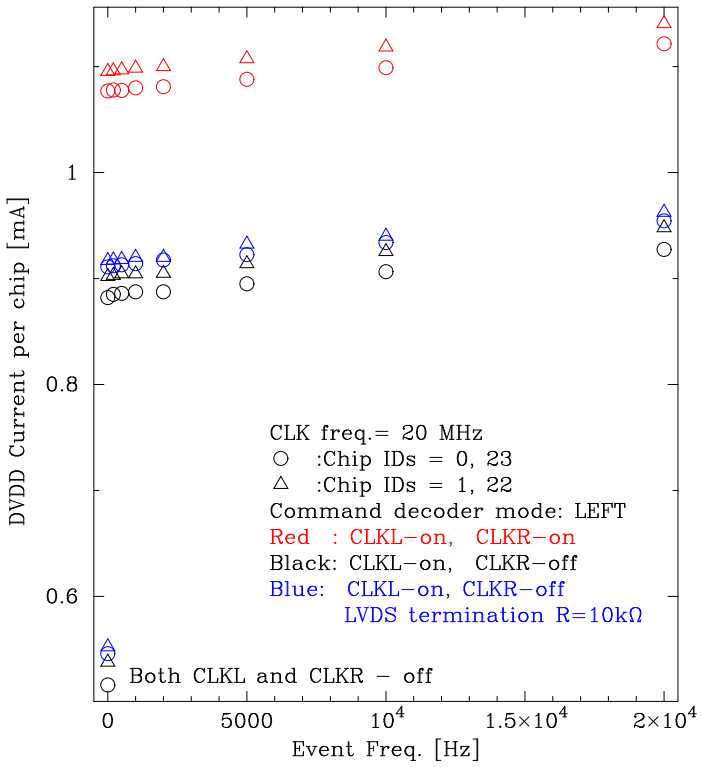

Figure 2: Current draws of DVDD when calibration strobe signals are issued in a frequency of 0–20 kHz.

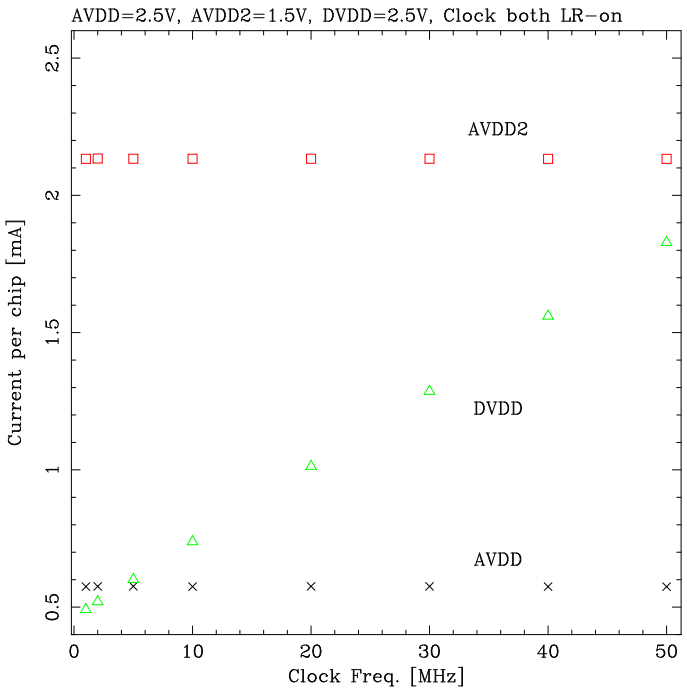

Figure 3: Current draws of the three power lines in a clock frequency from 0 to 50 MHz.

8 Receiver Testing

8.1 Purpose

The differential receivers for the clock, command and trigger acknowledge are tested. The receivers are tested with respect to the frequency of the input signal, the differential signal swing and the common mode shift. The setup is described in test 3000.

8.2 Tests and Results

8.2.1 Receiver Amplitude Sensitivity TP3000

Objective The amplitude range for which the receiver works properly is measured.

Method A pulse generator, LeCroy 9210, was used to generate test differential signals. The test signals were put into a receiver for CLKL in GTFE64D. The receiver output was pico probed on an internal test pad. The pico probe was connected to an oscilloscope to monitor the phase, rise/fall time of the signal and the duty cycle. The voltage swings of the differential signal were varied down to 10 mV with the pulse generator and attenuators. The tests were performed in 20 and 50 MHz clock signals with 50% duty cycle and 1000-mV common mode voltage.

Results Figure 4 shows pulse shapes of the input differential signals (CLKLP, CLKLP) and the receiver outputs observed by the oscilloscope in a clock frequency of 20 and 50 MHz and a differential voltage swing of 10, 20, and 50 mV. These pulse shapes in Figure 4 were averaged aver 300 samples using a function of the oscilloscope. The pulse heights indicated with the scale of the oscilloscope in Figure 4 are 1/20 of the real value because of the $\times 20$ pico probe. Also, the receiver is defined as its output signal goes high when the "plus" input signal (CLKLP) goes lower than the "minus" input signal (CLKLM).

In the case of the 20-MHz clock signal, any problem was not observed in the voltage swing down to 10 mV. On the other hand, in 50-MHz clock signal, a duty cycle of the receiver output shows significantly shorter than the input signal in the case of 10-mV voltage swing.

8.2.2 Receiver Frequency Response TP3001

Objective The frequency response is measured.

Method The input frequency was varied between 10-50 MHz. The ratio between pulses at the input and at the output of the receiver was measured.

Results It was found from the results of test TP3000 that the receiver response is good enough in a clock frequency up to 50 MHz as long as the differential voltage swing is higher than 20 mV.

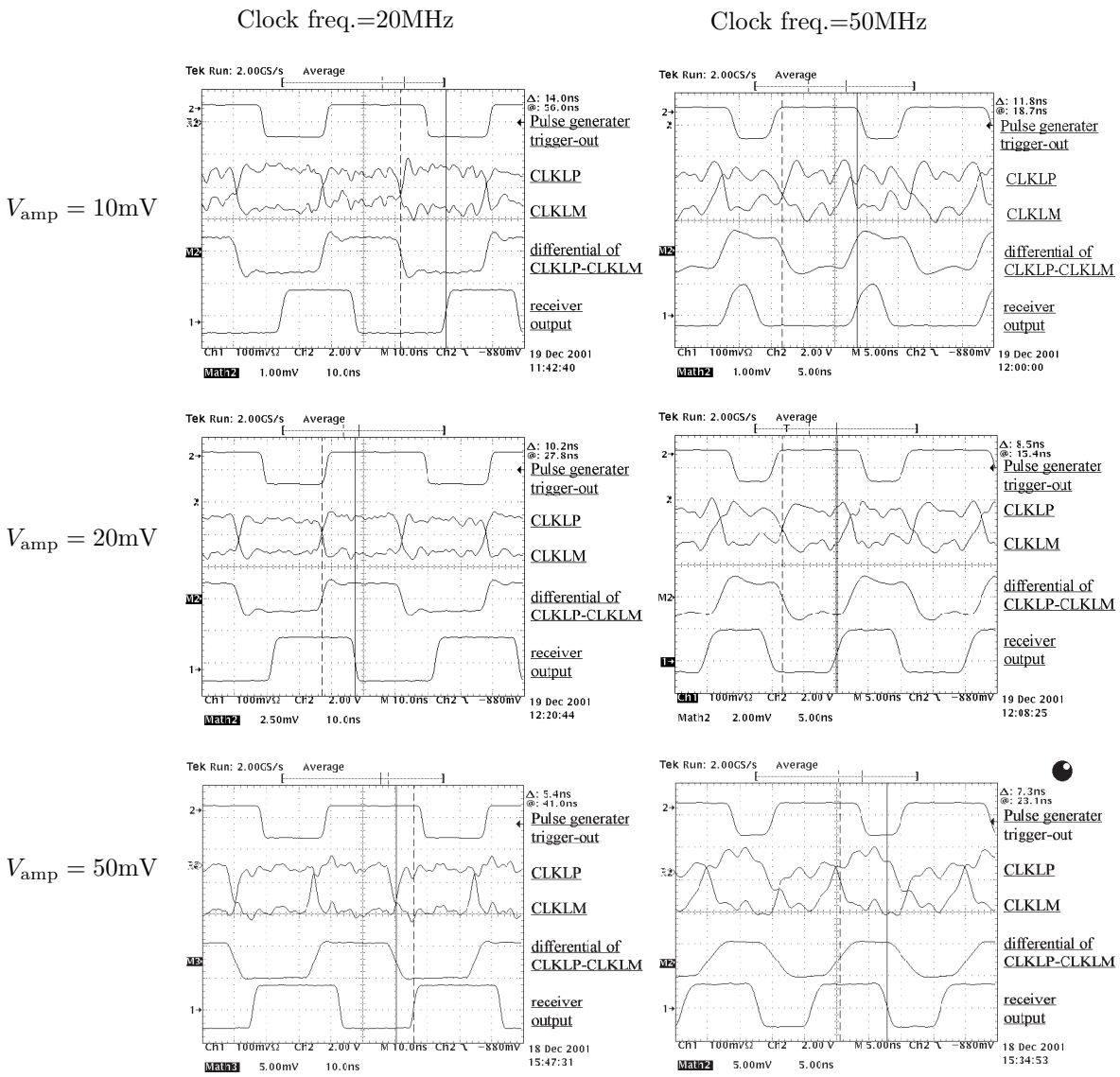

Figure 4: Pulse shapes of the input differential signals (CLKLP, CLKLP) and the output of the receiver in a clock frequency of 20 and 50 MHz and a differential voltage swing, $V_{\rm amp}$, of 10, 20, and 50 mV.

8.2.3 Receiver Common Mode Sensitivity TP3002

Objective The common mode of the differential input signal is varied and the receiver response is measured.

Method Same setup as for test 3000. The common mode of the differential signal was varied (between GND+amplitude and DVDD−amplitude) and the receiver output was monitored by an oscilloscope. The experiment was performed with 20 and 40 MHz clock signals with a nominal voltage swing of 100-mV amplitude.

Results Figure 5 shows the observed receiver responses for differential signals with various common mode voltages, V_{base}, in a clock frequency of (a) 20 MHz and (b) 40 MHz. It was obvious from Figure 5 that the common mode sensitivity has a dependence on the clock frequency.

8.2.4 Propagation Delay TP3003

Objective The time delay between the input and output of the receiver is determined.

Method Same setup as for test 3000 (also 3002).

Results It was found from the results of test 3000 and test 3002 that the propagation delay depends on the amplitude and the common mode voltage of the input differential signal. In the case of the nominal signal of the 100-mV amplitude and the 1000-mV common mode voltage, it is derived to be $\simeq$5 ns from Figure 5.

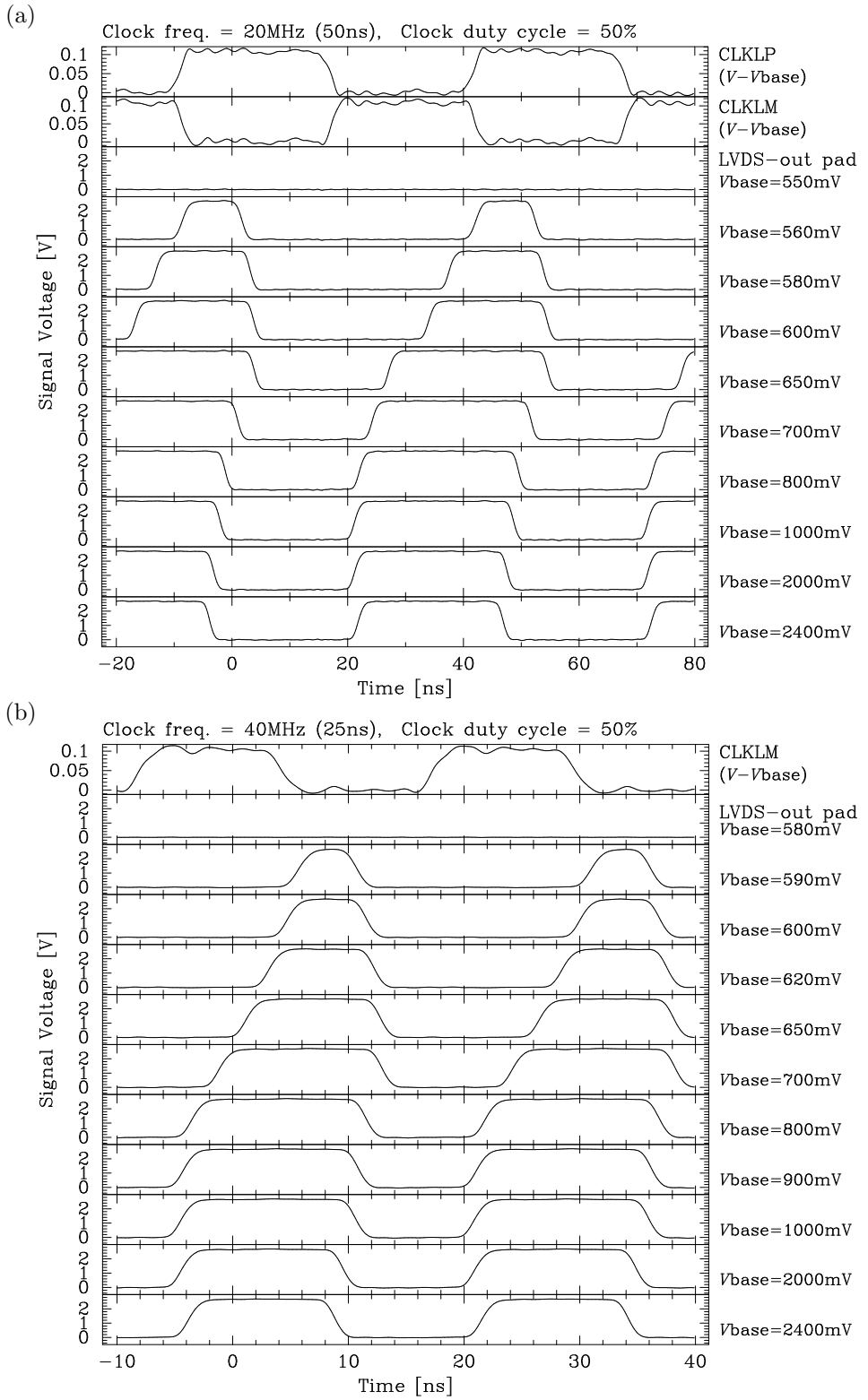

Figure 5: Receiver responses for differential signals with various common mode voltages, $V_{\rm base}$, in a clock frequency of (a) 20 MHz and (b) 40 MHz .