

RECOMMENDATION OF GTFE CHIP SIZE AND PAD LAYOUT

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Final tracker dimensions and assembly considerations lead toward an optimum front-end chip size of 13.9 x 2.4 mm. This is a 20% increase in chip length from the BTEM chip (11.65 x 2.4 mm). The chip can have 120 x 250 μm pads for wire bonding with 210 μm pitch. This is a significant improvement in the amount of metal available for angled wire bonds and re-bonding.

Method:

- 1) HDI final size was calculated from 8.95cm. detector size, 0.2 mm gaps between detectors, and otherwise the same tray dimensions as the BTEM. Size = 360.2 mm.
- 2) Spaces between chips and on the ends of the board were calculated based on IPC standards for trace spacing and clearances for Kullick & Soffa deep access wire bonders. Also a minimum gap of 0.5 mm between chips was used. (BTEM)
- 3) Chips were distributed evenly in the remaining space.
- 4) Pads were distributed on chips with the same spacing between pads and distance from last pad to diced edge as the BTEM GTFE64C.

Spacing Requirements:

- 1) IPC requirements
 - Minimum space between low voltage traces: **0.1 mm** (IPC-2221, p. 39)
 - Minimum space around 151-170 volt trace: **0.4 mm** (IPC-2221, p. 39)
 - Space between board edge and first trace: **0.5 mm** (IPC-2221, p. 20)
- 2) Deep access wire bonder clearances
 - K&S 1478, 60 deg: X clearance = **26 mils (0.65 mm)** (my calculation)¹
Y clearance = **30 mils (0.75 mm)** (from manual)²
 - K&S 8090, 60 deg: X clearance = **26 mils (0.65 mm)** (my calculation)
Y clearance = **40 mils (1.0 mm)** (from manual)
- 3) Wire bond minimum length: **1.5 mm**

Minimum spaces: There are 3 type of spaces needed between chips on the hybrid.

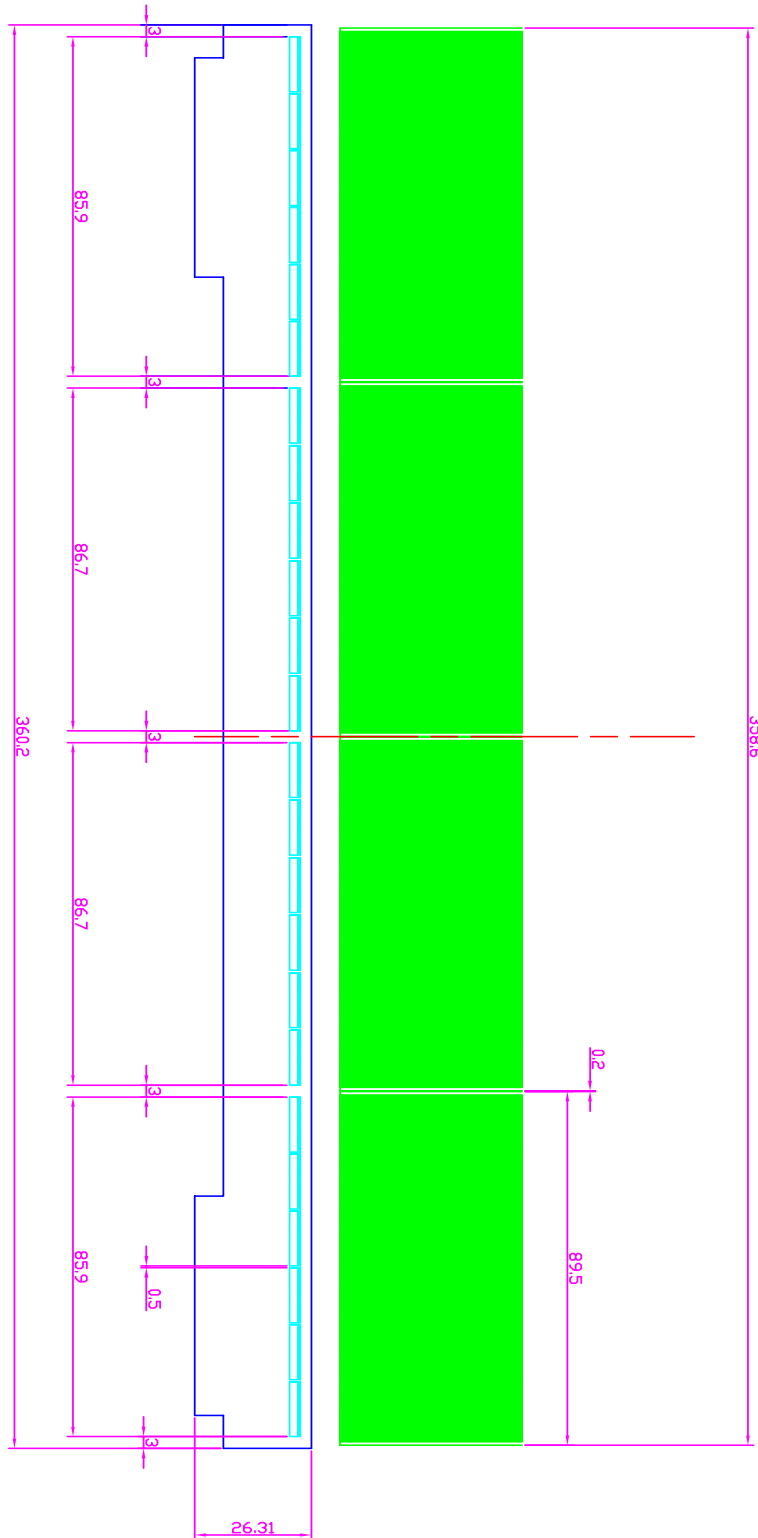
- 1) Between last chip and end of board for wire bonding (2 times)
- 2) Between 2 chips for bias traces running to Kapton interconnect (3 times)
- 3) Between remaining chips for epoxy squeeze out and ease of assembly (20 times)³

¹ This number should be checked.

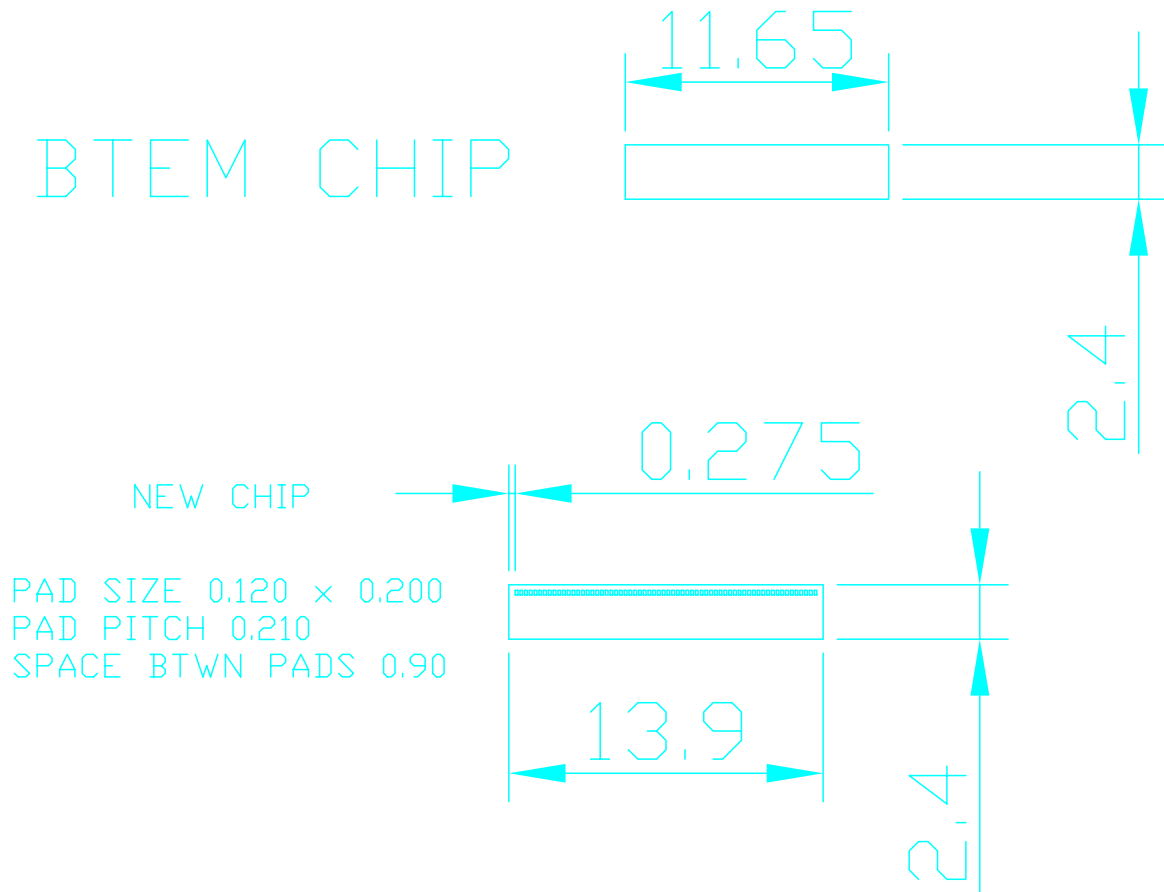
² Y clearance affects the dimensions and placement of the Right Angle Interconnect and requires that the chip to chip wire-bonds are moved to the lower half of the chip. This report assumes that the chip to chip bonds are compressed to 100 μm pitch.

³ The final layout has 2 different gaps between chips because the chip size is limited by the sets of chips between the edge of the board and the first bias traces. Thus, the chips in the center of the board have larger gaps.

HYBRID DRAWING WITH CHIPS: detectors are in green



CHIP DRAWING:



PAD LAYOUT:

- We measured the BTEM GTFE64C chip and determined that 275 microns was a good space between the last bonding pad and the diced edge (more than maximum measured).
- The 90 microns between pads is the same as the BTEM GTFE64C.
- A 250 micron deep bonding pad gives comfortable re-bonding space.

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