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Electrical Test of HP 0.5- μm Test Chip for Front-end Electronics for GLAST Tracker

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Abstract

The front-end electronics chips used to build the GLAST BTEM (Beam-Test Engineering Model) Tracker, GTFE64c chips and GTRC chips, were manufactured with the HP 0.8- μm process, which has already been shutdown and is no longer available. Electronics in the next generation, including ones for flight model, should be manufactured in other process, such as the HP 0.5- μm process. A test chip was newly designed for the HP 0.5- μm process to check its functionality and performance. Twenty-five chips were manufactured with the design and one of them was electrically tested in a test setup at UCSC/SCIPP. In this report, results from the electrical tests and measurements of the test chip (second version) after a brief description of the chip and the setup.

1. Test Chip, PC Board, and Test Setup

The test chip includes six channels of analog circuits identical to the one in GTFE64c; a charge-sensitive preamplifier, a shaping amplifier, and a comparator. Each of the channels is designed with slightly different design parameters and techniques; especially linear capacitors are used in three channels, while non-linear capacitors (in which capacitance changes with voltage across) are used in the other three as well as in GTFE64c. Below, the channels with linear capacitors are designated as 12C1, 12C2, and 12C3 and the ones with non-linear capacitors as 12IN1, 12IN2, and 12IN3 for historical reasons. The chip tested here is the second version, since the first version has a problem that makes it impossible to

perform reliable tests. It also includes three isolated transistors, but these are not tested this time.

A PC board, Liz board III, was designed and fabricated for tests of the test chip. One test chip can be mounted at the center of the board with passive components, such as load capacitors and bypass capacitors around it. An attenuation/termination circuit for each channel is on the board. It also can carry output LVDS driver chips for digital readout. Three power lines are needed to run a chip; two for analog circuit in the chip (+3.3 V for AVDD and +1.5 V for AVDD2) and one for digital (+3.3 V for DVDD). Internal layers supplying power are improved for noise measurements since Liz board II.

A pulse generator (LeCroy 9210 and 9211) was used to inject charges through an

internal or an external capacitor. Rising slope of charge injection pulse was 30 ns for all measurements in this report. Output pulse height was controlled within an accuracy of 2 percent in the range used in the measurements in this report. A picoprobe (GGB Industries, Inc., Model 12C) and a 500-MHz digital oscilloscope (Tektronics TDS 540) was used to probe preamplifier output, shaper output, and comparator output (after its output driver). A NIM crate and a few NIM modules (a level converter module, a gate generator module, and a scaler module) are used for noise measurements.

2. Pulse Shapes

Pulse shapes of preamplifier output and shaper output were snapshot with and without a 45-pF load-capacitor on input of each channel (Fig. 1). These are for about 3 fC injection onto a channel. Spiky structure at the leading edge of preamplifier outputs is confirmed to be a pick-up noise, picked up by a probe tip from charge injecting cable.

Pulse shapes are identical between three channels with the same type of internal capacitors. Channels with linear capacitors (12C1, 12C2, and 12C3) show slightly slower falling slope in shaper output than the ones with non-linear capacitors (12IN1, 12IN2, and 12IN3). Also, pulse height of shaper output on the former is lower than that on the latter. With a 45-pF load, shaper output becomes slightly wider in pulse width and smaller in pulse height.

3. Amplifier Gain

Gains were measured on all channels by measuring pulse height of preamplifier output and that of shaper output with a digital oscilloscope at charge injection ranging from 1 fC to 5 fC. The gain measurements were done without a load capacitor, with an 18-pF load, and with a 45-pF load (Fig. 2). Gains and voltage offsets in preamplifier output and shaper output were estimated by straight-line fits to the pulse heights measured, and are listed in a table below.

	Preamplifier					
	No load capacitor		18-pF load		45-pF load	
	Gain (mV/fC)	Offset (mV)	Gain (mV/fC)	Offset (mV)	Gain (mV/fC)	Offset (mV)
12IN1	5.32	-0.08	5.70	0.14	5.24	+0.52
12IN2	5.58	+0.10	5.48	0.16	5.20	+0.04
12IN3	5.62	+0.38	5.60	-0.04	5.18	-0.18
12C1	4.76	+0.04	5.18	-0.02	4.88	-0.04
12C2	5.04	+0.16	5.33	-0.21	5.08	-0.24
12C3	5.24	+0.04	5.28	-0.28	4.78	+0.26

50 fF is assumed for an internal capacitor on test input for gain calculation.

	Shaping Amplifier					
	No load capacitor		18-pF load		45-pF load	
	Gain (mV/fC)	Offset (mV)	Gain (mV/fC)	Offset (mV)	Gain (mV/fC)	Offset (mV)
12IN1	152	-47	144	-49	126	-49
12IN2	136	-37	146	-59	131	-54
12IN3	147	-53	140	-50	121	-48
12C1	123	-45	127	-52	113	-45
12C2	119	-43	136	-59	122	-55
12C3	137	-63	133	-61	118	-56

50 fF is assumed for an internal capacitor on test input for gain calculation.

	Noise Measurement			
	Equivalent noise charge		Capacitance-dependence	
	18-pF load (electron)	45-pF load (electron)	Slope (electron/pF)	Offset (electron)
12IN1	549	1164	22.8	139
12IN2	600	1199	22.2	201
12IN3	519	1114	22.0	122
12C1	477	977	18.5	144
12C2	519	1081	20.8	144
12C3	486	1019	19.7	131

50 fF is assumed for an internal capacitor on test input for noise calculation.

4. Electrical Noise

Noise on all the six channels were measured by charge-injection scans with threshold voltage fixed to about 165 mV (nominal threshold voltage for operation), with 18-pF load and with 45-pF load. Amount of charges injected on a channel was scanned from about 1.0 fC to about 2.5 fC with 0.025-fC increment for 18-pF load and with 0.05-fC increment for 45-pF load. At each charge amount, 1000 charge-injecting pulses were issued and the number of pulses on comparator output was counted (Fig. 3). By fitting a scan curve, i.e., the number of outputs versus charge injection, with an error function, equivalent noise charge was calculated for all the six channels with 18- and 45-pF load. Connecting two noise values, one at 18-pF load and another at 45-pF load, noise slope (capacitance-dependence of noise) and noise offset (noise with no load capacitance). Results are listed in the table above.

5. FastOR Timing

Leading edge of Comparator output signal, or FastOR signal, rises a couple of hundred nano-seconds after shaper output exceeds threshold voltage (Fig. 4). The delay is due to slow response of the comparator circuit. With 5-fC injection (about a MIP) and threshold voltage at 165 mV (nominal operation voltage), the time between leading edge of charge-injecting pulse and that of comparator output after the output driver (Δt in the figure) were monitored over 500 charge injections, and its maximum and minimum were measured. Results are in the

table below. The measurements were with 45-pF load capacitors. Results shown in the table is in good agreement with those from SPICE simulation, or about 450-ns delay.

	FastOR delay (Δt)	
	Minimum (ns)	Maximum (ns)
12IN1	550	678
12IN2	564	696
12IN3	534	672
12C1	552	688
12C2	544	668
12C3	546	688

SPICE simulation predicts 450 ns.

6. Large Signal Response

Electronics' response for large signal ranging from 100 fC to 900 fC was investigated with an external charge-injecting capacitor of 45-pF attached to each channel. The charge-injecting capacitor also acts as a load capacitor to the channel input (see the circuit diagram of Liz board III attached to this report). The charge-injecting pulse from the pulse generator was attenuated by a factor of 20, instead of 10 as in the circuit diagram. Snapshots of preamplifier outputs and shaper outputs are shown below (Fig. 5).

Pulse height of preamplifier output and pulse width of comparator output after the output driver, or ToT (Time-over-Threshold) were measured for injected charges of 100 fC to 900 fC and plotted in the figure below (Fig. 6). From the plot, one can see both of preamplifier pulse height and ToT saturate above 300-fC injection.

Injection of larger amount of charge was tried upto 9000 fC, but ToT stayed the value at the saturation, while preamplifier output became wider and wider with the amount of charge.

There is significant difference in ToT behavior against amount of injected charge between channels with and without linear capacitors in the circuit; the upper branch in the ToT plot is for linear-capacitor channels and the lower for non-linear ones. On the other hand, no difference is seen in preamplifier output.

Even before the saturation, both of preamplifier pulse height and ToT leaves linear dependency on charge. Note that ToT loses linear dependency on amount of injected charge before pulse height of preamplifier does. The reason for this phenomenon is not know yet.

7. Capacitance of Charge-injecting capacitor on Test Input

Pulse height of preamplifier were measured with charges injected both through test input of the test chip (about 50 fF) and through an external capacitor (about 45 pF). Comparing preamplifier gains obtained from charge injection through test input with those through the external capacitors, capacitance of charge-injecting capacitors on test inputs of the chip. The plots below show pulse height versus injected charge with 50 fF (test input) and 45 pF (external) assumed, respectively. (Fig. 7) Assuming external capacitor is exactly 45 pF, ratio of two gain slopes gives us a factor for test-input capacitance to multiply 50 fF. Results are listed in the table below.

	FastOR delay (Δt)	
	Ratio of Gain Slopes	Test-input Capacitance (fF)
12IN1	0.939	47.0
12IN2	0.945	47.2
12IN3	0.985	49.2
12C1	0.944	47.2
12C2	0.934	46.7
12C3	0.900	45.0

8. Recovery Time after Large Signal

If a large signal is input to a channel such that the preamplifier saturates, the channel will be dead after the large signal for a while. Injecting 5 fC signal through a test input of the chip after a large signal through an external capacitor connecting channel input, single channel recovery time was investigated on two channels, 12IN2 and 12C2. Control parameters here are the amount of injected charge of a large signal and time between two signals.

Pulse shapes of shaper output for 5 fC signal are plotted for a couple of signal intervals (Fig. 8). One can see pulse height and pulse width grows with signal interval. As a measure of channel's recovery, pulse heights of shaper out were measured against various signal intervals for large signals of 112 fC, 450 fC, and 1800 fC (Fig. 9). Let us define recovery time to be the signal interval that gives 50 percent pulse height in shaper output, then recovery times are found as in the table below.

Size of the preceding large signal	Approximate 50 % recovery time	
	12IN2	12C2
112 fC	< 60 μ s	< 60 μ s
450 fC	700 μ s	500 μ s
1800 fC	3.5 ms	4.0 ms

Threshold voltage was 164 mV.

The recovery time has a strong correlation to preamplifier saturation (see left panel in Fig. 5). Arrows in the plots corresponds the recovery time listed in the table above. One can see the recovery times correspond to recovery of preamplifier from its saturation.

Note that the recovery time defined here is a single channel dead time, not a system dead time. Even if a single channel is dead for a couple of milli-seconds, all other channels can issues a FastOR signal to trigger the system at 100 μ s after the large signal. This is because a comparator output of the channel becomes to logical zero after 100 μ s after a signal, no matter how big the signal is.

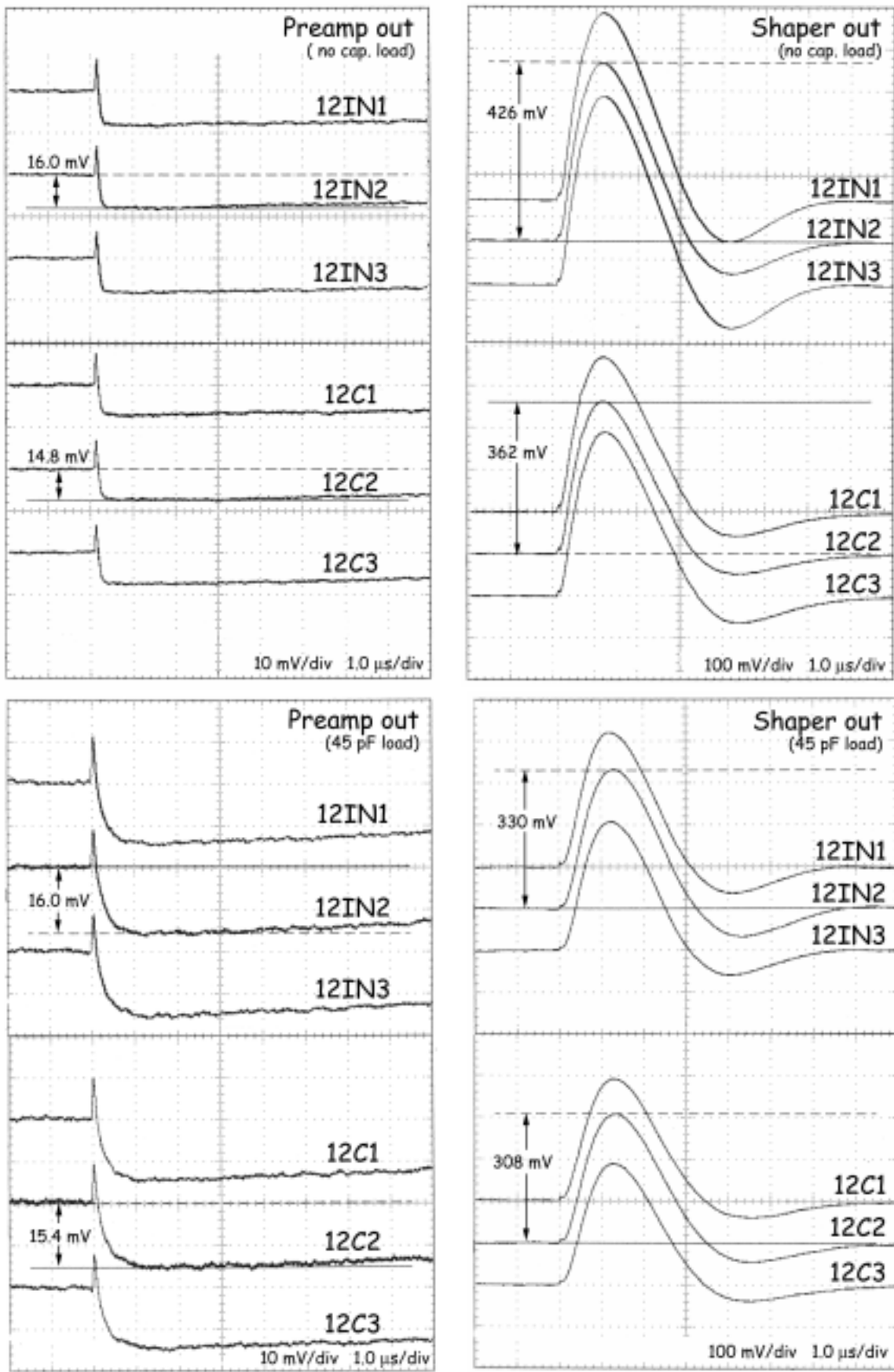


Figure 1. Pulse shapes of preamplifier output and shaping amplifier output of all the six channels with and without a 45-pF load capacitor on channel input.

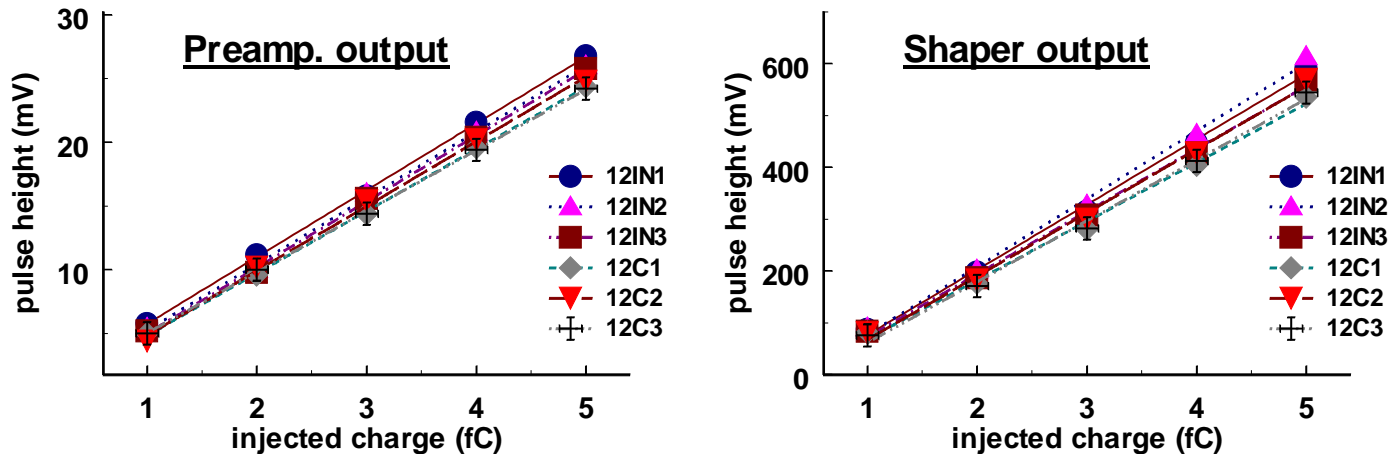


Figure 2. Measurements of gains and offsets of preamplifier and shaping amplifier with 45 pF of load capacitor. Charge-injecting capacitor on test input is assumed to be 50 fC.

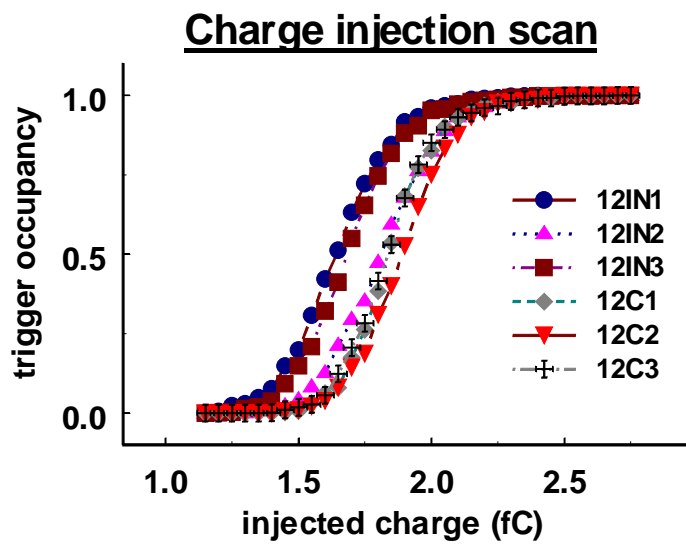


Figure 3. Charge-injection scan with 45 pF of load capacitor at threshold of 165 mV. Charge-injecting capacitor on test input is assumed to be 50 fC.

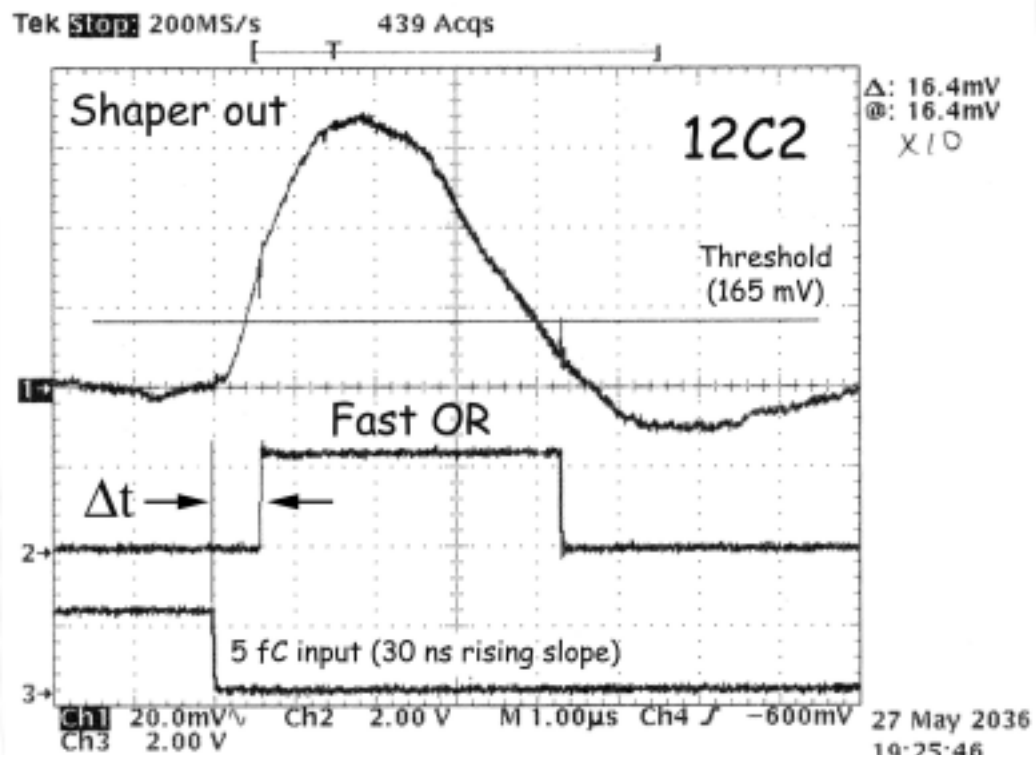


Figure 4. Definition of FastOR delay, Δt , in comparison with pulse shape of shaper output. A solid horizontal line shows threshold level of a comparator and spikes on shaper output corresponds to a rising and falling edge of FastOR signal. One can see FastOR signal is delayed by about 200 ns. The delay is due to slow response of comparator.

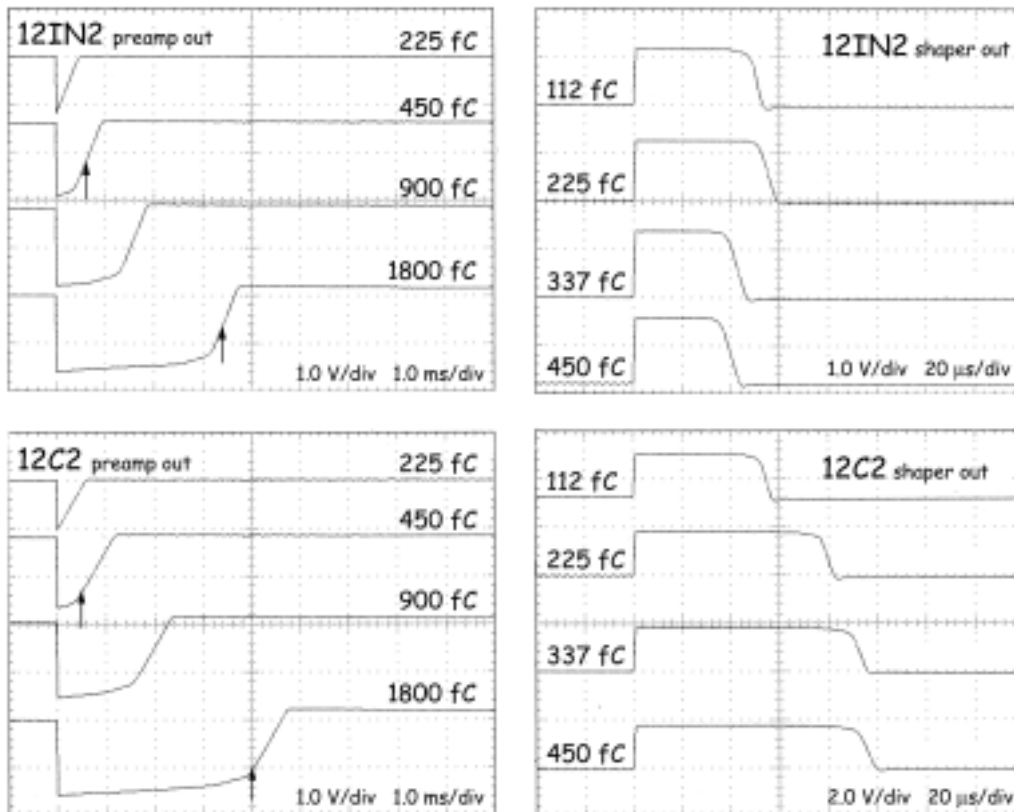


Figure 5. Pulse shapes of preamplifier output and shaping amplifier output for large signals over 100 fC. Not only pulse height of both amplifiers but also pulse width of shaper output saturates in this range of signal size, while pulse width of preamplifier output grows with signal size. Arrows in the left panel indicates recovery time defined in the later section (see text for details).

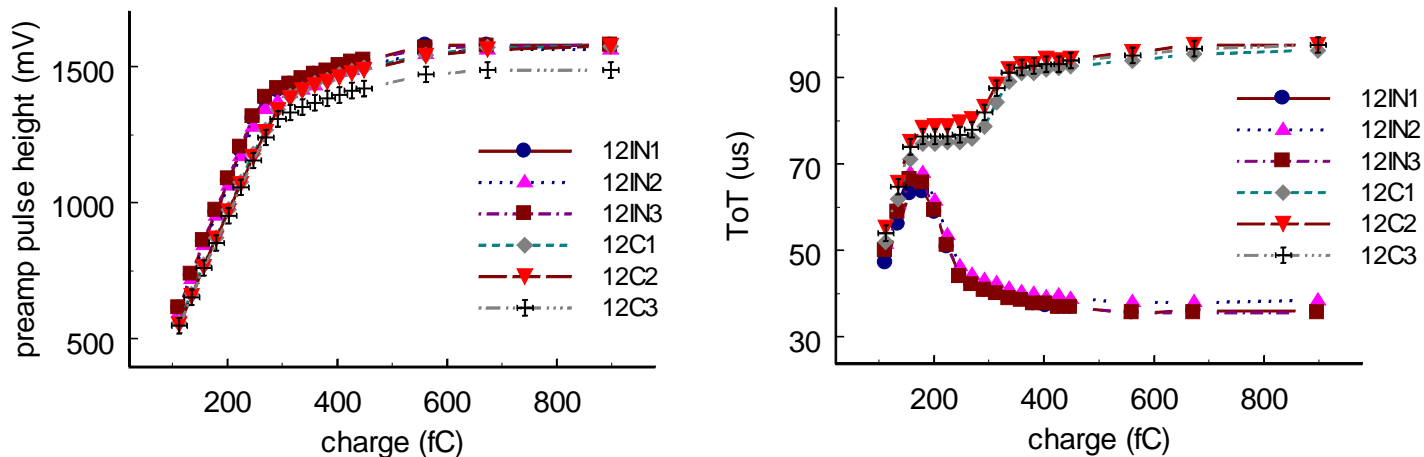


Figure 6. Pulse heights of preamplifier output and pulse width of FastOR signal (ToT, or Time-over-Threshold) for a large signal.

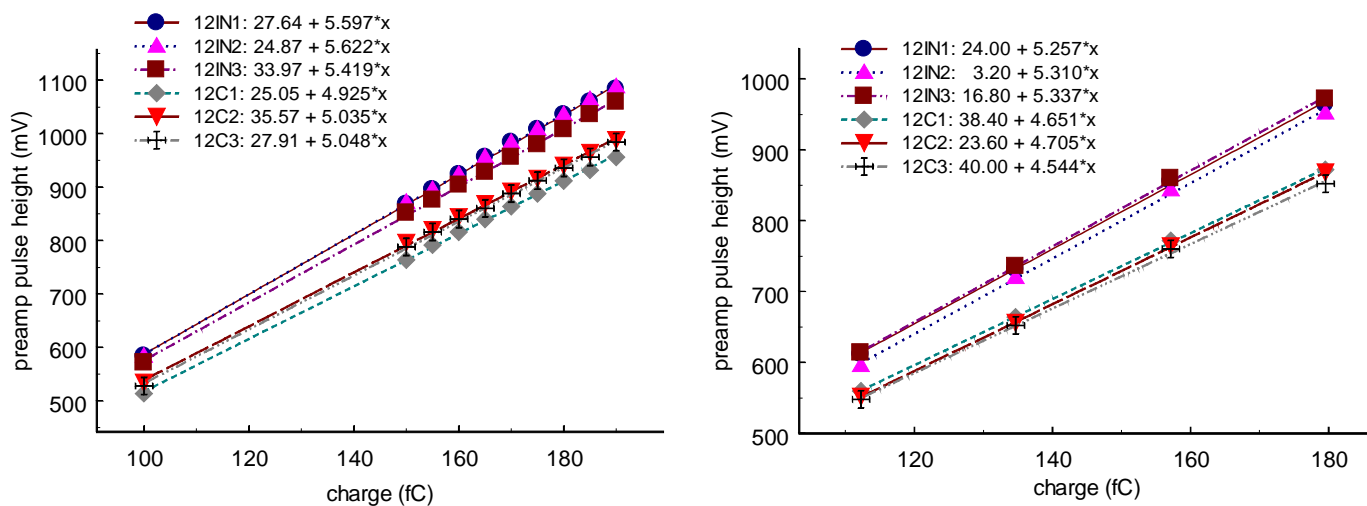


Figure 7. Straight-line fits to pulse heights of preamplifier output to calculate capacitance of internal capacitor on test input. Charges were injected through test input (left panel) or through an external capacitor (right panel). For horizontal axes of both plots, 50 fF (test input) and 45 pF (external) are assumed, respectively. Ratios of two slopes of a channel give a factor to multiply to 50 fF to obtain the capacitance.

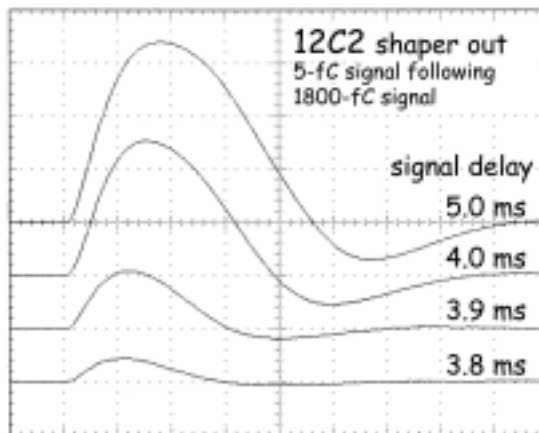
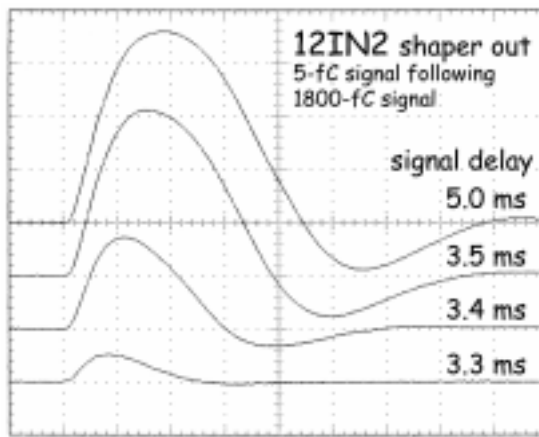


Figure 8. Pulse shapes of shaper output for 5 fC signal following 1800 fC signal with various signal intervals. The large signal is injected through an external capacitor (45 pF) and the 5 fC signal through internal capacitor on test input (50 fF).

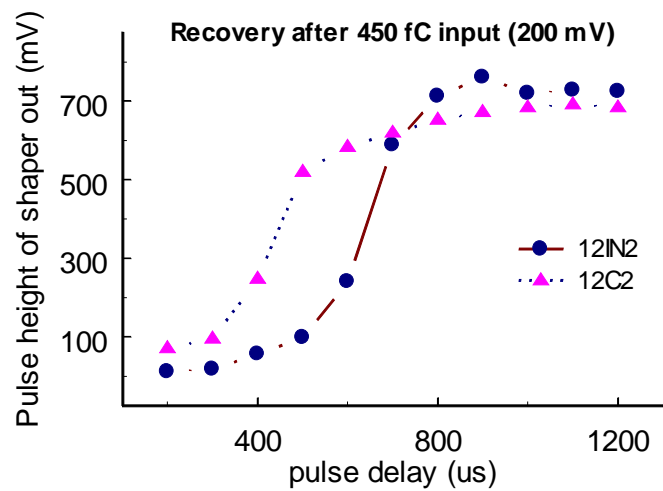
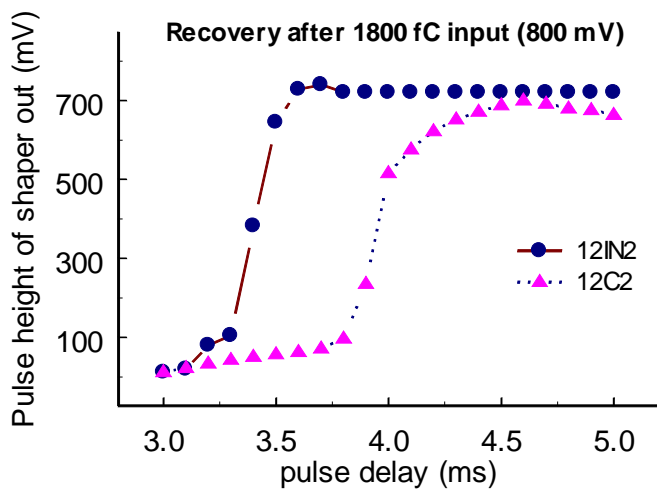
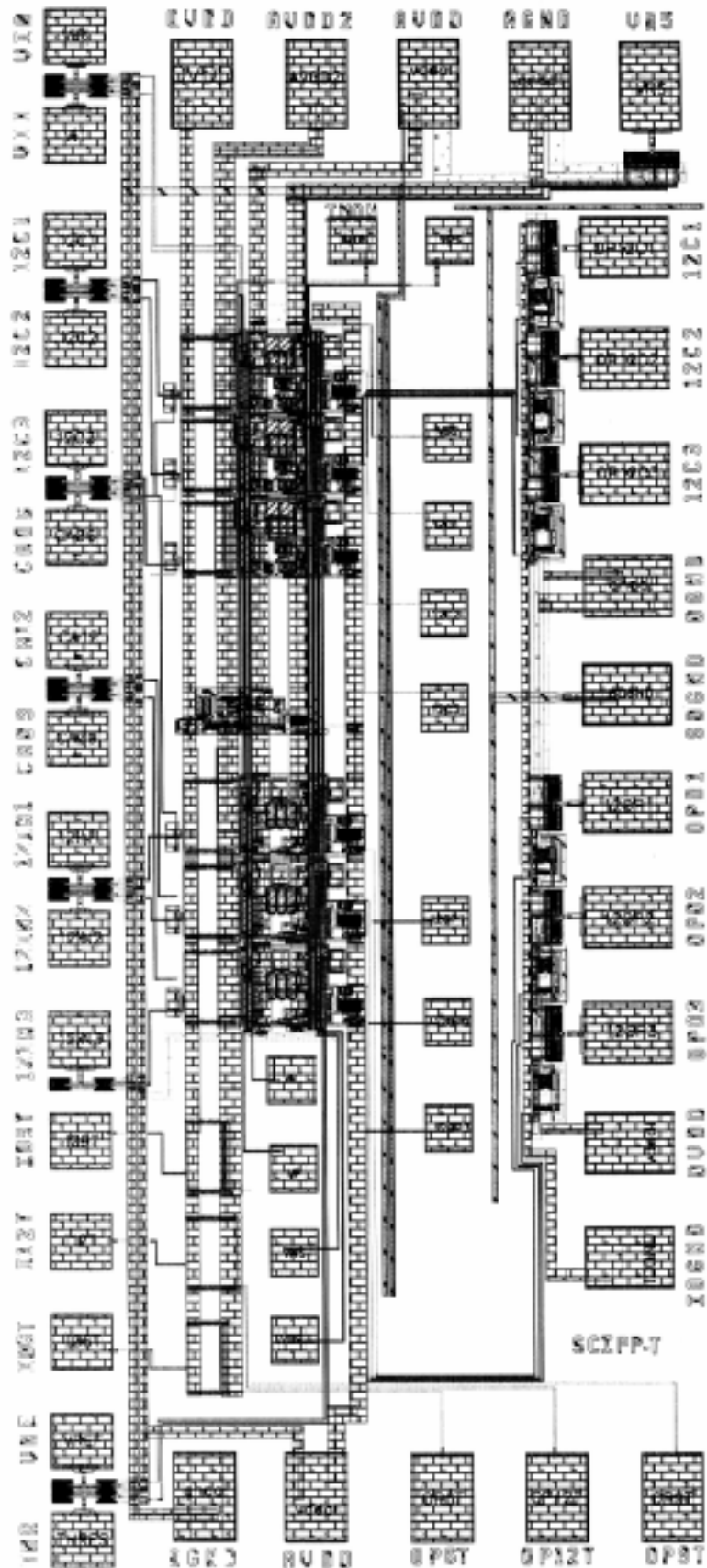
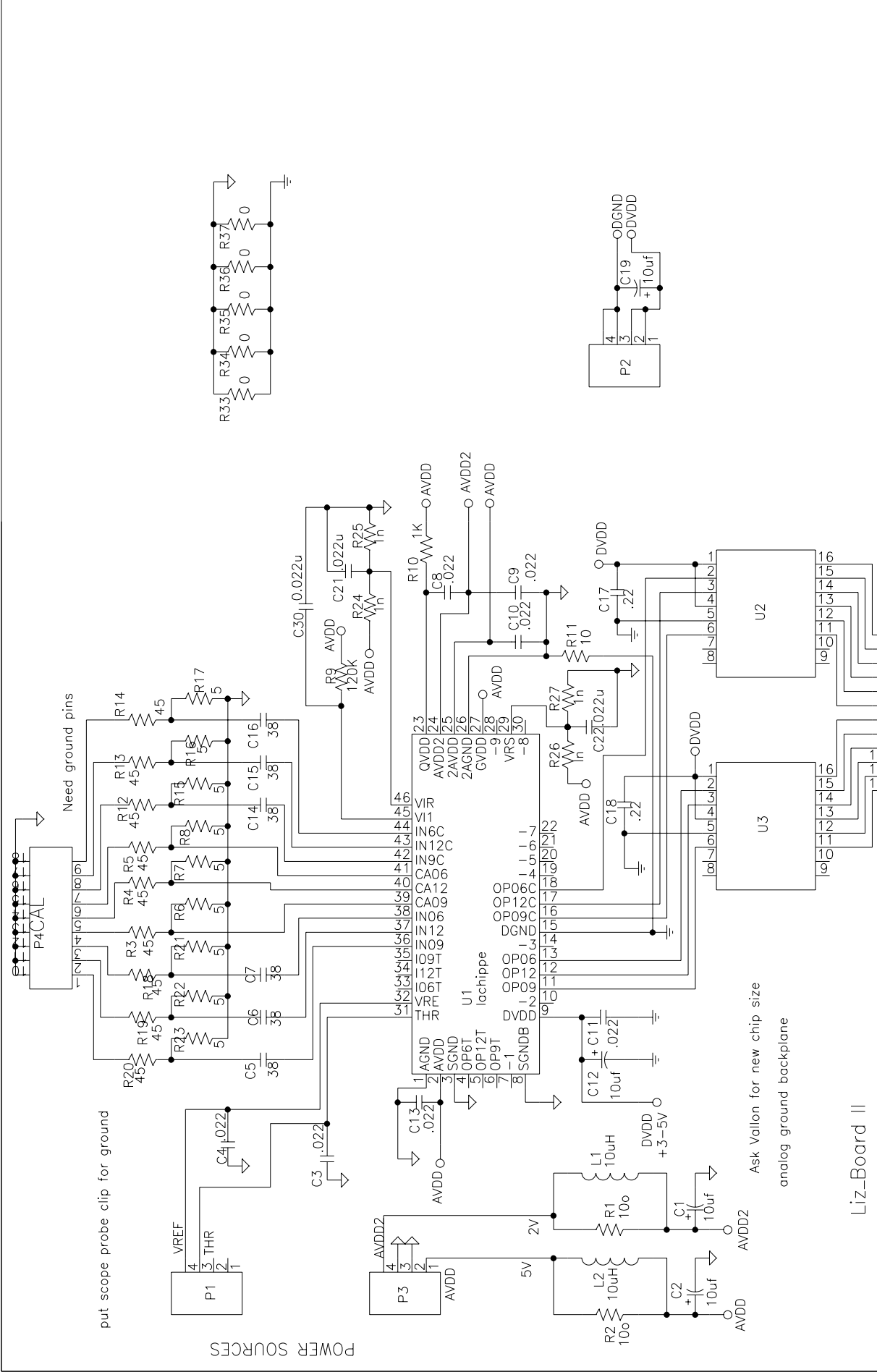


Figure 9. Pulse heights of shaper output for 5 fC signal following 1800 fC signal with various signal intervals. The large signal is injected through an external capacitor (45 pF) and the 5 fC signal through internal capacitor on test input (50 fF).

HP half-micron test chip for GLAST Tracker (version 2)





put scope probe clip for ground

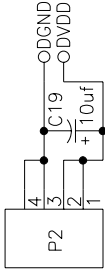
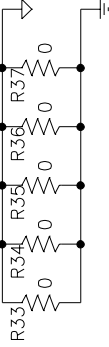
POWER SOURCES

Need ground pins

Ask Vallon for new chip size
analog ground backplane

Liz_Board II

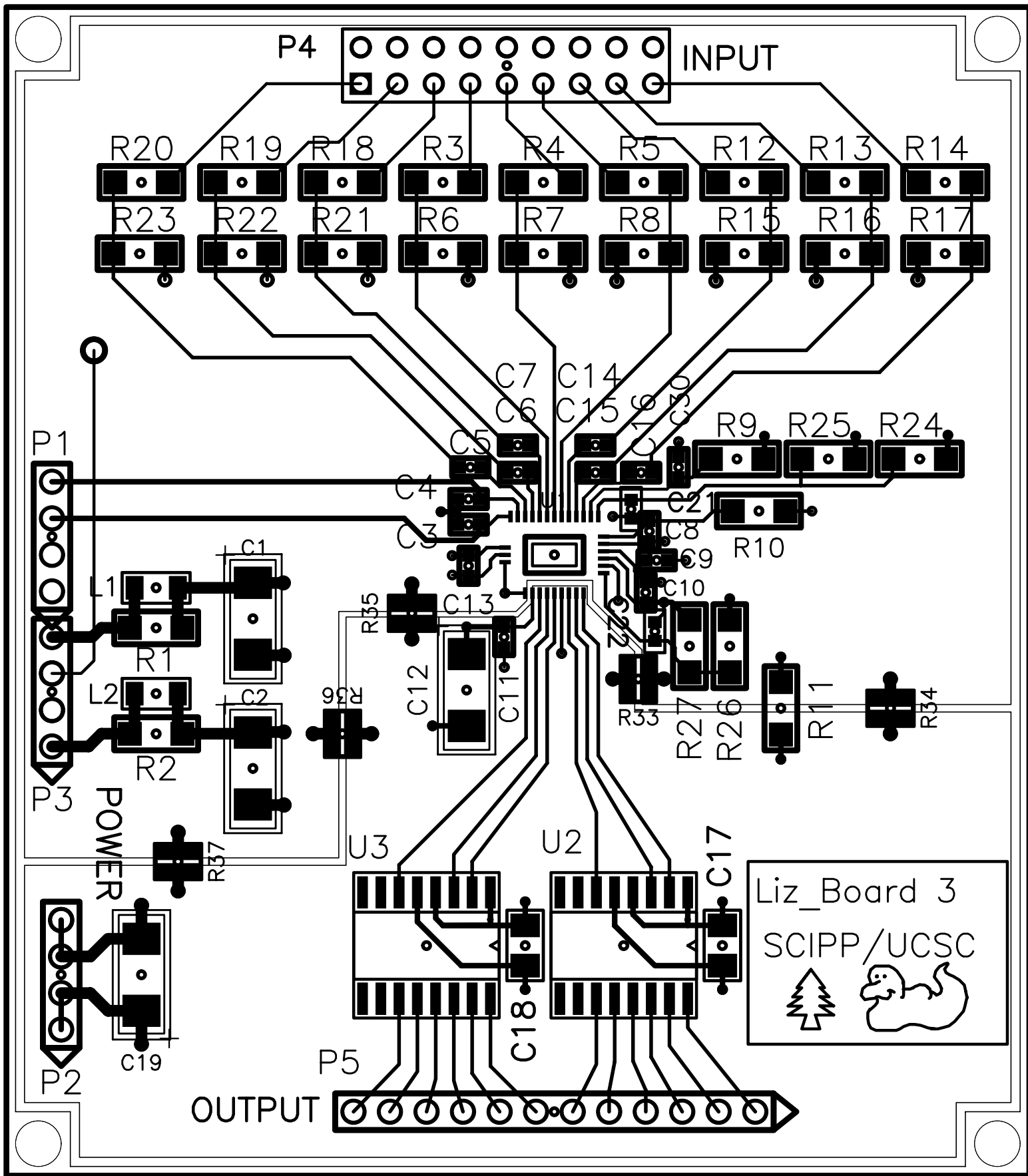
Liz Atwood



SCIPP/UCSC
1156 High St.
Santa Cruz, CA 95060
831-459-2694

Part List of Liz board III

Item	Count	Mfg ID	Attributes	RefDes
1	3	4-PLUG	4-plug	P1, P2, P3
2	1	9-PLUG	9-PLUG_2ROWS	P4
3	1	12-PLUG	12-plug	P5
4	2	C	C1005 .022u	C21, C22
5	1	C	C0603 0.022u	C30
6	2	C	C3216 .22	C17, C18
7	6	C	C0603 38	C5, C6, C7, C14, C15, C16
8	7	C	C0603 .022	C3, C4, C8, C9, C10, C11, C13
9	4	C_POLARIZED	TC6032 10uf	C1, C2, C12, C19
10	2	DS90LV047A	SOP16	U2, U3
11	2	L	L3216C 10uH	L1, L2
12	1	lachippe	lachippe_new	U1
13	1	R	R1206 120K	R9
14	9	R	R1206 5	R6, R7, R8, R15, R16, R17, R21, R22, R23
15	1	R	R1206 10	R11
16	3	R	R1206 1n	R24, R25, R27
17	1	R	R1206 In	R26
18	5	R	BRDG40x120 0	R33, R34, R35, R36, R37
19	9	R	R1206 45	R3, R4, R5, R12, R13, R14, R18, R19, R20
20	1	R	R1206 1K	R10
21	2	R	R1206 10o	R1, R2



Bonding Diagram of HP half-micron test chip version 2 on Liz board III

