Front-End Readout Chips

The silicon strip detectors must be read out by VLSI amplifier chips placed as close as is practical to the detector strips. A 64-channel CMOS amplifier-discriminator chip is currently being designed by the UCSC group to meet the GLAST requirements. Five such chips will be needed to read out each ladder of five detectors, or 25 chips per detector plane. The readout chips contain a significant amount of digital electronics, as well as amplifiers and comparators, in order to satisfy the data acquisition requirements.

Specifications

The readout chips must satisfy the following set of requirements:

1. Power less than 300 μW/channel, including amplifiers and digital readout.

2. Total noise less than about 1600 electrons equivalent charge. Noise occupancy less than $5 \cdot 10^{-4}$. Commensurate threshold uniformity from channel to channel.

3. Peaking time of amplifier output no longer than about 1 to 2 μs.

4. Self triggering.

5. Radiation hard to about 10 kRad.

6. Sufficient event buffering and readout speed to keep deadtime less than 1% at a trigger rate of 10 kHz. Must be able to acquire data while reading out previous events, which in turn requires that all digital signal transmission be designed not to induce noise into the sensitive amplifiers.

7. Sparse readout and data formatting as close to the front end as practical.

8. Sufficient redundancy in the digital readout to avoid catastrophic single-point failures.

9. Channel size to match the 194 μm detector pitch.

10. All control and data transfer via serial digital lines, in order to minimize cabling and avoid transfer of analog signals.

Design and Layout Status

Two prototypes of the analog section of the readout chip have been fabricated and tested on the bench and in a beam at SLAC and have been found to meet the GLAST power and noise requirements. Each analog channel includes a charge-sensitive preamp with a low input impedance (≈5 kΩ) and a continuous reset current coupled to an RC/CR shaping amplifier with an integration time of about 1 μs and a DC stabilized output. The shaper output goes into a comparator with an adjustable threshold.

The full-scale readout chip requires much more digital circuitry than those prototypes. The design currently in progress incorporates the following new features:

- Internal DACs for setting the threshold and the calibration pulse height.
- Mask to determine which channels are to be calibrated.
- Two separate registers for masking channels from the trigger and from the readout.
- An eight-event deep FIFO buffer.
- Two redundant readout registers, including a feature to bypass chips having no hits.

- Two redundant trigger outputs, with low-voltage differential transmission from chip to chip.
- Two redundant serial-command decoders.
- Differential receivers for low-voltage-swing, differential transmission of signals to the chips, to avoid inducing noise into the amplifiers.
- Low-voltage operation (3 V), plus capability of operation with the 20 MHz clock turned off when not needed, for minimal power consumption.

Figure 1 shows a simplified block diagram of the readout chip. At present, the schematic-level design is complete, the mask layout is nearly complete, and simulations and verification are continuing, with the prototype fabrication to begin in December 1997.

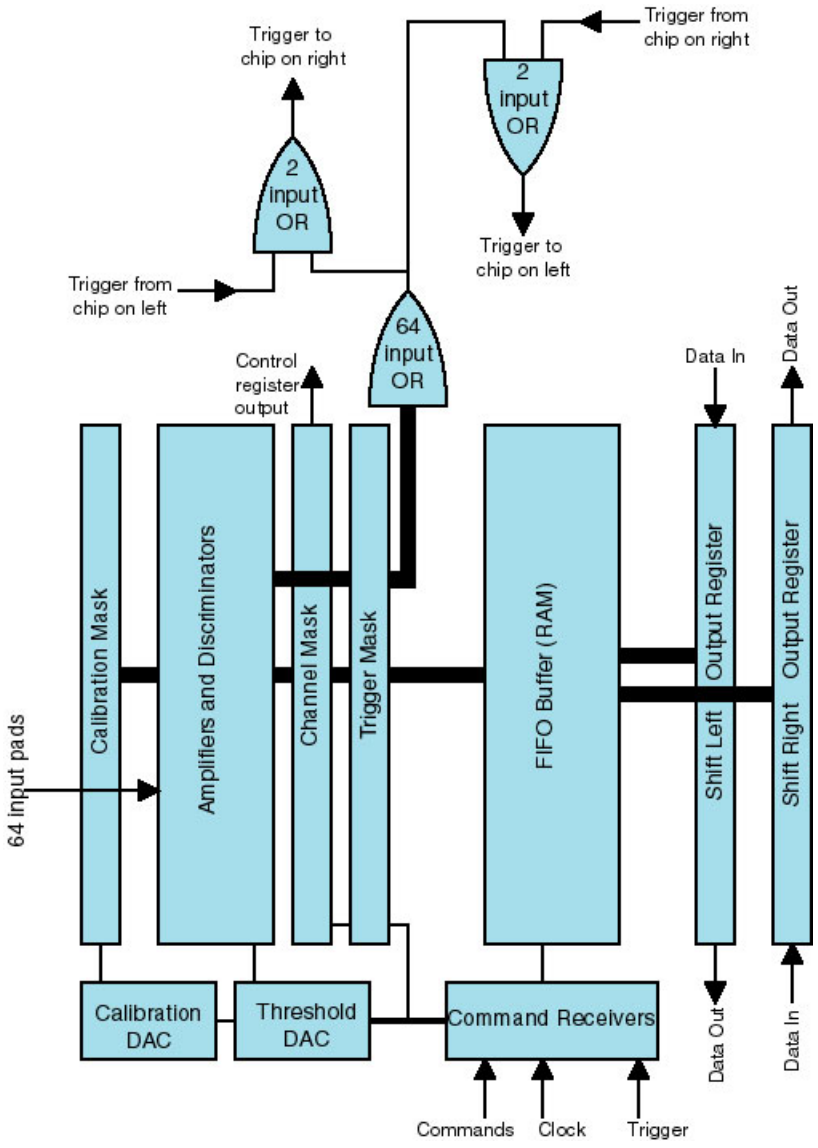

Figure 1. Simplified block diagram of the 64-channel front-end readout chip.

Prototype Results

The first prototype readout chip, with 16 channels, achieved a noise level of about 1400 electrons ENC for a capacitive load equivalent to 32 cm detector strips, with a power consumption of only 150 µW per channel and a peaking time of 1.6 µs. An example noise measurement is shown in Figure 2. The thresholds matched across the chip with an rms variation of 430 electrons ENC. A second prototype, with 32 channels and a 1.3 µs peaking time was fabricated for the beam test currently in progress and is functioning well in a system with a total of 2304 channels.

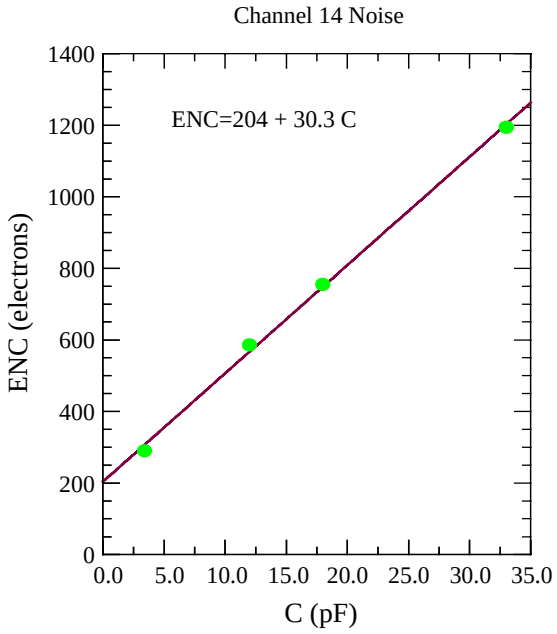

Figure 2. Noise measurement made on one channel of a 16-channel prototype chip, for four values of input capacitance.

Hybrid Circuits

The readout chips must be mounted on printed circuit boards located on the sides of the tracker trays, in order to minimize dead space around the tower perimeter. There is one 6.4 mm wide circuit board per ladder of five detectors, arranged side by side, as illustrated in Figure 3. Signals are passed from one circuit board to another by means of wire bonds. The two end boards each hold one controller chip, as well as the five front-end chips, and each is connected to the cables running up and down the tower. The circuit boards are connected to the detector plane via a flex circuit and wire bonds.

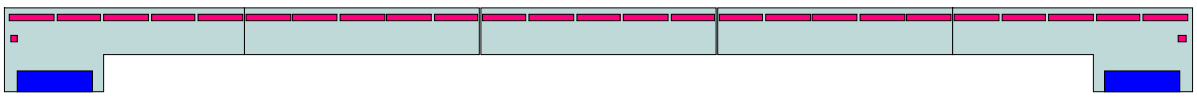

Figure 3. Arrangement of the five hybrid circuits along the edge of a tracker tray.

These tiny printed circuit boards must

- support the front-end readout chips and the tray-level readout control chips,
- filter and supply the bias voltage to the detectors,
- filter the two analog supplies for the chips and the digital supply,
- decouple the bias voltage to the 2V analog supply and decouple the two analog supplies to ground via low-inductance paths, in order to provide a low-noise return path for the current generated in the detectors,
- bus the digital signals between the controller chip and the front-end chips,
- support a connector to attach to the external cabling,
- provide space for gluing down the flex circuit that carries the signals and bias voltage to and from the detectors, and
- support a temperature monitor (on the end boards only).

The tight space and large number of interconnections results in a dense layout of 4 mil spaces and traces, as illustrated in Figure 4. Although four layers would be sufficient for all interconnects, eight are actually used, in order to provide shielding between the analog and digital circuitry and very low inductance paths to the decoupling capacitors. The analog traces, including the bias voltage, occupy the rear layers and are very broad (often entire planes) in order to provide low-inductance connections to the decoupling capacitors, which must lie on the top surface with the digital busses between them and the readout chips. Ground and power planes isolate the digital busses from the analog traces passing underneath. In addition, digital signals are propagated on differential lines with small voltage swings (of the order of 0.5 V). It is crucial that transitions on the digital lines not induce any significant charge (compared with the 1.5 fC threshold) into the amplifiers. That consideration, plus the need to provide return paths for the signal currents, dominates the hybrid design.

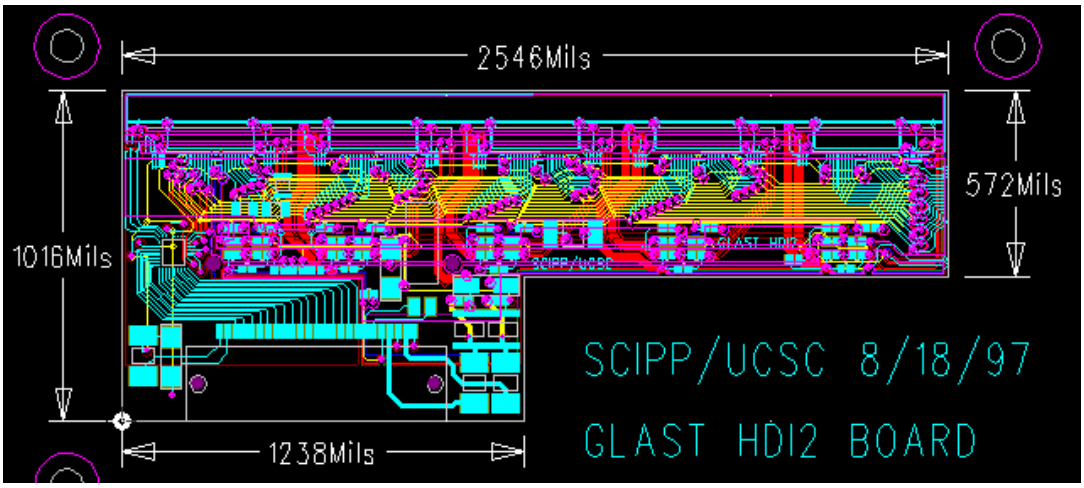

Figure 4. Prototype layout of the left-most hybrid circuit. It has spaces for five front-end chips, one controller chip, a connector, filter capacitors and inductors, fuses, termination resistors, a temperature sensor, and eight layers of interconnects and ground/power planes.

Prototypes of the central hybrids (*i.e.* ones with no connector) have been fabricated. The other two types have been designed, but fabrication is on hold pending a reevaluation of the connector choice.

Readout Control Chips

A digital chip is need in each detector plane to coordinate the readout of the 25 front-end chips. That "controller" chip is, in fact, duplicated, with one at each end of the readout chain for redundancy. Each front-end chip can move data and trigger signals either left or right, according to the setting of a bit in its control register. Therefore, the readout can be split in two in each layer between any pair of chips, in order to double the readout speed or, more importantly, to bypass a dead chip without losing the functionality of any other chip. Each controller chip can send a clock and command stream to one command decoder in each of the front-end chips and can, therefore, reinitialize any of the 25 chips to move the data and trigger signals in its direction.

The readout organization is illustrated in Figure 5, where only 3 of the 25 front-end chips per layer are shown. Whenever any of the unmasked channels on a layer fires, a trigger is generated and passed down the tower by the controller chip. The GLAST trigger logic has about 1.3 μs to respond with a trigger acknowledge (if there is a valid trigger), which is fanned out to the front-end chips by the controller chip. The front-end chips then latch the data into the FIFO buffer. At some later time a read command is sent

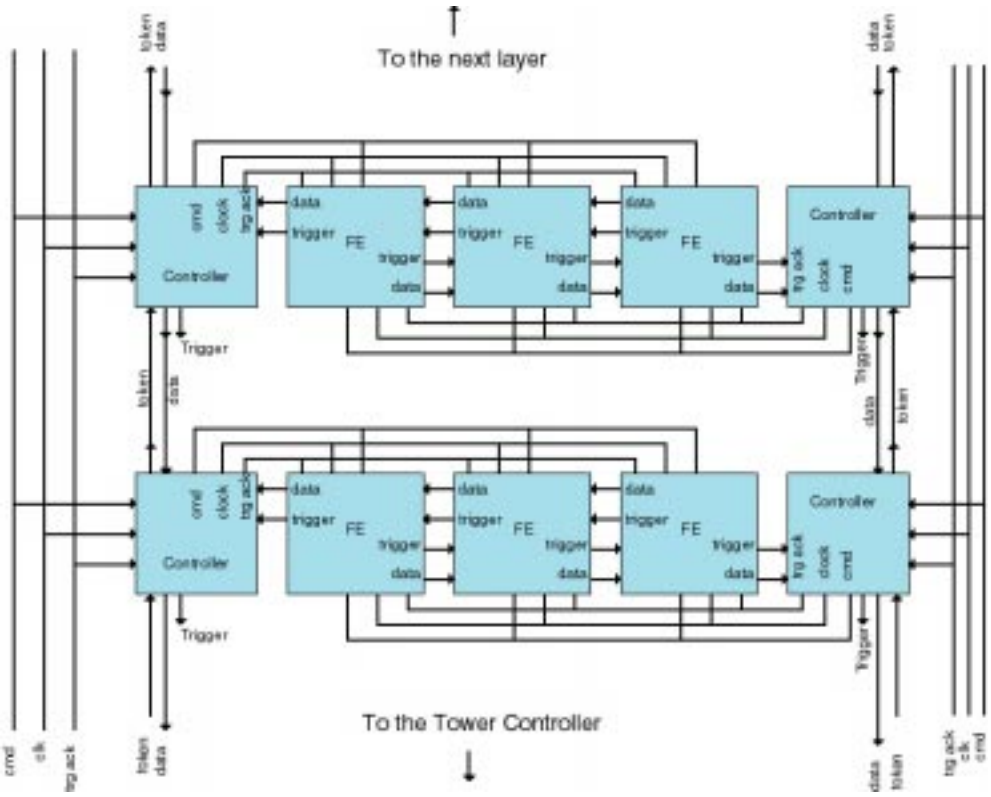

Figure 5. Simplified block diagram of the front-end readout of two adjacent layers, with only 3 of 25 readout chips shown.

to the controller chips. The data are then moved from the FIFOs into the output registers and shifted into the controller chips, where a list of hit channels is built. Finally, the data are read serially from the controller chips in a token-controlled daisy chain.

Specifications

In addition to controlling the readout and fanning signals out to the front-end chips, the controller chip also

- calculates a time-over-threshold for each trigger signal,
- controls the initialization of the front-end chips,
- and controls the calibration of the front-end chips.

Figure 6 shows a greatly simplified block diagram of the controller chip. The hit counter builds the sparse list of hits as the data flow in from the front-end chips. It can buffer hit lists for two events, so that the token-controlled readout can occur at the same time that the next event is being read from the front-end chips. The time-over-threshold counter has to be started with each trigger pulse produced by front-end chips on the layer. It stops after 1.3 μs if no trigger acknowledge has been received. Otherwise it continues until the end of the trigger pulse arrives. The results have to be buffered, just as are the data in the front-end chips. A command decoder interprets a set of 7 serial commands needed for initialization, calibration, and data acquisition.

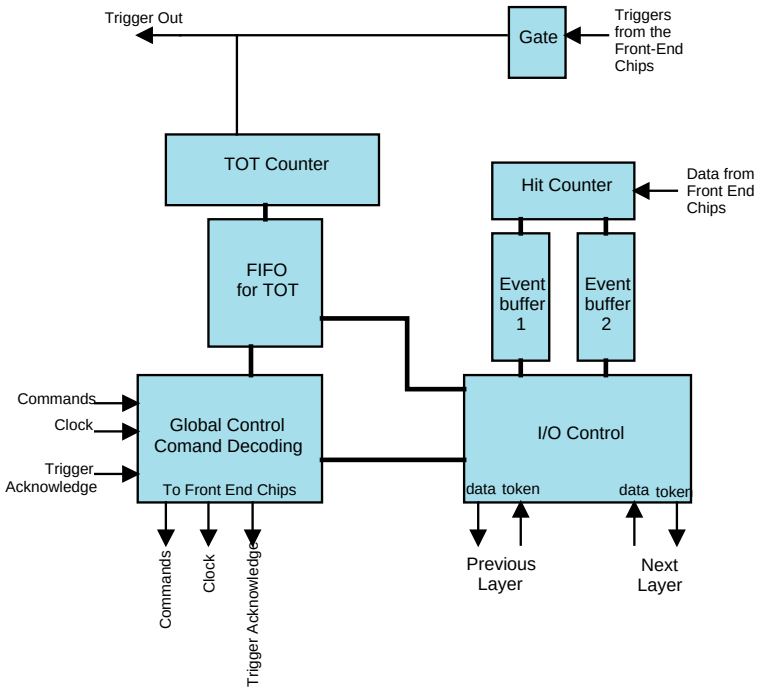

Figure 6. Simplified block diagram of a controller chip.

Design and Layout Status

The detailed design of the controller chip has been in progress since September 1997. Writing of an HDL description is well in progress, and the necessary tools for automatic generation of the logic circuit and most of the mask layout have been obtained from

Cadence and set up and tested. The layout will make use of the CMOSX standard cell library obtained from MOSIS and should be complete by the end of 1997.

Electronic Interconnects

The hybrid circuits handle the connections between front-end chips and controller chips. High density interconnects are also needed, however, between the front-end chips and the detectors and between all of the planes that comprise a tracker tower. Both of those tasks are foreseen to be handled by Kapton flex circuits.

A large almost-square flex circuit lies beneath the plane of 25 detectors to carry the bias voltage to their backs. We plan to use the same circuit to carry the signals and bias voltages around the tray corner to interconnect the detectors with the hybrid circuits. This circuit has two layers of metal. The upper layer, shown in Fig. 7, carries the bias voltages and signals, while the solid lower layer, which is connected directly to the analog ground on the hybrids, shields the sensitive detectors from noise that might be present in the conductive tray mechanical assembly. Eighth ounce copper is used, in order that the material in the kapton is a small fraction of that presented by the detectors themselves. The main part of this circuit is bonded to the surface of the tray before mounting detectors. The edge containing the 1606 4-mil traces (the white stripe at the top of Fig. 7) bends around the corner of the tray and bonds to the top surface of the hybrid circuits. In fact, the gluing, followed by wire bonding, will be done with the

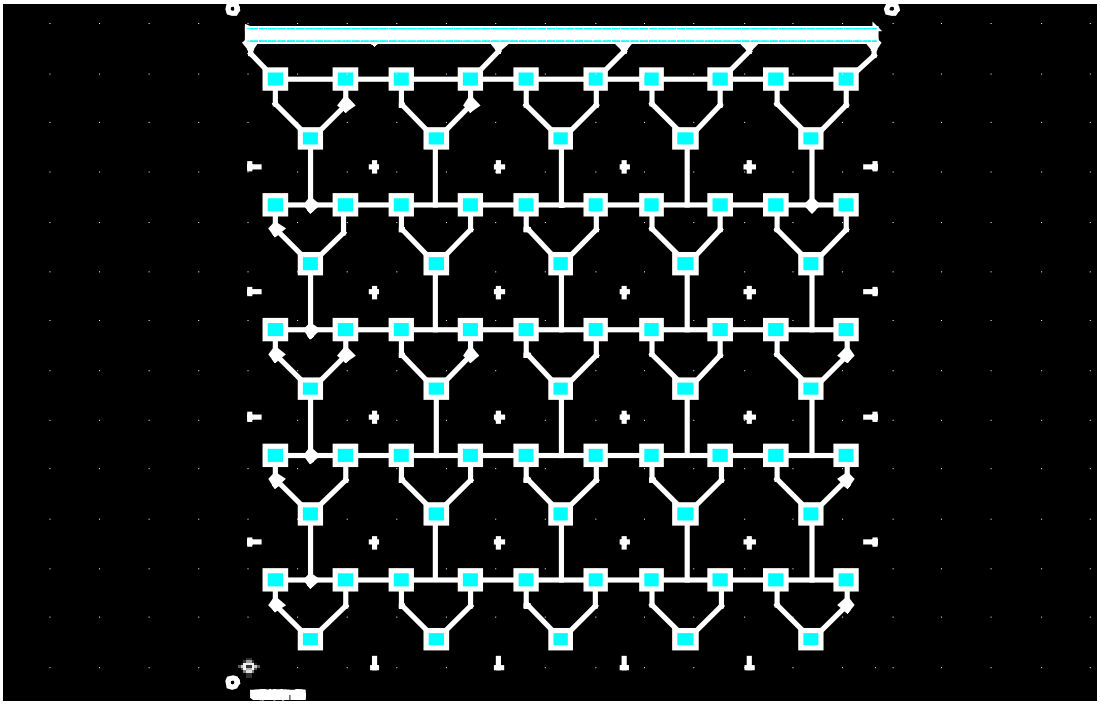

Figure 7. CAD drawing of the kapton flex-circuit interconnect that lies beneath the detectors to supply them with their bias voltage. Along the top edge it has short 4-mil traces to carry the signals and bias connections between detectors and the hybrid circuits.

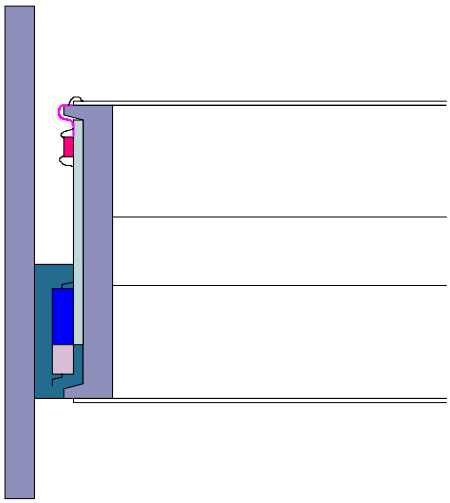

Figure 8. View of the edge of a tray, showing how the kapton flex circuit connects between the detectors and the readout chips.

detectors and hybrids jigged in a plane, after which the kapton will be folded around the corner and the hybrids attached to the side of the tray, as illustrated in Fig. 8. A thin sheet of light metal, or carbon-based material, must be bonded to the backs of the hybrids to support all five of them together during assembly. The kapton interconnect circuit has been completely designed, and prototypes will be fabricated soon.

Long, narrow, multi-layer kapton circuits will be used to interconnect the eight layers in a readout chain. Thus, each of the four sides of a tower will have two such kapton cables running up and down. The end of the cable that connects into the tower electronics below the calorimeter has 50 pins. Each connector on the hybrids has 25 pins. Eleven traces are bussed to all eight layers, while 32 traces go to only a single layer. Finally, eight traces are daisy chained from one layer to the next (for the data readout and the token). All signals are transmitted on differential pairs using balanced low-voltage-swing signals. The digital signal traces are sandwiched between digital power and ground planes, and the analog traces (analog power and detector bias) are separated from the digital traces. This circuit has been designed, with a particular choice of connector, but fabrication is awaiting a final decision on how best to connect to the hybrids.