Power consumption for the GTRC chip

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1. Introduction

The power consumption of a GLAST controller chip, GTRC, was measured. The chip was mounted in a chip carrier. The inputs and outputs of the chip were connected the following way:

Inputs	CMDI, CLKI, TACKI, TOKI, DIN, TRI	LVDS drivers
Output	CMDL, CLKL, TACKL, TOKO	1 kΩ between n and p line
Output	DOUT, TOUT	100 Ω between n and p line or 1 kΩ (depending of the address)
Input	RDINP, RDINN	0V or 3V Pattern generator
Input	A0 - A4	0V or 3V Pattern generator

The following contents was written into the register of the controller chip:

1. Readout the layer even if there is no hit
2. Calculate and add 11 bit check sum
3. Number of chips to read is 14

Some of the tests were performed with two different addresses for the controller chip. Also the termination for the data and fastOr output has been changed depending on the address.

- Chip address = 00000, termination: 100 Ω
- Chip address = 10110, termination: 1 kΩ

Quiescence and Clock-On Power

All inputs are in the default state, the register has been written.
The current was measured with no clock and with a continuos running clock. The data output (DOUT) and fastOr output (TOUT) were terminated with 100 Ω and 1000 Ω respectively.

	I [mA] (100 Ω termination) Chip address = 00000	I [mA] (1 kΩ termination) Chip address = 10110
Quiescence	5.3	4.6
Clock on (20 MHz)	8.38	7.7
Readout, 6 chips, 1hit/chip	8.68	7.9

(12kHz readout frequency)		

2. Power for Readout Cycle

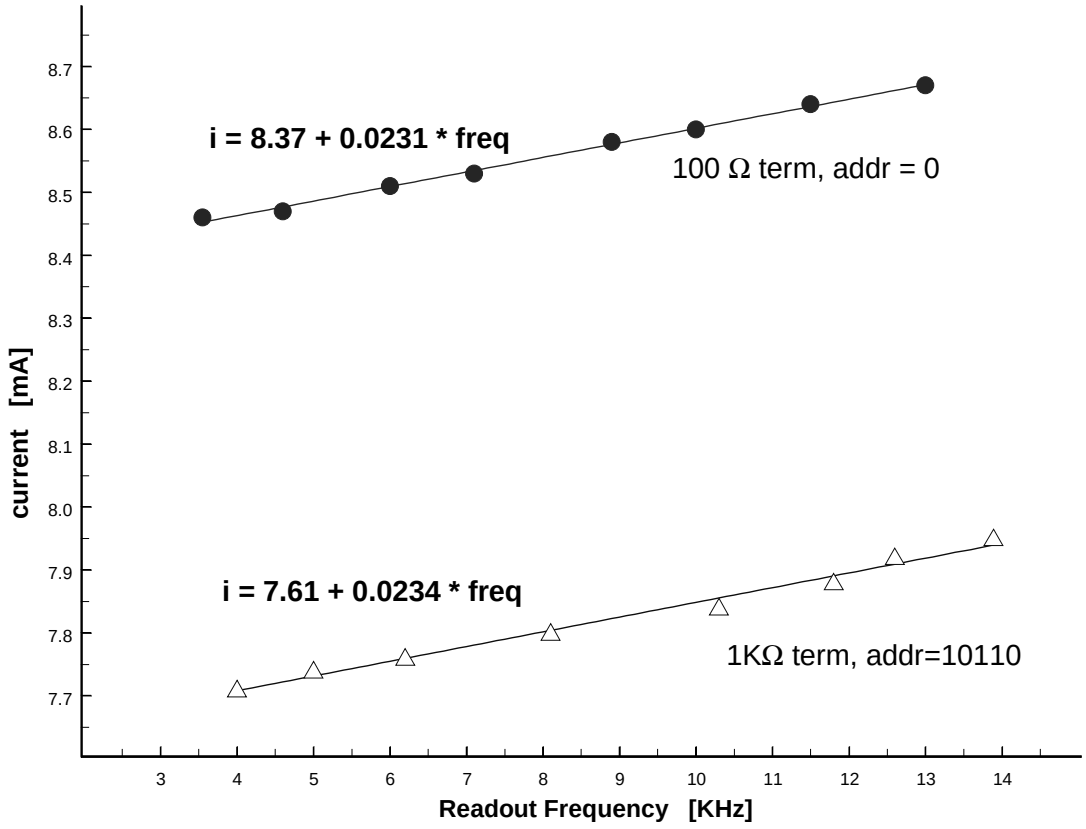
The readout cycle consisted of the following sequence:

1. FastOr, 31 cycles long (1.55 μs)
2. Trigger acknowledge 20 cycles (1μs) after the start of the fastOr
3. Read event command, two cycles after the end of the fastOr
4. Front-end data sequence (RDIN) starts 14 cycles after the last bit of the read-event command
5. The token-in is sent about 200 cycles after the last bit of the front-end data bit.

The standard pattern for the front-end data simulated that the first six chips recorded one hit per chip and the remaining eight chips recorded no hits (the number of chips in the controller register was set to be 14). The hits in the six chips were recorded in channel two.

Power versus readout frequency

The bit sequence for RDIN was chosen to simulate 6 GTFE chips with one hit per chip and 8 chips with no hits so that there are in total 6 hits. The following figure shows the current versus the readout frequency. The figure shows the results for the two different address settings.


i = 8.37 + 0.0231 * freq
100 Ω term, addr = 0
i = 7.61 + 0.0234 * freq
1KΩ term, addr=10110
current [mA]
Readout Frequency [KHz]
8.7
8.6
8.5
8.4
8.3
8.2
8.1
8.0
7.9
7.8
7.7
3
4
5
6
7
8
9
10
11
12
13
14

Power versus number of hits

The readout frequency was fixed to 12.1 kHz. The pattern for the front-end data (RDIN) simulated 6 chips with hits. The number of hits recorded in the first chip was varied. The number of hits in the remaining five chips was kept constant, to be one hit per chip.

Power versus GTFE clock cycles

The readout frequency was 12.1 kHz. The number of chips with one hit was varied between two chips (2 hits in total) and six chips (6 hits in total).